CB05

MICRO-PROJECTION MODULE

DESIGN SPECIFICATION

Issues Date: 08/18/2009

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Revision History:

VERSION	DESCRIPTION	DATE	APPROVED
A	CB05 Design Specification	08/18/2009	

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1. Overview

The purpose of this document is to describe the key performance characteristics of Butterfly Technology CB05 micro-projection module. The Module provides a compact solution for projecting bigger full color and high-quality video images on white screen. The main component of the Module is the low power FLC reflective micro-display panel, PBS, light compound system, three LEDs (R, G, B) and projection lens. The Module can be developed a micro projector or can be embedded in laptop, PDP, etc to project images out on screen or white wall.

Light from three LEDs is directed towards the panel, and the light being reflected from the panel makes up images that can be viewed on screen through a compact projection lens. The red, green and blue light from the LEDs is polarized and reflected by a polarizing beam splitter (PBS) onto the display panel. The light also passes through a pre-polarizer and diffuser to avoid stray light of unwanted polarization and to create an even illumination of the panel.

The micro-projection module CB05 works in a color sequential mode, which means that the image data for the colors red, green and blue are shown as three separate image fields in time. The human eye then integrates the three color images to produce the intended image and final color. To achieve this, the light source only emits one color at a time, and during that time the corresponding image data is shown on the display panel. This is done at a very high frequency in the module, typically at a frequency of 360 Hz (color field rate).

2. Specification Summary

Table 1: Specifications for optical engine module

Display format	800 (H) × 600 (V)
Pixel pitch	11.75 × 11.75 um
Aspect ratio	4:3
Color depth	16.777 million colors
Display frame rate	60 Hz (NTSC), 50 Hz (PAL)
Fill factor	91.7%
Brightness	Typ: >17 lumina
Contrast	Typ: 100:1 (FOFO)

CCT		6500~9000K
Light source		LED (RGB)
Color domain		>90% (NTSC)
Digital display interface	Video data	24 bit RGB
		24-bit 4:4:4 YCbCr
		24-bit 4:2:2 YCbCr
		8-bit 4:2:2 YCbCr
	Video timing	Hsync, Vsync, Valid, Clock
	Control	Sdat, Sck, Sen, Sout
Control interface		4 Wire serial
Power consumption for panel		88 mW
Power consumption for LEDs		Typ:8W (approximately)
Power supply voltage		Core 1.8V(±8%) (IC) Analog 5.0V (±10%) (LC) LED 2.8~3.5V
Dimensions (L× W × H)		67mm × 47mm× 19mm (max)
Operating temperature		-10°C to 70°C
Storage temperature		-30°C to 85°C

3. Block Diagram of Panel

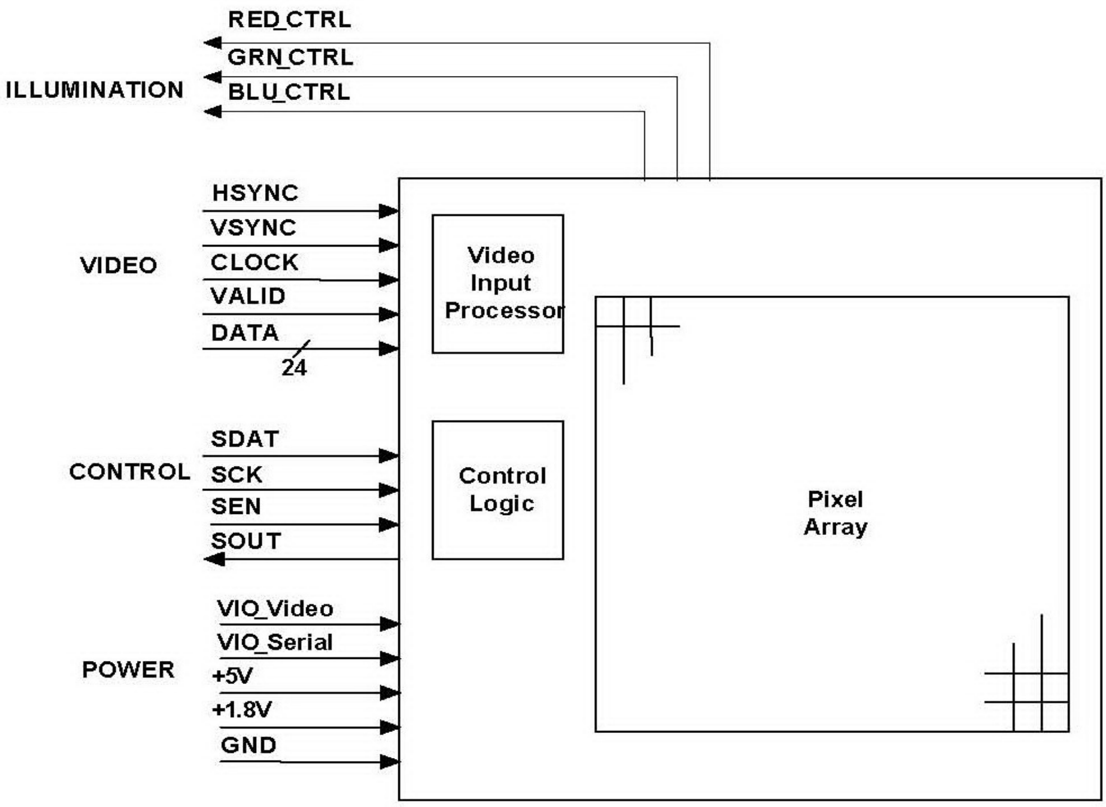


Figure 1: Block Diagram of Module Panel

4. Optical Specification

The Module optical system consists of three LEDs (red, green and blue), the FLC reflective micro-display panel, illuminator, PBS and projection lens. The passive optical components of the illuminator control the micro-display illumination and observation. A projection lens is supplied as part of the Module assembly. In combination, these optical components create a display system with quantifiable optical properties. The Module's optical performance therefore approximates a consumer display application (low cost polarizers, mechanically aligned polarizers and panel, f/1.7, and telecentric optics).

In comparison to conventional backlighting systems, the integral, low power LED package of the module reduces manufacturing costs and prolongs the life of the battery. The individual LEDs are turned on in a sequence. Sequential control of the FLC ON and OFF states relative to the LED's ON and OFF states defines the micro-display color at individual pixels of the FLC micro-display panel. A PBS in the illuminator assembly separates the illumination optical path from the imaging optical path. The PBS reflects off the PBS to the FLC micro-display panel. The state of each pixel controls the sates of the FLC polarization. When the pixel is in the ON state, the FLC rotates the linear polarization of the incident beam, maximizing the light transmitted by the PBS toward a viewer. When the pixel is in the OFF state, the FLC does not rotate the linear polarization of the incident beam which in turn, minimizes the light transmitted.

4.1 Duty Cycle

As for all liquid crystal devices, the electric field applied across the FLC needs to be “DC balanced” over time. The term “DC balanced” implies that the time average of the electrical field applied across any given area of the pixel array is zero. In practice, this means that if a certain field polarity was applied to a pixel for a time *t*, the opposite field polarity also needs to be applied over a time *t*. Therefore, each image being sent to and displayed by the display panel is followed by showing the inverse image on the display panel (this includes any “overhead” data). This functionality results in each pixel of the display showing exactly 50% gray when averaged over time. Since this would (predictably) not produce an image, the light source needs to be turned off during this inverse image time. This operation is shown graphically in Figure 2, along with the resulting LED output signals. The display panel is set for default operation of equal time for each color, as can be seen in the figure.

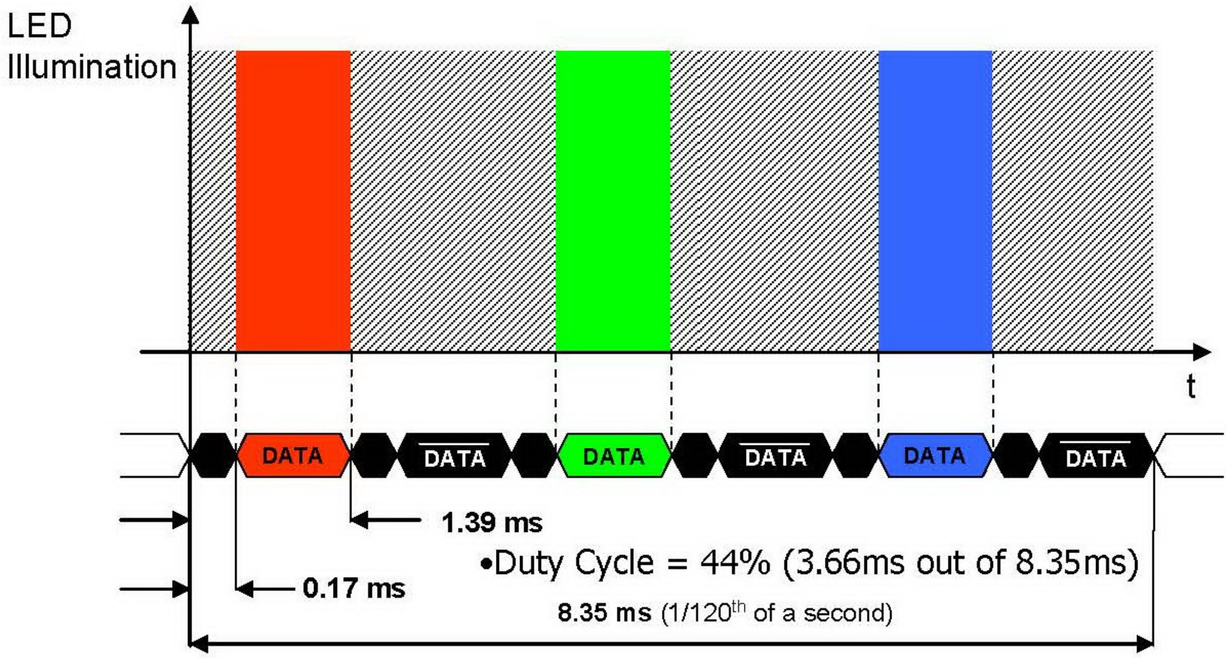


Figure 2: LED Illumination Duty Cycle

5. Mechanical Specification

5.1 Module Dimensions

The module is a flexible printed circuit board based package, with detachable flex connection. Envelope dimensions of the module package are shown in Figure 3.

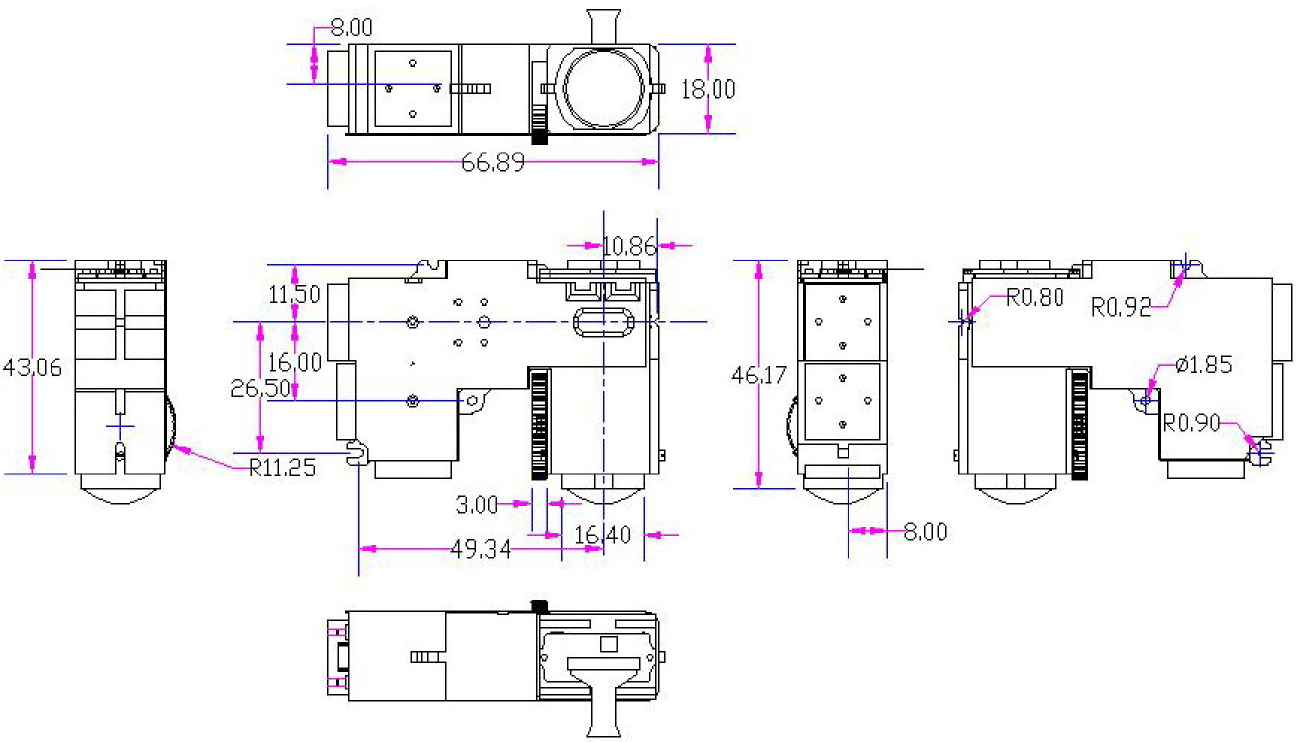


Figure 3: Optical Engine Module

Note 1: The 2D layout drawing is for reference. Please apply the 3D module supplied in details.

Note 2: The design does not include heat sink for RGB LEDs. Please pay attention to develop heat sink design.

5.2 Mounting Recommendations

The module is designed to mount into mobile systems, etc. Three locations of the Module should be referenced to the surface of the step. Electrical connection is made by means of an attached flex circuit. Mounting and electrical connecting of the module is designed for easy assembly reducing manufacturing time and complexity.

Refer to Figure 4 for detail of mounting dimensions for the module.

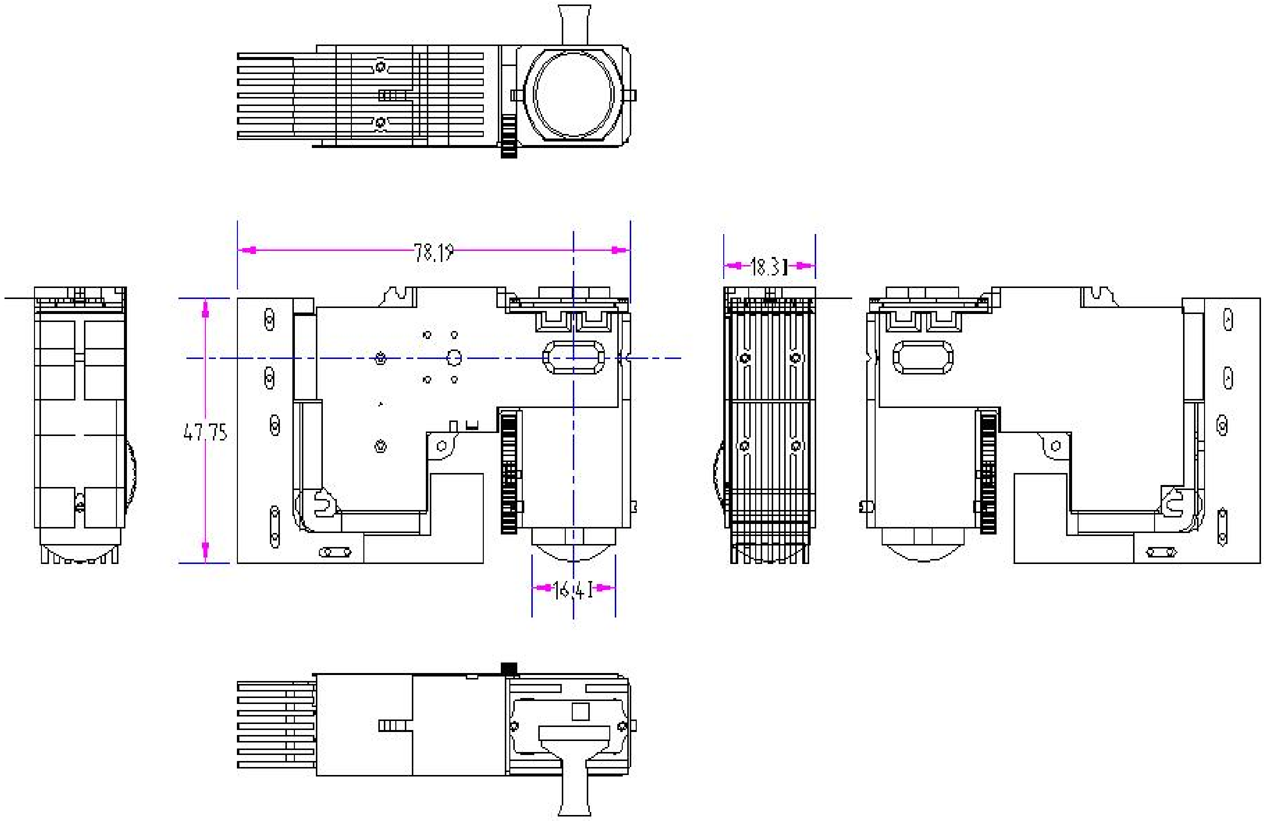


Figure 4: Mounting Dimensions for Module without LED Heat Sink System

5.3 Connector Recommendation

The type of connector chosen by the system designer is highly dependent on the application. The module provides 45 signals via pins at the end of the flex cable. The pins are spaced on a 0.3mm (0.30+0.30) pitch.

6. Electrical Specification

6.1 Theory of Operation

The display panel of the module is an LCOS micro-display, consisting of a CMOS integrated circuit. This IC acts as combined controller and display driver circuit. The display panel receives standard raster order RGB parallel video, the video can be cropped, scaled and color corrected. The processed video data is then stored to an on chip frame buffer. While a new image is being accumulated into a frame buffer, the previous frame of video data is then converted to the data necessary for sequential color operation and the voltage and timing of the display's pixels are controlled so as to recreate the color and gray shade for each pixel of the processed image.

6.2 Electrical Interface Specification

The display panel receives progressive scan raster order video data. The video may be formatted as 24 bit RGB, 4:4:4 YCbCr, 4:2:2 YCbCr, or 8-bit serial 4:2:2 YCbCr. Video timing signals Vsync, Hsync, and Clock are used to instruct the display where to position the video information. The video timing signal Valid may be used to indicate which period of which line to sample as the active data. Alternately, display registers may be programmed to instruct the display to automatically sample the video data after some delay from the end of the vertical and horizontal sync timing signals.

Three RGB illumination timing signals are generated by the display panel to control a separate illumination system.

A four wire serial interface is used to access the display panel's control registers. The details of the serial interface are outlined in the "Serial Interface" section.

A 1.8V digital power supply powers the IC. An analog 5V power supply is used to generate the necessary analog voltages to control the liquid crystal. The signaling voltages for the video interface and the serial interface are independently user selectable in the range of 1.8V to 3.3V. The video interface signaling voltage is set by the voltage applied to the Vio_Video pin and the serial signaling voltage is set by the voltage applied to the Vio_Serial pin.

The display panel contains a minimum of on-board bypass capacitance. The display drive system must then either provide low impedance power supplies or adequate de-coupling capacitance near the display to guarantee the specified power supply conditions are met.

The display panel is interfaced through a 0.3mm pitch flexible circuit. The flexible circuit connectors are two-row connectors. The connector pinout has been chosen so as to simplify the routing of the video data bus at the mating connector in which all the video signals are easily accessible and in order on one side of the two sided connector (illustrated in Figure 5).

However in the simplest flex circuit design, this pinout leads to the case where neighboring traces carry high speed video signals and sensitive control signals. Care must be taken in the design of the flexible cable and signal drivers so as to prevent crosstalk and ringing that would cause erroneous transitions on the control signals. The flex circuit length should be held to the minimum required for the application so as to reduce the level of crosstalk and ground impedance. The drive strength of the signal drivers should be minimized to the level necessary to operate at the desired frequency so as to slow the rise and fall times which will in turn limit crosstalk. The use of a ground plane in the flex circuit greatly reduces the ground impedance and may be helpful to control ringing, crosstalk, and ground bounce due to the simultaneous transitions of a large number of signals. Interleaving signal and ground traces is also useful for controlling crosstalk. All specifications for the electrical interface must be met at the display connector.

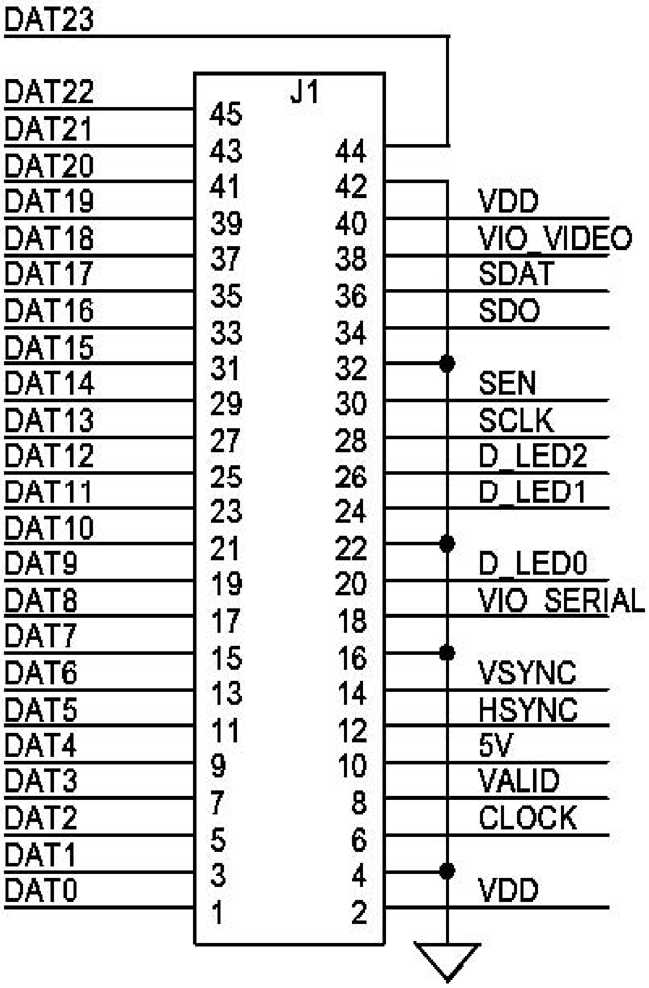


Figure 5: Illustration of Simplified Video Data Bus Routing

Table 2 shows the pin assignments for the 45 pin connector.

Pin	Name	I/O	Voltage Spec	Function
1	DATA 0	I	VIO_Video	
2	VDD	NA	NA	Core power supply (1.8V)
3	DATA 1	I	VIO_Video	
4	GND	NA	NA	Power and signal return
5	DATA 2	I	VIO_Video	
6	CLOCK	I	VIO_Video	CLOCK
7	DATA 3	I	VIO_Video	
8	VALID	I	VIO_Video	VALID
9	DATA 4	I	VIO_Video	
10	VCC	NA	NA	Analog power supply (5V)
11	DATA 5	I	VIO_Video	
12	HSYNC	I	VIO_Video	HSYNC
13	DATA 6	I	VIO_Video	
14	VSYNC	I	VIO_Video	VSYNC
15	DATA 7	I	VIO_Video	
16	GND	NA	NA	Power and signal return
17	DATA 8	I	VIO_Video	
18	VIO_Serial	NA	NA	I/O Voltage supply for Serial Interface Pins (VIO_Serial)
19	DATA 9	I	VIO_Video	
20	DLED_0	O	VIO_Serial	Digital Illumination Control Pad 0
21	DATA 10	I	VIO_Video	
22	GND	NA	NA	Power and signal return
23	DATA 11	I	VIO_Video	
24	DLED_1	O	VIO_Serial	Digital Illumination Control Pad 1
25	DATA 12	I	VIO_Video	
26	DLED_2	O	VIO_Serial	Digital Illumination Control Pad 2
27	DATA 13	I	VIO_Video	
28	SCLK	I	VIO_Serial	Serial interface clock input
29	DATA 14	I	VIO_Video	
30	SEN	I	VIO_Serial	Serial interface chip enable
31	DATA 15	I	VIO_Video	
32	GND	NA	NA	Power and signal return
33	DATA 16	I	VIO_Video	
34	SDO	O	VIO_Serial	Serial interface data output
35	DATA 17	I	VIO_Video	
36	SDAT	I	VIO_Serial	Serial interface data input
37	DATA 18	I	VIO_Video	
38	VIO_Video	NA	NA	I/O Voltage supply for Video Interface Pins (VIO_Video)
39	DATA 19	I	VIO_Video	
40	VDD	NA	NA	Core power supply (1.8V)
41	DATA 20	I	VIO_Video	
42	GND	NA	NA	Power and signal return
43	DATA 21	I	VIO_Video	
44	DATA 23	I	VIO_Video	
45	DATA 22	I	VIO_Video	

6.3 DC Operating Conditions

Table 3: DC Characteristics

Item	Symbol	Measurement Conditions		Min	Typ	Max	Unit
Input High Voltage	V_{IH_Video}	For all video inputs		VIO_Video *0.7	-	-	V
Input High Voltage	V_{IH_Serial}	For all serial inputs		VIO_Serial *0.7	-	-	V
Input Low Voltage	V_{IL_Video}	For all video inputs		-	-	VIO_Video *0.3	V
Input Low Voltage	V_{IL_Serial}	For all serial inputs		-	-	VIO_Serial *0.3	V
Input Capacitance	I_C	For all inputs, 3.3V Square wave @ 27Mhz		-	8	16	pF
Input Leakage Current	I_{IL}	$V_I = V_{IL\_Video}, V_{IL\_Serial}$		-10	-	-	µA
	I_{IH}	$V_I = V_{IH\_Video}, V_{IH\_Serial}$		-	-	10	µA
Output Low Voltage	V_{OL}	I_{OL} = 1mA		0.3	-	-	V
Output High Voltage	V_{OH}	I_{OH} = -1mA		-	-	VIO_Serial -0.3V	V
Supply Voltage	VDD			1.65	1.8	1.95	V
Supply Voltage	VCC			4.5	5.0	5.5	V
Supply Voltage	V_{VIO_Video}	User selectable, nominally 1.8 to 3.3V		1.65	3.3	3.6	V
Supply Voltage	V_{VIO_Serial}	User selectable, nominally 1.8 to 3.3V		1.65	3.3	3.6	V
Average Supply Current[1]	I_{VDD}	VDD=1.8V	Normal Mode[1]	-	46	TBD	mA
			Sleep Mode[2]	-	TBD	TBD	mA
Average Supply Current[1]	I_{VCC}	VCC=5.0V	Normal Mode[1]	-	0.3	TBD	mA
			Sleep Mode[2]	-	TBD	TBD	mA
Average Supply Current[1]	I_{VIO_Video}	VIO_Video = 3.3V	Normal Mode[1]	-	0.74	TBD	mA
			Sleep Mode[2]	-	TBD	TBD	mA
Average Supply Current[1]	I_{VIO_Serial}	VIO_Serial =3.3V	Normal Mode[1]	-	0.10	TBD	mA
			Sleep Mode[2]	-	TBD	TBD	mA

[1]Typical Values at 60 Hz, 800 x 600 operation with flat field video pattern at room temperature
[2]Typical Values with all inputs stopped at room temperature

6.4 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Item	Min	Max	Unit
VDD to GND	-0.5	2.5	V
VCC to GND	-0.5	6	V
VIO_Video to GND	-0.5	4	V
VIO_Serial to GND	-0.5	4	V
Voltage on any VIO_Video Input Pin to GND	GND-0.4	VIO_Video+ 0.4	V
Voltage on any VIO_Serial Input Pin to GND	GND-0.4	VIO_Serial+ 0.4	V

6.5 Video Input Signal Timing Requirements

All video input signals must meet the timing requirements shown on Figure 6 and Table 5.

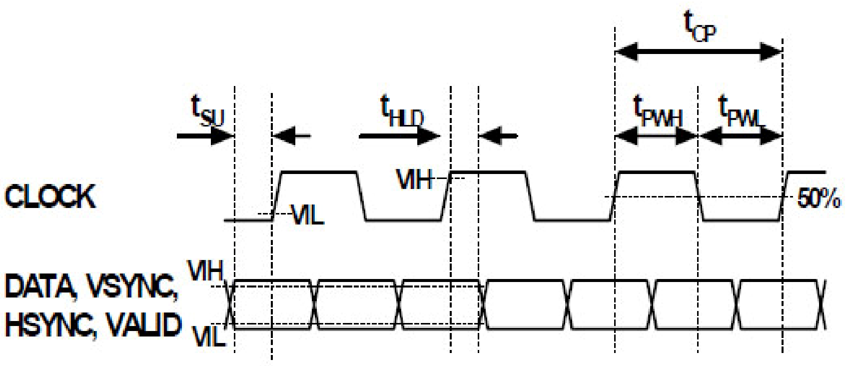


Figure 6: Video Input Signal Timing

Table 5: AC Characteristics, Video Input Signal Timing

Item	Symbol	Min	Typ	Max	Unit
CLOCK, rate	$1/t_{CP}$	25	27	41	MHz
CLOCK, pulse width high	t_{PWH}	40% t_{CP}	50% t_{CP}	60% t_{CP}	NA
CLOCK, pulse width low	t_{PWL}	40% t_{CP}	50% t_{CP}	60% t_{CP}	NA
DATA, VSYNC, HSYNC, VALID, setup time	t_{SU}	3			ns
DATA, VSYNC, HSYNC, VALID, hold time	t_{HLD}	3			ns

* Valid for a single clock per pixel input.

6.6 Serial Interface Signal Timing Requirements

All serial interface signals must meet the timing requirements shown in Figure 7 and Table 6.

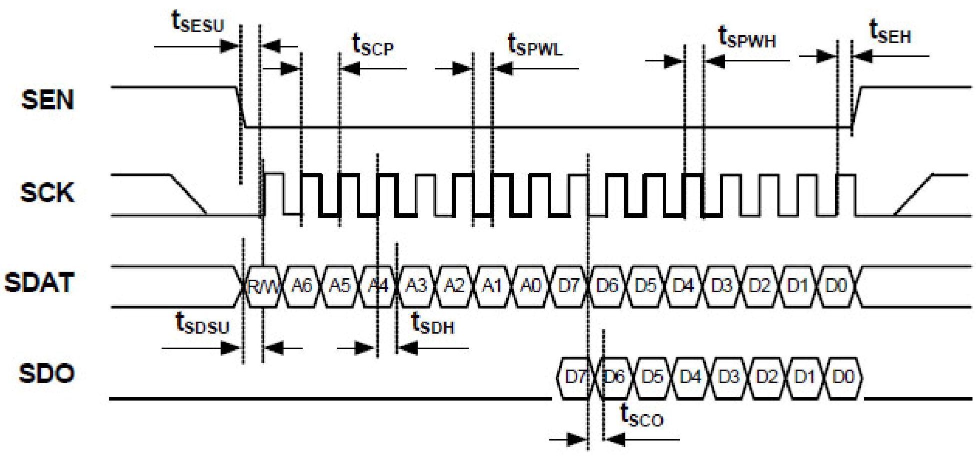


Figure 7: Four-wire Serial Interface

Table 6: AC Characteristics, Four-wire Serial Interface Timing

Item	Symbol	Min	Typ	Max	Unit
SCK, rate	$1/t_{SCP}$	100	-	7000	KHz
SCK, pulse width high	t_{SPWH}	45% tSCP	50% tSCP	55% tSCP	
SCK, pulse width low	t_{SPWL}	45% tSCP	50% tSCP	55% tSCP	
SDAT, setup time	t_{SDSU}	15	-	-	ns
SDAT, hold time	t_{SDH}	10	-	-	ns
SEN, setup time	t_{SESU}	15	-	-	ns
SEN, hold time	t_{SEH}	10	-	-	ns
SDO, clock to output time	t_{SCO}	-	-	20	ns

6.7 Control Sequence Requirements

Timing/sequence requirements must be met during power-up and power-down of the display panel. The required control sequence of the display panel is shown in Figure 8, and timing requirements are given in Table 7.

The power supplies may be enabled in any order. After the voltage supplies (VDD, VIO_Serial and VIO_Video) are present and in specification, and the **CLOCK** input is toggling, the display panel will load default register values from non-volatile memory to RAM for a time period of t_{PWRUP}. During this time period, the serial interface is ignored. The **CLOCK** must continue to toggle during a time period of t_{POCLK} from the end of the t_{PWRUP} time period. After the t_{POCLK} time period, the **CLOCK** input may continue to toggle or it may be disabled.

After the t_{PWRUP} period, the display panel will be in the Sleep state and the serial interface is active. The display panel is enabled by using the serial interface to set the **nSleep** bit of the Video Sleep Register. The VCC power supply must be present for a time period of t_{VCCUP} before the **nSleep** bit is set. If the VCC power supply is not present when the display is enabled, no image will be driven until VCC is detected. The **nSleep** bit may be set without the clock present, but the display will not be enabled until both the clock and a valid video signal are present.

For correct panel operation the control registers must be correctly programmed according to the input video signals and desired display operation. If the default values are incorrect, the serial interface is used to program the appropriate settings prior to enabling the display panel.

Once the display panel has been enabled, it must be disabled using the serial interface. For a time period t_{PWRDN} after the **nSleep** bit has been cleared the power supplies and **CLOCK** inputs must remain present. When the display panel is in the **Sleep** state, it will ignore data present on the video interface. As long as all power supplies are maintained at valid levels, the chip will remain in **Sleep** mode after the shutdown process, and all configuration register settings will be maintained. The display panel can be repeatedly enabled and disabled as desired.

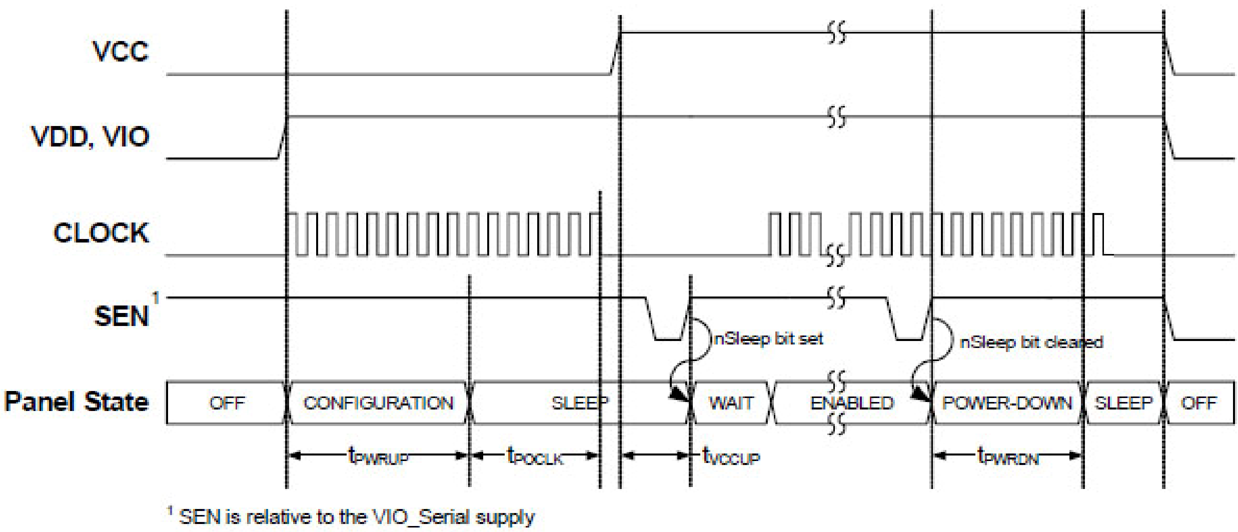


Figure 8: Power Up and Power Down Control Sequence

Table 7: AC Characteristics, Control Sequence Timing

Item	Symbol	Min	Typ	Max	Unit
Time from last valid power supply, and CLOCK present until display is ready for use	t_{PWRUP}	8	-	-	ms
Time from end of t_{PWRUP} period until CLOCK signal may be stopped.	t_{POCLK}	100	-	-	ms
Time from valid VCC power supply to enable of display using nSleep bit	t_{VCCUP}	1	-	-	ms
Time from disable of display panel to removal of first power supply	t_{PWRDN}	1500	-	-	µs

If it is desired to further reduce sleep mode power, the **CLOCK** input may be stopped after a time period t_{PWRDN} after the display panel has been disabled. The serial interface is active in the **Sleep** state even with no clock present, and all display registers may be written and read. The **nSleep** bit may also be set while the clock is stopped to allow the display to wake up as soon as the clock and a valid video signal are present again. Figure 9 shows the control sequence timing for the **Sleep** state, including setting the **nSleep** bit while the clock is stopped.

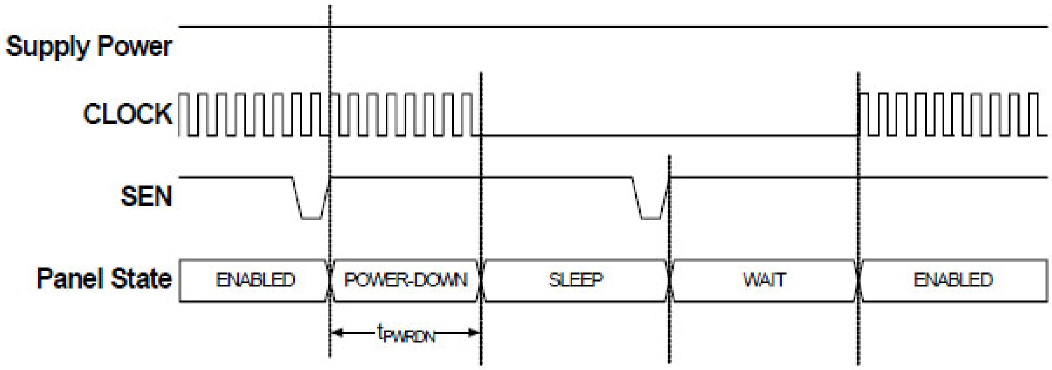


Figure 9: Sleep state Control Sequence

6.8 Video Input Interface

The display panel provides a universal parallel video interface. Video data may be formatted as RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2, or YCbCr 4:2:2 8-bit Serial Format. The display panel's sampling of video input data can be configured to any of three formats. The video input data bus would then be driven with the appropriate data signals as shown in the Table 8.

Table 8: Signal Assignment for Video Data Format Modes

Pin	RGB 4:4:4	YCbCr 4:4:4	YCbCr 4:2:2	YCbCr 4:2:2 8-bit Serial
DATA 0	RED0	Y0	Y0	Y0/Cb0/Cr0
DATA 1	RED1	Y1	Y1	Y1/Cb1/Cr1
DATA 2	RED2	Y2	Y2	Y2/Cb2/Cr2
DATA 3	RED3	Y3	Y3	Y3/Cb3/Cr3
DATA 4	RED4	Y4	Y4	Y4/Cb4/Cr4
DATA 5	RED5	Y5	Y5	Y5/Cb5/Cr5
DATA 6	RED6	Y6	Y6	Y6/Cb6/Cr6
DATA 7	RED7	Y7	Y7	Y7/Cb7/Cr7
DATA 8	GREEN0	Cb0	Cb0/Cr0	GND
DATA 9	GREEN1	Cb1	Cb1/Cr1	GND
DATA 10	GREEN2	Cb2	Cb2/Cr2	GND
DATA 11	GREEN3	Cb3	Cb3/Cr3	GND
DATA 12	GREEN4	Cb4	Cb4/Cr4	GND
DATA 13	GREEN5	Cb5	Cb5/Cr5	GND
DATA 14	GREEN6	Cb6	Cb6/Cr6	GND
DATA 15	GREEN7	Cb7	Cb7/Cr7	GND
DATA 16	BLUE0	Cr0	GND	GND
DATA 17	BLUE1	Cr1	GND	GND
DATA 18	BLUE2	Cr2	GND	GND
DATA 19	BLUE3	Cr3	GND	GND
DATA 20	BLUE4	Cr4	GND	GND
DATA 21	BLUE5	Cr5	GND	GND
DATA 22	BLUE6	Cr6	GND	GND
DATA 23	BLUE7	Cr7	GND	GND

The display panel's control registers can be set to specify the desired operating mode. In the first mode, the state of the VALID signal is used to indicate on which clocks the video data is to be sampled. In the second mode the display panel control registers are programmed to instruct the display panel to automatically sample video at fixed times after the assertion of the HSYNC and VSYNC signals. In the third mode, the VALID signal is a single clock pulse corresponding to start of the active video. In this mode, the display panel will begin sampling data automatically a number of clocks after the VALID pulse. The exact number of clock can be programmed to correspond to video guard band by programming additional control registers. Figure 10, Figure 11 and Table 9 provide the requirements for the video input format.

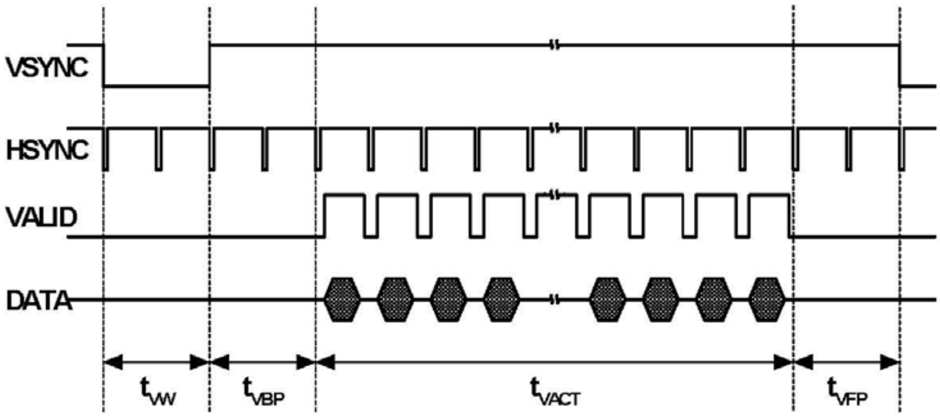


Figure 10: Video Input Vertical Timing

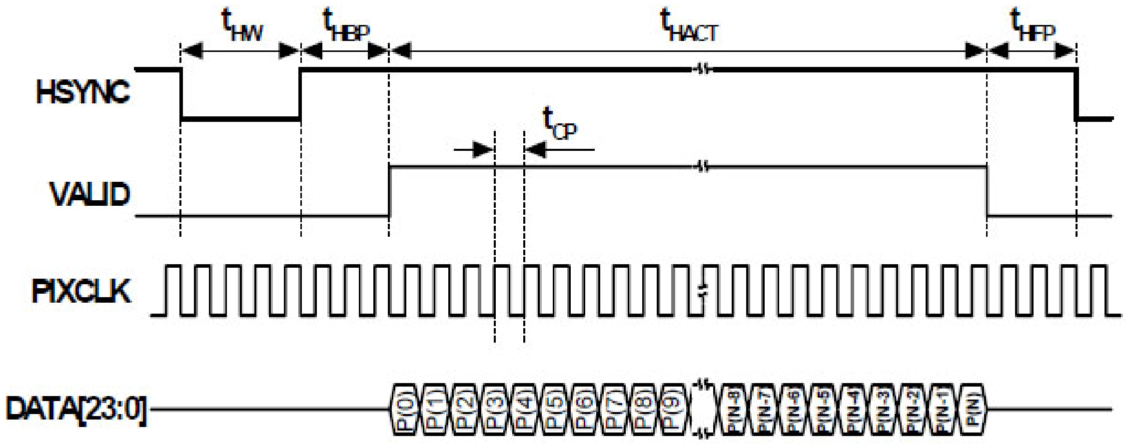


Figure 11: Video Input Horizontal Timing

Table 9: AC Characteristics, Vide Format Timing[1]

Item	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	t_{VF}	47	60	63	Hz
VSYNC, total lines	$t_{VTOT}= t_{VBLK}+ t_{VACT}$	612	628	968	Lines
VSYNC, active lines	t_{VACT}	600	600	768	Lines
VSYNC, blanking	$t_{VBLK}= t_{VFP}+ t_{VW}+ t_{VBP}$	12	28	200	Lines
VSYNC, front porch[2]	t_{VFP}	6	6	94	Lines
VSYNC, pulse width	t_{VW}	3	4	94	Lines
VSYNC, back porch	t_{VBP}	3	18	94	Lines
HSYNC, total clocks	$t_{HTOT}= t_{HBLK}+ t_{HACT}$	824	1056	1400	Clocks
HSYNC, active clocks	t_{HACT}	800	800	1280	Clocks
HSYNC, blanking	$t_{HBLK}= t_{HFP}+ t_{HW}+ t_{HBP}$	24	256	512	Clocks
HSYNC, front porch	t_{HFP}	12	40	256	Clocks
HSYNC, pulse width	t_{HW}	4	128	128	Clocks
HSYNC, back porch	t_{HBP}	8	88	256	Clocks
CLOCK, rate	$1/t_{CP}$	25	40	41	MHz

[1] All Minimum and Maximum timing specifications must be met simultaneously.
[2] The minimum VSYNC, front porch must be greater than 5000 clocks.

6.9 Serial Interface

The display panel is controlled by writing control registers via a serial interface. The serial interface follows the common industry standard 4-wire interface. The serial interface uses the signals SDAT, SCK, SEN and SOUT. The serial interface is activated by pulling the SEN input low. Then the SDAT input is sampled on each rising edge of the SCK input. A transfer is begun with the transfer of a read/write command bit and a 7-bit address.

For a write command, the command bit is set low and the 7-bit address is set to value of the register the user wishes to write. This is followed by an 8-bit data word to store that register address. Figure 12 illustrates a write command sequence.

For a read command, the command bit is set high and the 7-bit address is set to value of the register the user wishes to read. The display panel will output the addressed register's data to the SOUT output. The data is changed on the falling edge of the SCK input and can be sampled on each rising edge of the SCK input. Figure 13 illustrates a read command sequence.

As described in the Control Sequence Requirements section, for a time period of $t_{PWR\text{-}UP}$

following the application of power to the display, the serial interface is not accessible.

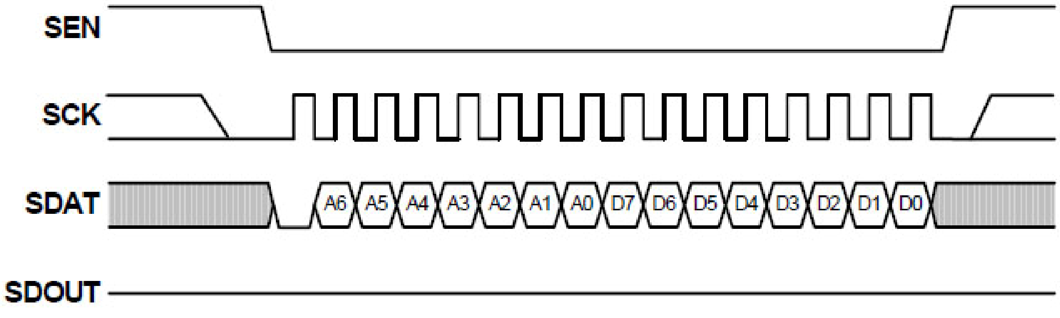


Figure 12: Serial Interface Write Example

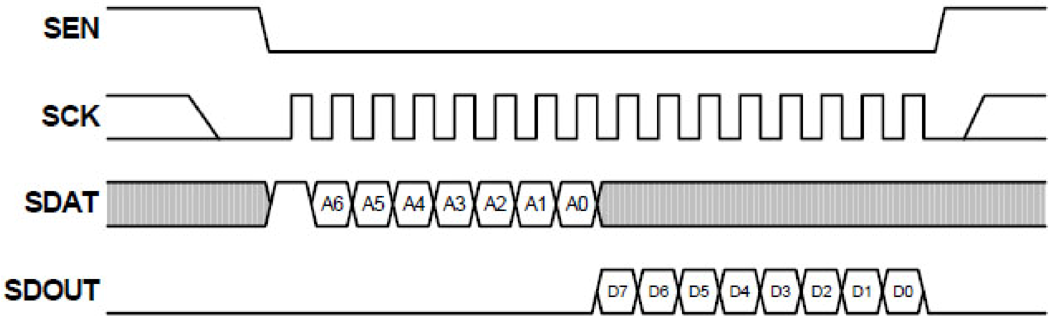


Figure 13: Serial Interface Read Example

6.10 Video Overscan and Scaling

The scaling engine can implement overscan by cropping the input image resolution down to the 800*600 active display pixels. Cropping is accomplished by internally delaying the sampling of video and sampling fewer lines and pixels. The scaling engine supports arbitrary input image resolutions, from 800 to 1280 horizontal pixels and 600 to 768 vertical lines. A higher resolution input image can be down scaled to the 800×600 active display pixels.

6.10.1 Overscan

Overscan is produced by delaying the sample time from the start of Valid data, and configuring the scaler to finish producing the desired output resolution before the end of valid data. Figure 14 illustrates how the HVldDelay and VVldDelay values are used to produce overscan. The HVldDelay and VVldDelay values determine the delay in sampling of Valid data. The scaler registers must be correspondingly programmed so as to finish sampling the Valid data early. The portion of the display resolution not occupied with input data will be automatically filled with black data.

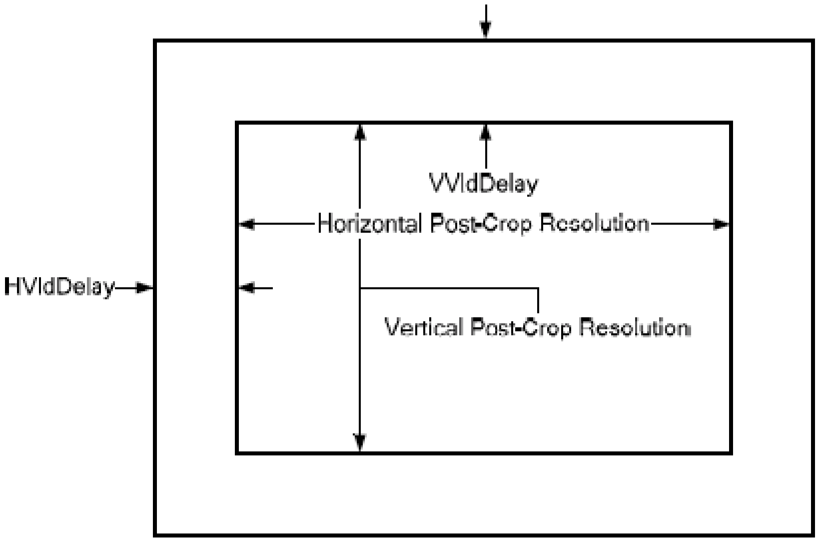


Figure 14: Overscan of the input image using VVldDelay and HVldDelay

The Horizontal sample delay HVldDelay (0Dh-0Eh) is always given in number of clocks, and the vertical sample delay VVldDelay (0Ch) is given in lines. If the valid signal is used, horizontal sampling is relative to the start of the valid signal, and vertical sampling is relative to the first valid line. In automatic video sampling mode, horizontal and vertical sampling are relative to their respective Sync signals.

6.10.2 Scaling

The scaling engine is based on a fractional accumulator to support arbitrary input resolutions from 800 horizontal pixels to 1280 horizontal pixels, and from 600 valid input lines to 768 valid input lines (after overscan). The horizontal and vertical scaling coefficients (HScaleStep and VScaleStep) determine the scaling ratio and horizontal and vertical cycle counts (HScaleCycle and VScaleCycle) reduce rounding error.

The Scaling registers control two bi-linear interpolators. The HScaleStep and VScaleStep register settings are determined as follows in decimal values (conversion to hexadecimal format must be done):

$$ScaleStep = \text{RoundUp}\left(\frac{512 * \text{Scaled Output Resolution}}{\text{Post Crop Resolution}}\right)$$

The Horizontal and Vertical Scaling Cycle Registers are used to re-set the scaling engine to prevent rounding error in the Scaling Step values from carrying over input data past the desired output pixel range. The Scaling Cycle values may be determined as follows in decimal values (conversion to hexadecimal format must be done):

$$ScaleCycle = \text{GreatestCommonDenominator}\left(\frac{\text{Post Crop Input}}{\text{Scaled Output Resolution}}\right)$$

Figure 15 illustrates the relationship of HScaleStep and HScaleCycle to the Post Crop Resolution and Scaled Output resolution. The same relationship exists for the VScaleStep and VScaleCycle. Table 10 gives several example calculations for both Horizontal and Vertical scaling both with and without Overscan. Note that the Scaled Output value always corresponds to the VGA's native 800 x 600 displayed resolution.

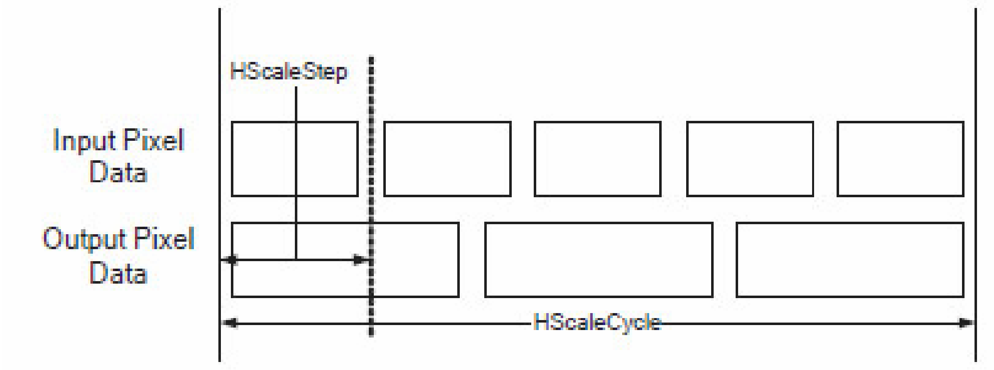


Figure 15: Scaling Coefficients

Table 10: Sample Scaling Coefficients

Exampe	Input Res	VldDly	Post Crop Res	Scaled Output	GCD	Step (dec)	Cycle (dec)	VldDly (dec)	Step [9:0] (hex)	Cycle [9:0] (hex)	VldDly [9(7):0] (hex)
1024 In, no overscan	1024	0	1024	800	32	400	25	0	190	19	0
1024 In, 50 pix overscan	1024	50	924	800	4	444	200	150	1BC	C8	96
1280 In, no overscan	1280	0	1280	800	160	320	5	0	140	5	0
1280 In, 50 pix overscan	1280	50	1180	800	20	348	40	150	15C	28	96
720 In, no overscan	720	0	720	600	120	427	5	0	1AB	5	0
720 In, 50 pix overscan	720	50	620	600	20	496	40	50	1F0	1E	32

6.11 Configuration Registers

The configuration registers are set at power-up by the integrated EEPROM, subsequently they can be read and written with the four-wire serial interface. Any register not described is considered Reserved and is not intended for customer use. Altering Reserved registers is not supported and may result in erroneous operation.

6.11.1 Display Configuration Page Register, with Default Settings

Register Index: 00h. Register is Read Only

7	6	5	4	3	2	1	0
Configuration Page							
A9h							

Configuration Page: A9= Page 1. All other pages are reserved.

6.11.2 Video Mode Register, with Default Settings

Register Index: 01h. Register is RW

7	6	5	4	3	2	1	0
CSpaceSel	ChannelMap			DataChannel		DataSequence	
0	000			00		00	

CSpaceSel: Color Space Select, 0=RGB, 1=YCbCr
ChannelMap: Select mapping of data channel to color information, dependent on the Data Channel setting according to the following table.

Channel Map	24-bit RGB [23:16]	[15:8]	[7:0]	24-bit YCbCr [23:16]	[15:8]	[7:0]	16-bit YCbCr [23:16]	[15:8]	[7:0]	8-bit YCbCr [23:16]	[15:8]	[7:0]
0h	Blue	Green	Red	Cr	Cb	Y		Cb/Cr	Y			Y/Cb/Cr
1h	Green	Red	Blue	Cb	Y	Cr		Y	Cb/Cr		Y/Cb/Cr	
2h	Red	Blue	Green	Y	Cr	Cb	Cb/Cr	Y		Y/Cb/Cr		
3h	Red	Green	Blue	Y	Cb	Cr	Y	Cb/Cr				
4h	Green	Blue	Red	Cb	Cr	Y	Cb/Cr		Y			
5h	Blue	Red	Green	Cr	Y	Cb	Y		Cb/Cr			

DataChannel: 00=24-bit data interface, 01=16-bit data interface, 10=8-bit data interface
DataSequence: Data Sequence, 00 for 24-bit RGB interface. Selects sequence of color information for 16-bit and 8-bit interface modes according to the following table.

DataSequence	16-bit YCbCr	8-bit YCbCr
00	[Y_0Cb] [Y_1Cr]	[Cb] [Y_0] [Cr] [Y_1]
01	[Y_0Cr] [Y_1Cb]	[Cr] [Y_0] [Cb] [Y_1]
10		[Y_0] [Cb] [Y_1] [Cr]
11		[Y_0] [Cr] [Y_1] [Cb]

6.11.3 Video Configuration Register, with Default Settings

Register Index: 02h. Register is RW

7	6	5	4	3	2	1	0
VPol	HPol	ValidPol	RES	RES	RES	SyncMode	
1	1	0	0	0	0	00	

VPol: Vertical Sync Polarity, 0=Active High, 1=Active Low.
HPol: Horizontal Sync Polarity, 0=Active High, 1=Active Low.
ValidPol: Valid input Polarity, 0=Active High, 1=Active Low.
SyncMode: 00=Use HSync, VSync, and Valid inputs for video timing, 01=Use HSync and VSync inputs, with Valid timing specified from Valid delay registers, 10=Reserved, 11=Reserved

6.11.4 Gamma Register, with Default Settings

Register Index: 05h. Register is RW

7	6	5	4	3	2	1	0
RES	DLEDInv	DLEDEn	RES	GammaVal			
0	0	0	0	9h			

DLEDInv: 0=Active high digital LED output s, 1=Active low digital LED outputs
DLEDEn: 0=Disable digital LED outputs, 1=Enable Digital LED outputs
GammaVal: Selected display gamma, values shown in the table below

GAMMAVAL	DISPLAY GAMMA	GAMMAVAL	DISPLAY GAMMA
0h	1.0	8h	2.0
1h	1.2	9h	2.1
2h	1.4	Ah	2.2
3h	1.5	Bh	2.3
4h	1.6	Ch	2.4
5h	1.7	Dh	2.6
6h	1.8	Eh	2.8
7h	1.9	Fh	3.0

6.11.5 Video Configuration Register, with Default Settings

Register Index: 06h. Register is RW

7	6	5	4	3	2	1	0
RES	VFlip	HFlip	RES	nSleep	RES		
0	0	0	0	0	000		

VFlip: Flip display vertically, 0=Don't flip, 1=Flip
HFlip: Flip display horizontally, 0=Don't flip, 1=Flip
nSleep: Sleep Mode, 0=Sleep Mode, 1=Normal mode

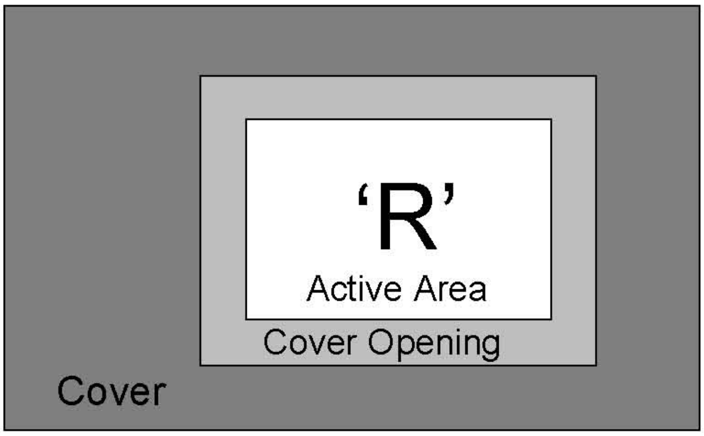


Figure 16: Display Orientation with VFlip=0 and HFlip=0

6.11.6 Scaling Coefficient Registers, with Default Settings

Register Index: 07-0Bh. Register is RW

Index	Default	7	6	5	4	3	2	1	0
07h	22h	HScaleCycle[9:8]		HScaleStep[9:8]		VScaleCycle[9:8]		VScaleStep[9:8]	
08h	00h	VScaleStep[7:0]							
09h	01h	VScaleCycle[7:0]							
0Ah	00h	HScaleStep[7:0]							
0Bh	01h	HScaleCycle[7:0]							

HScaleStep: Horizontal scaling repeat count
HScaleCycle: Horizontal scaling repeat count
VScaleStep: Vertical Scaling Coefficient
VScaleCycle: Vertical scaling repeat count

6.11.7 Vertical Valid Delay Register, with Default Settings

Register Index: 0Ch. Register is RW

7	6	5	4	3	2	1	0
VVldDelay [7:0]							
00h							

VVldDelay: Vertical Valid delay.

6.11.8 Horizontal Valid Delay 2 Register, with Default Settings

Register Index: 0Dh. Register is RW

7	6	5	4	3	2	1	0
RES						HVldDelay[9:8]	
00						00	

6.11.9 Horizontal Valid Delay Register, with Default Settings

Register Index: 0Eh. Register is RW

7	6	5	4	3	2	1	0
HVldDelay[7:0]							
00h							

HVldDelay: Horizontal Valid Delay, delay from horizontal valid assertion to sampled video when using Valid input, otherwise delay from HSync assertion to sampled video - 2.

6.11.10 Panel Clock Frequency Register, with Default Settings

Register Index: 0Fh. Register is RW

7	6	5	4	3	2	1	0
PClkFreq7:0]							
50h							

PClkFreq: This value must be 2X the applied clock frequency in hex. The default value is based on a specified input clock frequency of 40 MHz (40 x 2 = 50h). This register **must** be set to twice the input clock frequency for display to operate correctly.

6.11.11 Color Space Gain Registers, with Default Settings

Register Index: 12-1Ah. Register are RW

Index	Default	7	6	5	4	3	2	1	0
12h	00h	ColorSpace11							
13h	00h	ColorSpace12							
14h	00h	ColorSpace13							
15h	00h	ColorSpace21							
16h	00h	ColorSpace22							
17h	00h	ColorSpace23							
18h	00h	ColorSpace31							
19h	00h	ColorSpace32							
1Ah	00h	ColorSpace33							

6.11.12 Color Space Offset Registers, with Default Settings

Register Index: 1B-1Dh. Register are RW

Index	Default	7	6	5	4	3	2	1	0
1Bh	00h	ColorOffset1							
1Ch	00h	ColorOffset2							
1Dh	00h	ColorOffset3							

The CSpaceSel bit of the Video Mode register (register 01h, bit 7) determines the base color space transformation for RGB or YCrCb data as shown in the following figure, part (a) for RGB and part (b) for YCrCb. The coefficients for the selected RGB or YCrCb transformation are highlighted in yellow. The base color space transformation may be modified using the 8-bit signed number color space adjustment values from configuration registers ColorSpace11-ColorSpace33 (12h-1Ah) and ColorOffset1-ColorOffset3 (1Bh-1Dh), highlighted in blue. A value of 0 for CSpaceSel selects the base transformation in Figure 17(a), used for RGB input data while a value of 1 for CSpaceSel selects the base transformation in Figure 17 (b), for YCbCr input data.

$$\begin{bmatrix} R_O \\ G_O \\ B_O \end{bmatrix} = \frac{1}{128}\begin{bmatrix} 128+cs_{11} & 0+cs_{12} & 0+cs_{13} \\ 0+cs_{21} & 128+cs_{22} & 0+cs_{23} \\ 0+cs_{31} & 0+cs_{32} & 128+cs_{33} \end{bmatrix} \bullet \begin{bmatrix} R_I+O_1 \\ G_I+O_2 \\ B_I+O_3 \end{bmatrix}$$

(a)

$$\begin{bmatrix} R_O \\ G_O \\ B_O \end{bmatrix} = \frac{1}{128}\begin{bmatrix} 128+cs_{11} & 0+cs_{12} & 175+cs_{13} \\ 128+cs_{21} & -42+cs_{22} & -90+cs_{23} \\ 128+cs_{31} & 222+cs_{32} & 0+cs_{33} \end{bmatrix} \bullet \begin{bmatrix} Y_I+O_1 \\ Cb_I-128+O_2 \\ Cr_I-128+O_3 \end{bmatrix}$$

(b)

Figure 17: Base Color Space Transformation

6.11.13 Red Ratio Register, with Default Settings

Register Index: 3Ch. Register is RW

7	6	5	4	3	2	1	0
RedRatio[7:0]							
55h							

RedRatio: Ratio out of 256 time periods for Red Display time.

6.11.14 Green Ratio Register, with Default Settings

Register Index: 3Dh. Register is RW

7	6	5	4	3	2	1	0
GreenRatio[7:0]							
56h							

GreenRatio: Ratio out of 256 time periods for Green Ramp time.

6.11.15 Blue Ratio Register, with Default Settings

Register Index: 3Eh. Register is RW

7	6	5	4	3	2	1	0
BlueRatio[7:0]							
55h							

BlueRatio: Ratio out of 256 time periods for Blue Ramp time.

The sum of the Red, Green, and Blue Ratios may not exceed 256d. To ensure this, color registers being reprogrammed should be done in order of smallest values first.

6.11.16 Temperature Measurement Register

Register Index: 56h. Register is Read Only

7	6	5	4	3	2	1	0
ChipTemp[7:0]							
FFh							

ChipTemp: Chip temperature measurement. The on-chip temperature sensor records temperature as an 8-bit NTC value. The following formula may be used to translate the temperature sensor value to degrees Celsius:

TempDegreesC=-30.4559 + (0.53163*DecimalTempRegisterCode)

6.11.17 ID Code Registers, with Default Settings

Register Index: 78h-7Ah. Register are Read Only

Index	7	6	5	4	3	2	1	0
78h	IDCode[7:0]							
79h	IDCode[15:8]							
7Ah	IDCode[23:16]							

IDCode: This 24 bit code is a unique serial number for each display device.

7. Reliability Specification

7.1 Operating Environment

Temperature: 0°C~ 40°C

Humidity: 20~80%

Avoid corrosive and combustible environment.

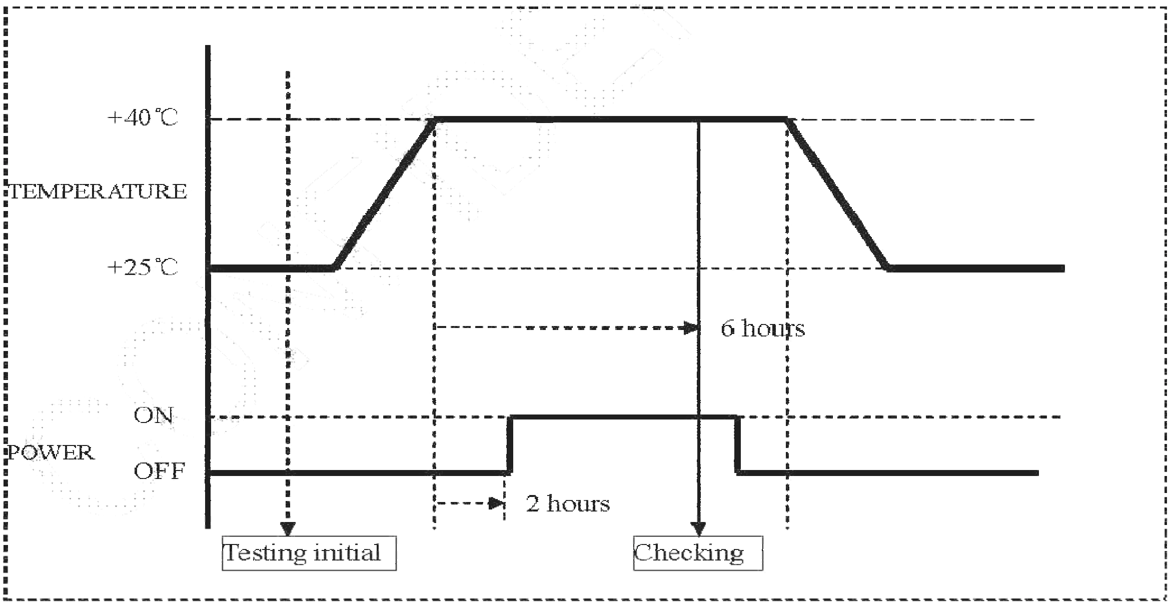
7.2 Transport and Storage Environment

Temperature: -10°C~ 60°C

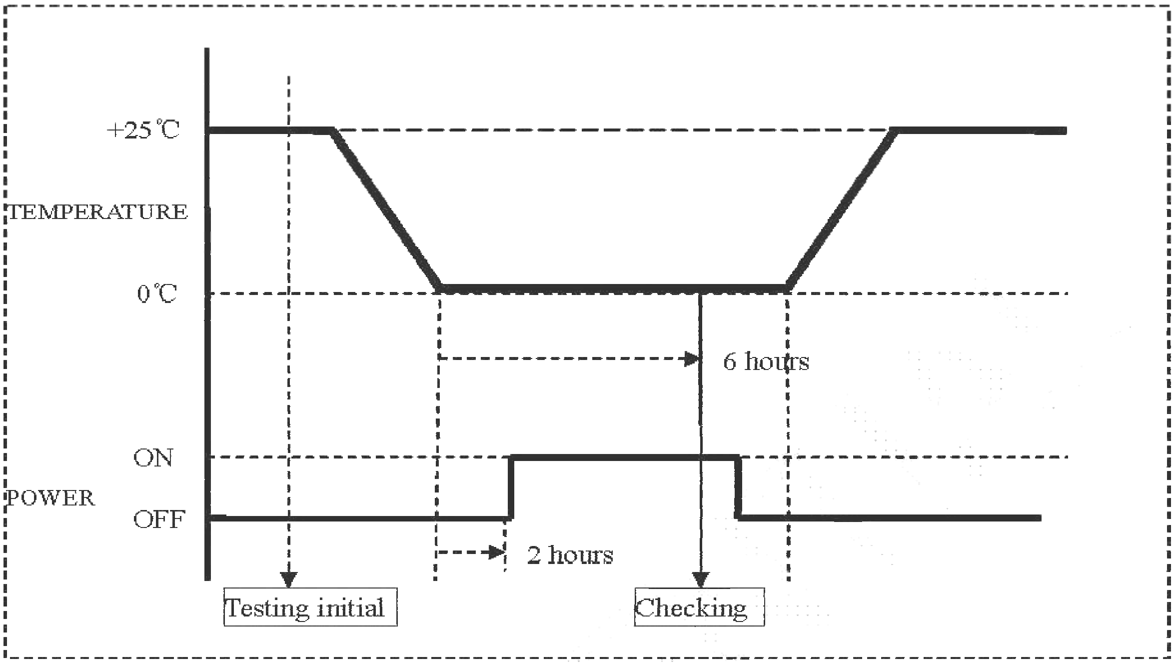
Humidity: 20~80%

Avoid corrosive and combustible environment, moistureproof package.

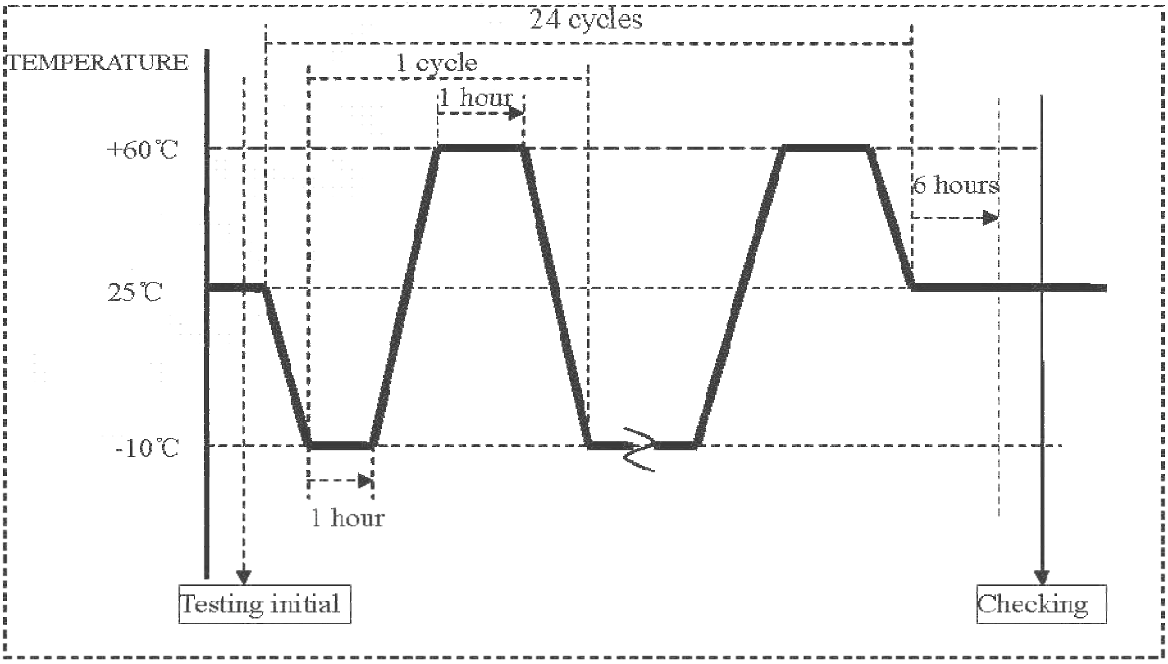
7.3 High Temperature Testing for Operation



7.4 Low Temperature Testing for Operation



7.5 Temperature Cycle Testing for Packaging Storage



Testing instrument: SBTH-2-030N

Notes: Speed for temperature goes up and down is (0.7~1°C)/min.

7.6 Sinusoidal Vibration Testing for Package Storage

Frequency: 30~55~30Hz

Amplitude: 0.25mm

Direction: Z axis

Cycle times: 5

Sweep frequency: 1 octave/min

Peak acceleration: 2.0G

Round trip Time: 15min

7.7 Drop Testing for Package Storage

Height: UL

Amplitude: 5 Sides/2 flanks/1 edge

Shocked surface: Concrete, smooth

8. Handing Caution

- During optical engine module assembly process, wearing anti-static gloves shall be required, and please handle with care.
- The module with LCOS panel is built with various sensitive electronic parts and components. Therefore it must be grounded by ESD protection equipment (wrist band, foot grounder etc.) before handing.
- For optical engine module with FPC, avoid excessive bending of FPC.
- Turn off the power when connecting or disconnecting the module.
- Follow the proper instructions when connecting modules to other devices.
- All necessary ESD precautions shall be taken to avoid damage to the product.
- Avoid scratch the outside surface of projection lens and FPC.
- Avoid pull FPC and wire of LED excessively.
- Avoid drop ground without any package.

9. Packaging Specification

- Product dimensions: 67×47×19mm (Max. without heat sink system)
  79×48×19mm (Max. with heat sink system)
- Packaging item list: Optical engine module ×1
  Data sheet ×1
- Packaging: TBD