Key Features

Processor

- XuanTie C907 RISC-V CPU

Memory

- DDR2/DDR3/DDR3L, up to 256MB
- eMMC4.41, SPI Flash

Video Engine

- Video decoding
  - H.264, up to 1920x1080@30fps
  - MPEG-4, up to 1920x1080@30fps
  - MPEG-1/2, up to 1280x720@30fps
- Image decoding
  - JPEG, Maximum resolution: 16384x16384
  - PNG, Maximum resolution: 2048x2048
- Video encoding
  - JPEG/MJPEG up to 1280x720@30fps
  - Maximum resolution: 8192x8192

Display Engine

- Allwinner Awonder1.1 Lite post processing for an excellent display experience
- Supports de-interlace (DI) up to 720p@60fps
- Supports G2D hardware accelerator including rotate and mixer functions

Video Output

- 1 x RGB888 output interface up to 1280x720@60fps
- Single link LVDS interface up to 1366x768@60fps
- 4-lane MIPI DSI interface up to 1280x800@60fps

Audio

- 2x DACs and 1x ADC
- Analog audio interfaces: MICIN, LINEIN, FMIN, HPOUTL/R
- Digital audio interfaces: I2S/PCM, OWA OUT

Peripherals Interfaces

- USB2.0 DRD x 1
- SDIO2.0/3.0
- SPI x 2
- UART x 6
- TWI x 3
- 4-ch PWM x 1
- PWM_BL x 2
- IR_RX x 1
- 1-ch GPADC x 1
- 4-ch TPADC x 1

Security Subsystem

- Integrated 512 bits eFuse storage space

Device Summary

- QFN128, 12.3mm x 12.3mm

Revision History

Revision	Date	Author	Description
0.10	April 28, 2025	AWA1233	Draft Version
0.11	December 2, 2025	AWA1233	**Chapter 4 Electrical characteristics** 1. Update Duty Cycle in section 4.11.1 SMHC Interface Timing 2. Update 4.11.5 SPI Interface Timing 3. Update 4.11.7 SPI Flash Interface Timing

Content

Figures

Tables

About This Document

Purpose and Scope

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package of the F1102MX family. For details about register descriptions of each module, see the *F102MX_User_Manual*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Related Documentation

For a complete listing of related documentation and development-support tools for the device, contact the Allwinner FAE or access the Allwinner Customer Service Platform by visiting https://open.allwinnertech.com/.

Revision Number Definition

Revision 0.10-0.1x

This document is released based on the experimental sample(s). Therefore, it may be modified, calibrated and supplemented hereafter.

All statements, information and recommendations in this document do not constitute any express or implied representation or warranty (including, but not limited to, the warranties of fitness for a particular purpose, merchantability, non-infringement, and accuracy and completeness of the document). Allwinner shall not be liable for any person's use of such information or/and this document.

If you have any questions about the document, please contact us to confirm and obtain the latest version.

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description

Symbol	Description
 CAUTION	A caution means that damage to equipment is possible.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

FT/QA/QC Test

All Allwinner chips provided for clients have passed the following tests.

Test Item	Description
FT Test	FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.
QA Test	QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.
QC Test	QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

1 Overview

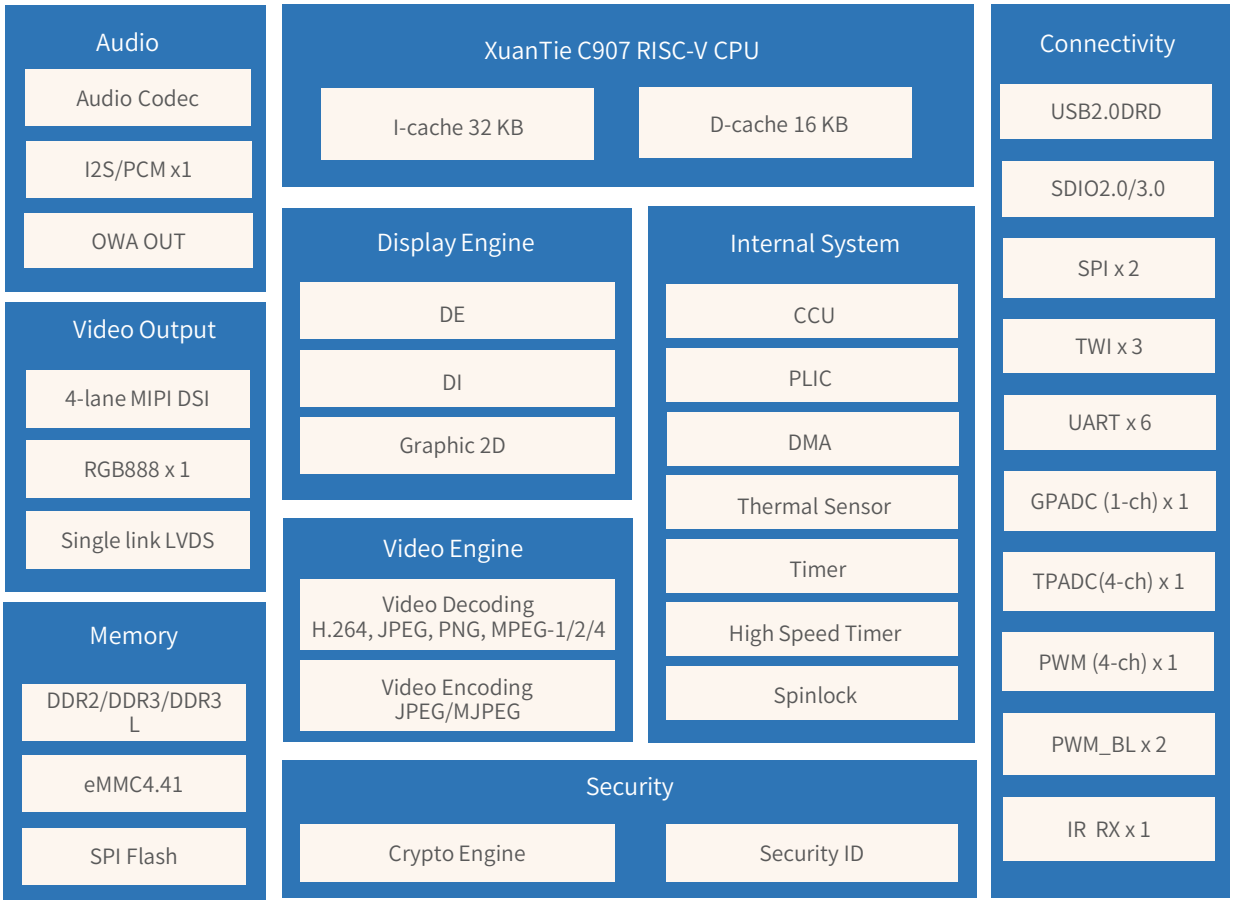
The F102MX is an advanced application processor designed specifically for video decoding market, integrating a domestic RISC-V CPU instruction architecture.

This advanced SoC supports a wide range of decoding formats, including H.264, MPEG-1/2/4, JPEG, PNG, etc. Additionally, its independent hardware encoder can perform encoding in JPEG or MJPEG.

This advanced SoC also supports rich display interfaces such as RGB, LVDS, and MIPI. Integrated multi-channel ADCs/DACs and audio interfaces (I2S/PCM/OWA) provide an excellent voice interaction solution.

The F102MX can be used in network video players, digital photo frames, smart vision transmission screen, and so on.

Figure 1-1 System Block Diagram



2 Features

2.1 Processors

- XuanTie C907 RISC-V CPU
- 32 KB I-cache + 16 KB D-cache

2.2 Memory

2.2.1 Boot ROM (BROM)

- Supports system boot from the following devices:
  - SD Card
  - eMMC
  - SPI NOR Flash (Quad Mode or Single Mode)
  - SPI NAND Flash (Quad Mode or Single Mode)
- Supports mandatory upgrade process through USB
- Supports GPIO pin and eFuse module to select the boot media type

2.2.2 DRAMC

- 8/16-bit DDR2/DDR3/DDR3L interface
- Clock frequency up to 528 MHz for external DDR2/DDR3/DDR3L

2.2.3 SD/MMC Host Controller (SMHC)

- Three SD/MMC Host Controller (SMHC) interfaces
  - SMHC0, compliant with the protocol Secure Digital Memory (up to SD3.0)
  - SMHC2, compliant with the protocol Multimedia Card (up to eMMC4.41)
  - Supports one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 4.41)
- The SMHC0 and SMHC1 supports the following:
  - 1-bit or 4-bit data width
  - Maximum performance:
    - SDR mode 100 MHz@1.8 V IO pad
    - DDR mode 50 MHz@1.8 V IO pad
    - SDR mode 50 MHz@3.3 V IO pad
- Supports block size of 1 to 65535 bytes
- Supports hardware CRC generation and error detection
- Internal 1024-Bytes TX FIFO

- Supports descriptor-based internal DMA controller

2.2.4 SPI Flash Controller (SPIF)

- Supports multiple SPI mode
  - Standard SPI(3-Wire/4-Wire SPI)
  - Dual-Output/Dual-Input SPI/ Dual I/O SPI
  - Quad-Output/Quad-Input SPI/Quad I/O/QPI
  - 3wire SPI with programmable serial data frame length: 1bit to 32bits
- Supports XIP mode of operation for executing code from FLASH memory
- Supports for STR mode and DTR mode, and DTR Supports DQS signal.
- High Speed Clock Frequency
  - 100MHz for STR Mode
  - 100MHz for DTR Mode
- Software Write Protection
  - Write protect all/portion of memory via software
  - Top/Bottom Block protection
- Programmable delays between transactions
- Supports Data Sample Mode: Mode0, Mode1, Mode2 and Mode3
- Support Control signal config
  - Up to four chip selects to support multiple peripherals
  - Polarity and phase of the Chip Select (SPIF_CS) and SPI Clock (SPIF_CLK) are configurable
- Support data scramb/descramb
- Support byte transfer
- Support private DMA，support chain transmission，descriptor length is 8 words

2.3 Graphics Processing

2.3.1 Display Engine (DE)

- One display output, up to 1366x800@60fps
- Supports 2x UI channel and 1x video channel. Each channel supports 4 overlay layer
- Video input format
  - YUV422/YUV420/YUV411
  - ARGB8888/XRGB8888/RGB888/ RGB565/ARGB4444/ ARGB1555
- UI input format: ARGB8888/ARGB8565/RGB888/RGB565/ARGB4444/ARGB1555. UI0 channel supports pallete format
- Supports output RGB@8bit, and dither to 6bit
- Supports gamma and csc
- One Video channel and one UI channel support zooming function

- Supports transparent overlay between VI and UI channels
- Supports updating registers in rcq mode
- Supports simple RGB write-back
- VI layer and UI layer, with a maximum output support of 1366*800
- The Video channel supports input up to 2048*1280

2.3.2 De-interlacer (DI)

- Supports video resolution from 32 x 32 to 2048 x 1280 pixel
- Supports up to 720p@60fps
- Supports Inter-field interpolation/motion adaptive de-interface method
- Supports 8 bit NV12/NV21/YV12/planer YUV422/YUV422UV combine

2.3.3 Graphic 2D (G2D)

- Supports mixer layer size up to 2048 x 2048 pixels, and rotation size up to 4096x4096 pixels
- Supports gradient color fill
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function above
- Supports 1/16x to 32x resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter, 32-phase 4-tap vertical anti-alias filter.
- Supports window clip
- Supports FillRectangle, FillGradient, BitBlt, StretchBlt and MaskBlt
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate
- Supports 4 Thread RCQ function for mixer and rotate
- Supports dither
- Supports ARGB8565 input format

2.4 Video Engine

2.4.1 Video Decoder

2.4.1.1 Video Decoding

- H.264/AVC, BP/MP/HP@Level4.1, up to 1920 x 1080@30fps
- H.263 BP, up to 1280 x 720@30fps

- MPEG-4 SP@L0-3, ASP@L0-5, up to 1920 x 1080@30fps
- MPEG-2 SP@ML, MP@HL, up to 1280 x 720@30fps
- MPEG-1, up to 1280 x 720@30fps

2.4.1.2 Image Decoding

- JPEG decoding
  - Up to 1280 x 720@30fps
  - Maximum decoding resolution: 16384 x 16384
- PNG
  - 1024 x 768 < 100ms
  - Maximum decoding resolution: 2048 x 2048

2.4.2 Video Encoder

- JPEG/MJPEG up to 1280 x 720@30fps
- Maximum resolution is 8192 x 8192

2.5 Video Output Interfaces

2.5.1 MIPI DSI

- Compliant with MIPI DSI specification v1.02 and MIPI D-PHY specification v1.0
- Supports one 4-lane MIPI DSI display, up to 1280 x 800@60fps
- Support up to 4 lanes and lane speed up to 1.0 Gbps per lane in forward direction

2.5.2 LVDS

- Up to 1366x768@60fps for single-link
- Compatible with TIA/EIA 644-A specification
- Compatible with VESA/JEIDA data format

2.5.3 LCD

- One panel interface
  - RGB interface, up to1280x720@60fps
  - Serial/dummy RGB interface, up to 800 x 480@60fps
  - SRGB/I8080 interface, up to 800x480@60fps

2.6 System Peripherals

2.6.1 Clock Controller Unit (CCU)

- Supports clock configuration and clock generation for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.6.2 Power Reset Clock Management (PRCM)

- Module clock configuration
- Bus gating, bus reset, and clock configuration
- RAM configuration control

2.6.3 RTC

- Supports one external 24 MHz DCXO and one internal 24 MHz RC
- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- Multiple general purpose registers for storing power-off information in RTC domain

2.6.4 Thermal Sensor Controller (THS)

- One thermal sensor
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Support ±3°C error limit from 60°C to 125°C, and ±5°C from -40°C to 60°C

2.6.5 LDO Power

- Integrated 1 LDOA
  - LDOA 1.8 V power output
  - LDOA for IO and analog module
- Integrate 1 ALDO, 1.8V power output for AVCC
- Input voltage is 3.6 V to 2.8 V

2.6.6 Timer

Timer0-1

- The counting clock can be configured as LOSC and OSC24M, among which LOSC is the internal low-frequency clock
- Configurable 8 pre-frequency division coefficients
- Programmable 32-bit down timer
- Two working modes: cycle mode and single timing mode
- An interrupt can be generated when the count value drops to 0

Watchdog

- The watchdog is used to transmit a reset signal to reset the entire system when an exception occurs in the system
- Single clock source OSC24M/750
- Supports 12 initial value configurations
- Supports the generation of timeout interrupts
- Supports the generation of reset signals
- Supports watchdog to restart the timer

Audio Video Synchronization (AVS)

- The AVS is used to synchronize the audio and video. The AVS sub-block includes AVS0 and AVS1, which are completely consistent
- Single clock source OSC24M
- Programmable 33-bit additive timer (LSB is 0)
- The initial value can be updated at any time
- 12-bit frequency division factor
- Support the Pause/Start function

2.6.7 High Speed Timer (HSTimer)

- The HSTimer module consists of HSTimer0 and HSTimer1. HSTimer0 and HSTimer1 are down counters that implement timing and counting functions. They are completely consistent.
- Configurable 56-bit down timer
- Supports 5 prescale factors
- The clock source is synchronized with AHB0 clock, much more accurate than other timers
- Supports 2 working modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

2.7 Audio

2.7.1 Audio Codec

- Two audio digital-to-analog(DAC) channel
  - SNR 100dB ±2dB，THD+N -85±3dB
  - Output level≧0.54Vrms, Crosstalk ≦ -75±3dB

  - Supports 16-bit and 20-bit Sample Resolution
  - Supports DAC Sample Rates from 8KHz to 192KHz
- One audio analog-to-digital(ADC) channels
  - SNR 95dB ±3dB，THD+N -80±3dB
  - Input level≧800mFFS@3.2Vpp input
  - Supports 16-bit and 20-bit Sample Resolution
  - Sample Rates from 8KHz to 48KHz
- Audio inputs:
  - One single microphone inputs(MICIN1P)
  - One line-in input (LINEINL)
  - One FM-in input (FMINL)
- One analog audio output:
  - One stereo headphone output (HPOUTL and HPOUTR) .
- Stereo headphone driver
  - 95±3dB SNR@A-weight
  - Output Level 0.54 Vrms@10k Ohm/THD+N -77±3dB，0.37Vrms@16 Ohm/THD+N -40dB
- Support Dynamic Range Controller adjusting the DAC playback and ADC capture
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports DMA and Interrupt

2.7.2 I2S/PCM

- One I2S/PCM external interface for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
  - programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and Receive data FIFOs
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO,64 depth x 32-bit width RXFIFO
- Support multiple function clock
  - clock up to 24.576MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - clock up to 12.288MHz Data Input of I2S/PCM in Master mode
- Support TX/RX DMA Slave interface
- Support Multiple application scenarios
  - up to 16 channel(fs = 48khz) which has adjustable width from 8-bit to 32-bit
  - sample rate from 8KHz to 384KHz(CHAN = 2)
  - 8-bits u-law and 8-bits A-law companded sample

- Support Master/Slave mode

2.7.3 One Wire Audio (OWA)

- One OWA TX
- Compatible with IEC-60958 and IEC-61937
  - IEC-60958 supports data formats: 16 bits, 20 bits, and 24 bits
- Transmit data FIFOs
  - Programmable FIFO thresholds
  - One 128x24bits TXFIFO for audio data transfer
- Supports TX DMA Slave interface
- Supports Multiple function clock
  - Separate OWA TX clock
  - OWA TX function clock includes a series of 24.576MHz and 22.579MHz frequency
- Supports hardware parity On TX
  - Hardware parity generation on the transmitter
- Support channel status insertion for the transmitter

2.8 Peripheral Interfaces

2.8.1 USB2.0 DRD

- One USB2.0 DRD, complies with USB2.0 Specification
- Static host and device mode
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports bi-directional endpoint0 for Control transfer
- Supports up to 10 User-Configurable Endpoints for Bulk, Isochronousl and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)
- Supports up to (8KB+64Bytes) FIFO for EPs (Including EP0)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Includes interface to an external Normal DMA controller for every EPs
- Device and Host controller share a 8KB SRAM and a physical PHY

- Supports BC1.2 protocal(only as CDP Host)

2.8.2 PWM

- Up to 4 PWM channels
  - Supports PWM continuous mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range:
    - 0 to 24 MHz (when the clock source is DCXO)
    - 0 to 100 MHz (when the clock source is APB1 clock)
  - Various duty-cycle: 0% -100%
  - Minimum resolution: 1/65536
- Maximum 2 complementary pairs output
  - PWM01 pair (PWM-0 + PWM-1), PWM23 pair (PWM-2 + PWM-3)
  - Supports dead-zone generator, and the dead-zone time is configurable
- Maximum 2 group of PWM channel output for controlling stepping motors
  - Supports any plural channels to form a group, and output the same duty-cycle pulse
  - In group mode, the relative phase of the output waveform for each channel is configurable
- Maximum 4 channels capture input
  - Supports rising edge detection and falling edge detection for input waveform pulse
  - Supports pulse-width measurement for input waveform pulse

2.8.3 PWM_BL

- Supports two PWM_BL outputs: PWM_BL0 is the digital circuit output BOOST_PWM0, and PWM_BL1 is the digital circuit or pure analog circuit output BOOST_PWM1.
- Supports backlight BOOST control and adjusts the output duty cycle of PWM_BL by detecting the level of feedback voltage.

2.8.4 UART

- Up to 6 UART controllers (UART0, UART1, UART2, UART3, UART4, UART5)
- Compatible with industry-standard 16450/16550 UARTs
- Transmit and Receive data FIFOs
  - UART0(RX-64Layer, TX-64Layer)
  - UART1-5(RX-128Layer, TX-128Layer)
- Supports baud rate generator from APB bus clock
  - Speed up to 1.5Mbps with 24MHz APB clock
  - Speed up to 3.75Mbps with 60MHz APB clock
  - Speed up to 5Mbps with 80MHz APB clock
  - Speed up to 4Mbps with 64MHz APB clock

- Supports 5-8 data bits and 1/1.5/2 stop bits
- Supports Even, Odd or No Parity
- Supports TX/RX DMA Slave interface
- Supports Software/ Hardware Flow Control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode
- Supports RS-485 full duplex mode
- Supports Auto-Flow by using CTS & RTS(exclude UART0)

2.8.5 SPI

- Up to 2 SPI controllers
  - SPI0, supporting SPI mode
  - SPI1, supporting SPI mode and display bus interface (DBI) mode

SPI mode

- Supports Interrupt or DMA
- Supports Mode0, Mode1, Mode2 and Mode3
- Supports the Maximum clock frequency: 100MHz
- Supports 3-Wire/4-Wire SPI, with programmable serial data frame length of 1 bit to 32 bits
- Supports programmable serial data frame length: 0bit to 32bits
- Supports Standard SPI/Dual-Output/Dual-Input SPI/ Dual I/O SPI and Quad-Output/Quad-Input SPI

DBI mode

- Supports DBI Type C 3 Line/4 Line Interface Mode
- Supports 2 Data Lane Interface Mode
- Supports RGB111/444/565/666/888 video format
- Supports maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Supports maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Supports tearing effect
- Supports software flexible control video frame rate

2.8.6 Two Wire Interface (TWI)

- Supports up to 3 TWI controllers (TWI0, TWI1, TWI2)
- Supports Master mode and Slave mode
- Standard mode (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s)
- Supports multi-master devices

2.8.7 General Purpose ADC (GPADC)

- One 1-ch ADC
- 12-bit sampling resolution
- Maximum sampling frequency up to 1 MHz
- Supports two operation modes: single conversion mode, and continuous conversion mode
- Analog input range: 0 to 1.8 V

2.8.8 Touch Panel ADC(TPADC)

- 12 bit SAR type A/D converter
- 4-wire resistive touch panel input detection
  - Single touch detect
  - Dual touch detect
  - Pen down detection, with programmable sensitivity
  - Touch-pressure measurement (Support programmable threshold)
  - X/Y coordinate exchange
- Sampling frequency: 750 kHz (max)
- Analog input range: 0 to 1.8V

2.8.9 Consumer Infrared Receiver (IR_RX)

- One IR_RX interface
- NEC format infra data
- RLC encoding
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.9 Security

2.9.1 Crypto Engine (CE)

- Supports Symmetrical algorithm for encryption and decryption: AES, DES, 3DES, MD5, PRNG, SHA-1, CRC32/16, SHA256
- Supports ECB, CBC, CTR mode for AES/DES/3DES
- Supports CTS for AES
- Supports 128/192/256-bit key for AES
- Supports 160-bit hardware PRNG with 192-bit seed
- Supports RX FIFO, up to 32x32
- Supports TX FIFO, up to32x32
- Supports AHB interface and CPU access
- Supports DMA interface and external DMA access

2.9.2 Security ID (SID)

- 512-bit eFuse
- One-time programming

2.10 Package

QFN 128 pins, 12.3 mm x 12.3 mm body size, 0.85 mm height (maximum)

3 Pin Description

3.1 Pin Characteristics

This section lists the characteristics of the device pins from the following seven aspects.

[1] **Pin#**: Package pin numbers associated with each signal.

[2] **Pin Name**: The name of the package pin.

NC means these pins are not connected.

[3] **Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

N/A (Not Applicable)

[4] **Ball Reset State**: The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] **Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pullup

PD: Internal pulldown

PU/PD: Internal pullup and pulldown

N/A: Not Applicable

[6] **Default Buffer Strength**: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

N/A means Not Applicable.

[7] I/O Power Supply: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

3.1.1 SDRAM

Table 3-1 SDRAM Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
47	SDQ0	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
46	SDQ1	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
45	SDQ2	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
44	SDQ3	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
40	SDQ4	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
39	SDQ5	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
38	SDQ6	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
37	SDQ7	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
59	SDQ8	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
58	SDQ9	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
57	SDQ10	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
56	SDQ11	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
52	SDQ12	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
51	SDQ13	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
50	SDQ14	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
49	SDQ15	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
41	SDQS0P	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
53	SDQS1P	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
42	SDQS0N	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
54	SDQS1N	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
43	SDQM0	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
55	SDQM1	I/O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
74	SCKP	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
73	SCKN	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
63	SCKE0	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
68	SA0	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
70	SA1	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
75	SA2	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
69	SA3	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
80	SA4	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
76	SA5	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
67	SA6	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
84	SA7	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
64	SA8	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
65	SA9	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
72	SA10	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
61	SA11	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
62	SA12	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
85	SA13	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
66	SWE	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
71	SCAS	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
79	SRAS	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
86	SCS0	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
78	SBA0	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
83	SBA1	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
82	SBA2	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
87	SODT0	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
81	SRST	O	N/A	N/A	N/A	VCC-DRAM0/VCC-DRAM1
48	VCC-DRAM0	P	N/A	N/A	N/A	N/A
77	VCC-DRAM1	P	N/A	N/A	N/A	N/A

3.1.2 GPIO Groups

3.1.2.1 Port A

Table 3-2 Port A Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
105	PA0	A I/O	Z	PU/PD	4 mA	AVCC
103	PA1	A I/O	Z	PU/PD	4 mA	AVCC
106	PA2	A I/O	Z	PU/PD	4 mA	AVCC
104	PA3	A I/O	Z	PU/PD	4 mA	AVCC

3.1.2.2 Port B

Table 3-3 Port B Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
127	PB0	I/O	Z	PU/PD	4 mA	VCC33-PB-USB
126	PB1	I/O	Z	PU/PD	4 mA	VCC33-PB-USB
125	PB2	I/O	Z	PU/PD	4 mA	VCC33-PB-USB
124	PB3	I/O	Z	PU/PD	4 mA	VCC33-PB-USB

3.1.2.3 Port C

Table 3-4 Port C Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
94	PC0	I/O	Z	PU/PD	4 mA	VCC33-PC-PF
93	PC1	I/O	PU	PU/PD	4 mA	VCC33-PC-PF
92	PC2	I/O	PU	PU/PD	4 mA	VCC33-PC-PF
91	PC3	I/O	Z	PU/PD	4 mA	VCC33-PC-PF
90	PC4	I/O	PU	PU/PD	4 mA	VCC33-PC-PF
89	PC5	I/O	Z	PU/PD	4 mA	VCC33-PC-PF

3.1.2.4 Port D

Table 3-5 Port D Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
3	PD0	I/O	Z	PU/PD	4 mA	VCC-PE-PD
4	PD1	I/O	Z	PU/PD	4 mA	VCC-PE-PD
5	PD2	I/O	Z	PU/PD	4 mA	VCC-PE-PD
6	PD3	I/O	Z	PU/PD	4 mA	VCC-PE-PD
7	PD4	I/O	Z	PU/PD	4 mA	VCC-PE-PD
8	PD5	I/O	Z	PU/PD	4 mA	VCC-PE-PD
9	PD6	I/O	Z	PU/PD	4 mA	VCC-PE-PD
10	PD7	I/O	Z	PU/PD	4 mA	VCC-PE-PD
11	PD8	I/O	Z	PU/PD	4 mA	VCC-PE-PD
12	PD9	I/O	Z	PU/PD	4 mA	VCC-PE-PD
13	PD10	I/O	Z	PU/PD	4 mA	VCC-PE-PD
14	PD11	I/O	Z	PU/PD	4 mA	VCC-PE-PD
15	PD12	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
16	PD13	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
17	PD14	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
18	PD15	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
19	PD16	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
20	PD17	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
23	PD18	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
24	PD19	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
25	PD20	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
26	PD21	I/O	Z	PU/PD	4 mA	VCC-PE-PD/VCC18-LVDS
2	PD22	I/O	Z	PU/PD	4 mA	VCC-PE-PD
21	VCC18-LVDS	P	N/A	N/A	N/A	N/A
22	VCC-PE-PD	P	N/A	N/A	N/A	N/A

3.1.2.5 Port E

Table 3-6 Port E Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
28	PE0	I/O	Z	PU/PD	4 mA	VCC-PE-PD
27	PE1	I/O	Z	PU/PD	4 mA	VCC-PE-PD
30	PE2	I/O	Z	PU/PD	4 mA	VCC-PE-PD
29	PE3	I/O	Z	PU/PD	4 mA	VCC-PE-PD
32	PE4	I/O	Z	PU/PD	4 mA	VCC-PE-PD
31	PE5	I/O	Z	PU/PD	4 mA	VCC-PE-PD
33	PE6	I/O	Z	PU/PD	4 mA	VCC-PE-PD
34	PE7	I/O	Z	PU/PD	4 mA	VCC-PE-PD
35	PE8	I/O	Z	PU/PD	4 mA	VCC-PE-PD
36	PE9	I/O	Z	PU/PD	4 mA	VCC-PE-PD

3.1.2.6 Port F

Table 3-7 Port F Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
97	PF0	I/O	Z	PU/PD	4 mA	VCC33-PC-PF/VCC18-PLL-HPVCC
98	PF1	I/O	Z	PU/PD	4 mA	VCC33-PC-PF/VCC18-PLL-HPVCC
99	PF2	I/O	Z	PU/PD	4 mA	VCC33-PC-PF/VCC18-PLL-HPVCC
100	PF3	I/O	Z	PU/PD	4 mA	VCC33-PC-PF/VCC18-PLL-HPVCC
101	PF4	I/O	Z	PU/PD	4 mA	VCC33-PC-PF/VCC18-PLL-HPVCC
102	PF5	I/O	Z	PU/PD	4 mA	VCC33-PC-PF/VCC18-PLL-HPVCC
96	PF6	I/O	Z	PU/PD	4 mA	VCC33-PC-PF/VCC18-PLL-HPVCC
95	VCC33-PC-PF	P	N/A	N/A	N/A	N/A

3.1.3 USB

Table 3-8 USB Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
120	USB-DM	A I/O	N/A	N/A	N/A	VCC33-PB-USB
121	USB-DP	A I/O	N/A	N/A	N/A	VCC33-PB-USB

3.1.4 GPADC

Table 3-9 GPADC Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
107	GPADC	AI	N/A	N/A	N/A	AVCC

3.1.5 Audio Codec

Table 3-10 Audio Codec Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
115	HPOUTL	AO	N/A	N/A	N/A	VCC18-PLL-HPVCC
117	HPOUTR	AO	N/A	N/A	N/A	VCC18-PLL-HPVCC
116	HPOUTFB	AI	N/A	N/A	N/A	VCC18-PLL-HPVCC
114	VCC18-PLL-HPVCC	P	N/A	N/A	N/A	N/A
108	FMIN	AI	N/A	N/A	N/A	AVCC
109	LINEIN	AI	N/A	N/A	N/A	AVCC
110	MICIN	AI	N/A	N/A	N/A	AVCC
112	VRA	AO	N/A	N/A	N/A	N/A
113	AVCC	P	N/A	N/A	N/A	N/A
111	AGND	G	N/A	N/A	N/A	N/A

3.1.6 DCXO

Table 3-11 DCXO Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
118	DXIN	AI	N/A	N/A	N/A	VCC18-PLL-HPVCC
119	DXOUT	AO	N/A	N/A	N/A	VCC18-PLL-HPVCC

3.1.7 RESET

Table 3-12 RESET# Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
128	RESET	OD	N/A	N/A	N/A	VCC33-PB-USB

3.1.8 Power

Table 3-13 Power Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
123	VCC18-EFUSE-LDOA	P	N/A	N/A	N/A	N/A
122	VCC33-PB-USB	P	N/A	N/A	N/A	N/A
1	VDD-CORE0	P	N/A	N/A	N/A	N/A
60	VDD-CORE1	P	N/A	N/A	N/A	N/A
88	VDD-CORE2	P	N/A	N/A	N/A	N/A

3.2 GPIO Multiplex Function

The following tables provide a description of the GPIO multiplex function.

NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function11 to Function13 are reserved.

3.2.1 Port A

Table 3-14 Port A Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PA0	AI/O	TP-X1	PWM0-0								PA-EINT0
PA1	AI/O	TP-X2	PWM0-1								PA-EINT1
PA2	AI/O	TP-Y1	PWM0-2								PA-EINT2
PA3	AI/O	TP-Y2	PWM0-3								PA-EINT3

3.2.2 Port B

Table 3-15 Port B Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PB0	I/O	BOOST1-PWM	TWI1-SCK	UART1-TX	UART2-RTS		PWM0-0	SPIF0-CS1			PB-EINT0
PB1	I/O	BOOST1-FB	TWI1-SDA	UART1-RX	UART2-CTS		PWM0-1	IR-RX			PB-EINT1
PB2	I/O	BOOST0-PWM	TWI2-SCK	UART1-RTS	UART2-TX		PWM0-2	SPI0-CS1			PB-EINT2
PB3	I/O	BOOST0-FB	TWI2-SDA	UART1-CTS	UART2-RX		PWM0-3	IR-RX			PB-EINT3

3.2.3 Port C

Table 3-16 Port C Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PC0	I/O	SDC2-CLK	SPI0-CLK	SPIF0-CLK							PC-EINT0
PC1	I/O	SDC2-CMD	SPI0-CS0	SPIF0-CS0							PC-EINT1
PC2	I/O	SDC2-D2	SPI0-MISO	SPIF0-MISO	BOOT-SEL0	UART3-RTS					PC-EINT2

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PC3	I/O	SDC2-D1	SPI0-WP	SPIF0-WP	TWI1-SCK	UART3-TX	PWM0-0				PC-EINT3
PC4	I/O	SDC2-D0	SPI0-MOSI	SPIF0-MOSI	BOOT-SEL1	UART3-CTS					PC-EINT4
PC5	I/O	SDC2-D3	SPI0-HOLD	SPIF0-HOLD	TWI1-SDA	UART3-RX	PWM0-1				PC-EINT5

3.2.4 Port D

Table 3-17 Port D Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PD0	I/O	LCD0-D2	SPI1-CS0/DBI-CSX	TWI1-SCK	UART3-TX	TWI0-SCK	RJTAG-MS				PD-EINT0
PD1	I/O	LCD0-D3	SPI1-CLK/DBI-SCLK	TWI1-SDA	UART3-RX	PWM0-0	RJTAG-DI				PD-EINT1
PD2	I/O	LCD0-D4	SPI1-MOSI/DBI-SDO	UART2-TX	TWI0-SDA	UART1-TX	RJTAG-DO				PD-EINT2
PD3	I/O	LCD0-D5	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	UART2-RX	UART3-RTS	UART1-RX	RJTAG-CK				PD-EINT3
PD4	I/O	LCD0-D6	SPI1-HOLD/DBI-DCX/DBI-WRX	UART2-RTS	UART3-CTS	TWI0-SCK					PD-EINT4
PD5	I/O	LCD0-D7	SPI1-WP/DBI-TE	UART2-CTS	IR-RX	TWI0-SDA					PD-EINT5
PD6	I/O	LCD0-D10	SPI1-CS1	I2S0-MCLK	UART4-TX	PWM0-0					PD-EINT6
PD7	I/O	LCD0-D11	IR-RX	I2S0-BCLK	UART4-RX	PWM0-1					PD-EINT7
PD8	I/O	LCD0-D12	TWI1-SCK	I2S0-LRCK	UART4-RTS	PWM0-2					PD-EINT8
PD9	I/O	LCD0-D13	TWI1-SDA	I2S0-DOUT0	UART4-CTS	PWM0-3	LCD0-VSYNC				PD-EINT9
PD	I/	LCD0-	TWI2-SCK	I2S0-D	UART	UART	PWM0				PD-EI

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
10	O	D14		IN0	1-TX	5-TX	-3				NT10
PD 11	I/O	LCD0-D15	TWI2-SDA	OWA-OUT	UART 1-RX	UART 5-RX					PD-EINT11
PD 12	I/O	LCD0-D18	LVDS0-D0P	DSI-D0P	UART 3-RX	TWI0-SDA					PD-EINT12
PD 13	I/O	LCD0-D19	LVDS0-D0N	DSI-D0N	UART 2-TX						PD-EINT13
PD 14	I/O	LCD0-D20	LVDS0-D1P	DSI-D1P	UART 2-RX						PD-EINT14
PD 15	I/O	LCD0-D21	LVDS0-D1N	DSI-D1N	UART 2-RTS						PD-EINT15
PD 16	I/O	LCD0-D22	LVDS0-D2P	DSI-CKP	UART 2-CTS						PD-EINT16
PD 17	I/O	LCD0-D23	LVDS0-D2N	DSI-CKN	UART 5-TX						PD-EINT17
PD 18	I/O	LCD0-CLK	LVDS0-CKP	DSI-D2P	UART 5-RX						PD-EINT18
PD 19	I/O	LCD0-HSYNC	LVDS0-CKN	DSI-D2N	UART 5-RTS	UART 4-TX					PD-EINT19
PD 20	I/O	LCD0-VSYNC	LVDS0-D3P	DSI-D3P	UART 5-CTS	UART 4-RX					PD-EINT20
PD 21	I/O	LCD0-DE	LVDS0-D3N	DSI-D3N	UART 1-TX	UART 4-RTS					PD-EINT21
PD 22	I/O	OWA-OUT	IR-RX	PWM0-2	UART 1-RX	UART 4-CTS					PD-EINT22

3.2.5 Port E

Table 3-18 Port E Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PE0	I/O		LCD0-D0	TWI1-SCK	I2S0-MCLK	UART0-TX		SPI1-CS0/DBI-CSX	SDC2-D1	CLK-FANOUT0	PE-EINT0
PE1	I/O		LCD0-D1	TWI1-SDA	I2S0-BCLK	UART0-RX		SPI1-CLK/DBI-SCLK	SDC2-D0		PE-EINT1
PE2	I/O		LCD0-D8	TWI0-SCK	I2S0-LRCK	UART4-TX		SPI1-MOSI/DBI-SDO	SDC2-CLK	PWM0-0	PE-EINT2
PE3	I/O		LCD0-D9	TWI0-SDA	I2S0-DOUT0	UART4-RX		SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	SDC2-CMD	PWM0-1	PE-EINT3
PE4	I/O		LCD0-D16	TWI2-SCK	I2S0-DIN0	UART4-RTS	UART5-TX	SPI1-HOLD/DBI-DCX/DBI-WRX	SDC2-D3	PWM0-2	PE-EINT4
PE5	I/O		LCD0-D17	TWI2-SDA	IR-RX	UART4-CTS	UART5-RX	SPI1-WP/DBI-TE	SDC2-D2	PWM0-3	PE-EINT5
PE6	I/O		UART2-TX	LCD0-D14		OWA-OUT	IR-RX	SPI1-CS1			PE-EINT6
PE7	I/O		UART2-RX	LCD0-D15					CLK-FANOUT1		PE-EINT7
PE8	I/O		UART2-RTS	TWI0-SCK		UART3-TX	PWM0-0		CLK-FANOUT2		PE-EINT8
PE9	I/O		UART2-CTS	TWI0-SDA		UART3-RX	PWM0-1				PE-EINT9

3.2.6 Port F

Table 3-19 Port F Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PF0	I/O	SDC0-D1	DJTAG-MS	RJTAG-MS	PWM0-0	UART1-CTS					PF-EINT0
PF1	I/O	SDC0-D0	DJTAG-DI	RJTAG-DI	PWM0-1						PF-EINT1

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PF2	I/O	SDC0-CLK	UART0-TX	TWI0-SCK							PF-EINT2
PF3	I/O	SDC0-CMD	DJTAG-DO	RJTAG-DO	TWI1-SCK						PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX	TWI0-SDA		UART1-TX	TWI2-SCK				PF-EINT4
PF5	I/O	SDC0-D2	DJTAG-CK	RJTAG-CK	TWI1-SDA	UART1-RX	TWI2-SDA				PF-EINT5
PF6	I/O	PWM0-3	IR-RX	SPI0-CS1	SPIF0-CS1	UART1-RTS					PF-EINT6

3.3 Detailed Signal Description

The following tables show the detailed function description of every signal based on the different interfaces.

[1] Signal Name: The name of every signal.

[2] Description: The detailed function description of every signal.

[3] Type: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

3.3.1 SDRAM

Table 3-20 SDRAM Signal Description

Signal Name[1]	Description[2]	Type[3]
SRST	DRAM Reset Signal	O

Signal Name[1]	Description[2]	Type[3]
SWE	DRAM Write Enable	O
SA0	DRAM Address Signal 0	O
SA1	DRAM Address Signal 1	O
SA2	DRAM Address Signal 2	O
SA3	DRAM Address Signal 3	O
SA4	DRAM Address Signal 4	O
SA5	DRAM Address Signal 5	O
SA6	DRAM Address Signal 6	O
SA7	DRAM Address Signal 7	O
SA8	DRAM Address Signal 8	O
SA9	DRAM Address Signal 9	O
SA10	DRAM Address Signal 10	O
SA11	DRAM Address Signal 11	O
SA12	DRAM Address Signal 12	O
SA13	DRAM Address Signal 13	O
SBA0	DRAM Bank Address Signal 0	O
SBA1	DRAM Bank Address Signal 1	O
SBA2	DRAM Bank Address Signal 2	O
SRAS	DRAM Row Address Strobe	O
SCAS	DRAM Column Address Strobe	O
SCKE0	DRAM Clock Enable Signal to the Memory Device 0	O
SCKN	DRAM Differential Clock (Negative)	O
SCKP	DRAM Differential Clock (Positive)	O
SCS0	DRAM Chip Select Signal to the Memory Device for RANK 0	O
SDQ0	DRAM Bidirectional Data Line 0	I/O
SDQ1	DRAM Bidirectional Data Line 1	I/O
SDQ2	DRAM Bidirectional Data Line 2	I/O
SDQ3	DRAM Bidirectional Data Line 3	I/O
SDQ4	DRAM Bidirectional Data Line 4	I/O
SDQ5	DRAM Bidirectional Data Line 5	I/O

Signal Name[1]	Description[2]	Type[3]
SDQ6	DRAM Bidirectional Data Line 6	I/O
SDQ7	DRAM Bidirectional Data Line 7	I/O
SDQ8	DRAM Bidirectional Data Line 8	I/O
SDQ9	DRAM Bidirectional Data Line 9	I/O
SDQ10	DRAM Bidirectional Data Line 10	I/O
SDQ11	DRAM Bidirectional Data Line 11	I/O
SDQ12	DRAM Bidirectional Data Line 12	I/O
SDQ13	DRAM Bidirectional Data Line 13	I/O
SDQ14	DRAM Bidirectional Data Line 14	I/O
SDQ15	DRAM Bidirectional Data Line 15	I/O
SDQM0	DRAM Data Mask Signal 0	I/O
SDQM1	DRAM Data Mask Signal 1	I/O
SDQS0N	DRAM Bidirectional Data Strobe 0 (Active Low)	I/O
SDQS0P	DRAM Bidirectional Data Strobe 0 (Active High)	I/O
SDQS1N	DRAM Bidirectional Data Strobe 1 (Active Low)	I/O
SDQS1P	DRAM Bidirectional Data Strobe 1 (Active High)	I/O
SODT0	DRAM On-Die Termination Output Signal 0	O
VCC-DRAM0	IO Power Supply for DRAM0 PHY	P
VCC-DRAM1	IO Power Supply for DRAM1 PHY	P

3.3.2 System Control

Table 3-21 System Control Signal Description

Signal Name[1]	Description[2]	Type[3]
RESET	SoC Reset Signal (Active Low)	OD
BOOT-SEL0	Boot Media Select 0	I
BOOT-SEL1	Boot Media Select 1	I

3.3.3 DCXO

Table 3-22 DCXO Signal Description

Signal Name[1]	Description[2]	Type[3]
DXIN	Digital Compensated Crystal Oscillator Input	AI

Signal Name[1]	Description[2]	Type[3]
DXOUT	Digital Compensated Crystal Oscillator Output	AO

3.3.4 Clock Fanout

Table 3-23 Clock Fanout Signal Description

Signal Name[1]	Description[2]	Type[3]
CLK-FANOUT0	Internal Clock Fanout 0 Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, and so on	O
CLK-FANOUT1	Internal Clock Fanout 1 Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, and so on	O
CLK-FANOUT2	Internal Clock Fanout 2 Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, and so on	O

3.3.5 SD Card/eMMC

Table 3-24 SD Card/eMMC Signal Description

Signal Name[1]	Description[2]	Type[3]
SDC0-CMD	SD Card Command Output/Response Input	I/O, OD
SDC0-CLK	SD Card Clock Output	O
SDC0-D0	SD Card Data Input/ Output 0	I/O
SDC0-D1	SD Card Data Input/ Output 1	I/O
SDC0-D2	SD Card Data Input/ Output 2	I/O
SDC0-D3	SD Card Data Input/ Output 3	I/O
SDC2-CMD	eMMC Command Output/Response Input	I/O, OD
SDC2-CLK	eMMC Clock Output	O
SDC2-D0	eMMC Data Input/ Output 0	I/O
SDC2-D1	eMMC Data Input/ Output 1	I/O
SDC2-D2	eMMC Data Input/ Output 2	I/O
SDC2-D3	eMMC Data Input/ Output 3	I/O

3.3.6 USB

Table 3-25 USB Signal Description

Signal Name[1]	Description[2]	Type[3]
USB-DM	USB Differential Data (Negative)	A I/O
USB-DP	USB Differential Data (Positive)	A I/O

3.3.7 Audio Codec

Table 3-26 Audio Codec Signal Description

Signal Name[1]	Description[2]	Type[3]
HPOUTL	Headphone Left Output	AO
HPOUTR	Headphone Right Output	AO
HPOUTFB	Pseudo Differential Headphone Ground Reference	AI
FMIN	FMIN Left Input	AI
LINEIN	LINEIN Left Single-End Input	AI
MICIN	Microphone Differential Positive Input	AI
VRA	Internal Reference Voltage	AO
VCC18-PLL-HPVCC	Headphone Power	P
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G

3.3.8 I2S/PCM

Table 3-27 I2S/PCM Signal Description

Signal Name[1]	Description[2]	Type[3]
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O
I2S0-DIN0	I2S0/PCM0 Serial Data Input 0	I
I2S0-DOUT0	I2S0/PCM0 Serial Data Output 0	O

3.3.9 OWA

Table 3-28 OWA Signal Description

Signal Name[1]	Description[2]	Type[3]

Signal Name[1]	Description[2]	Type[3]
OWA-OUT	One Wire Audio Output	O

3.3.10 SPI&SPI_DBI

Table 3-29 SPI&SPI_DBI Signal Description

Signal Name[1]	Description[2]	Type[3]
SPI0-CS0	SPI0 Chip Select 0 (Active Low)	I/O
SPI0-CS1	SPI0 Chip Select 1 (Active Low)	I/O
SPI0-CLK	SPI0 Clock	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI0-HOLD	SPI0 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-CS0	SPI1 Chip Select 0 (Active Low)	I/O
SPI1-CS1	SPI1 Chip Select 1 (Active Low)	I/O
SPI1-CLK	SPI1 Clock	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-HOLD	SPI1 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
DBI-CSX	Chip Select Signal (Active Low)	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge.	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command.	I/O

Signal Name[1]	Description[2]	Type[3]
	DCX = 0: register command; DCX = 1: data or parameter.	
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O

3.3.11 SPI_Flash

Table 3-30 SPI_Flash Signal Description

Signal Name[1]	Description[2]	Type[3]
SPIF0-CS0	SPIF0 Peripheral Chip Select Signal 0, Low Active	O
SPIF0-CS1	SPIF0 Peripheral Chip Select Signal 1, Low Active	O
SPIF0-CLK	SPIF0 Master Mode Clock Output	O
SPIF0-MOSI	SPIF0 Master Data Out, Slave Data In	I/O
SPIF0-MISO	SPIF0Master Data In, Slave Data Out	I/O
SPIF0-WP	SPIF0 Write Protection (Active Low)	I/O
SPIF0-HOLD	SPIF0Hold Signal	I/O

3.3.12 LCD

Table 3-31 LCD Signal Description

Signal Name[1]	Description[2]	Type[3]
LCD0-CLK	LCD0 Clock	O
LCD0-VSYNC	LCD0 Vertical Synchronization	O
LCD0-HSYNC	LCD0 Horizontal Synchronization	O
LCD0-DE	LCD0 Data Enable	O
LCD0-D0	LCD0 Data Input/Output 0	I/O
LCD0-D1	LCD0 Data Input/Output 1	I/O
LCD0-D2	LCD0 Data Input/Output 2	I/O
LCD0-D3	LCD0 Data Input/Output 3	I/O
LCD0-D4	LCD0 Data Input/Output 4	I/O
LCD0-D5	LCD0 Data Input/Output 5	I/O
LCD0-D6	LCD0 Data Input/Output 6	I/O
LCD0-D7	LCD0 Data Input/Output 7	I/O

Signal Name[1]	Description[2]	Type[3]
LCD0-D8	LCD0 Data Input/Output 8	I/O
LCD0-D9	LCD0 Data Input/Output 9	I/O
LCD0-D10	LCD0 Data Input/Output 10	I/O
LCD0-D11	LCD0 Data Input/Output 11	I/O
LCD0-D12	LCD0 Data Input/Output 12	I/O
LCD0-D13	LCD0 Data Input/Output 13	I/O
LCD0-D14	LCD0 Data Input/Output 14	I/O
LCD0-D15	LCD0 Data Input/Output 15	I/O
LCD0-D16	LCD0 Data Input/Output 16	I/O
LCD0-D17	LCD0 Data Input/Output 17	I/O
LCD0-D18	LCD0 Data Input/Output 18	I/O
LCD0-D19	LCD0 Data Input/Output 19	I/O
LCD0-D20	LCD0 Data Input/Output 20	I/O
LCD0-D21	LCD0 Data Input/Output 21	I/O
LCD0-D22	LCD0 Data Input/Output 22	I/O
LCD0-D23	LCD0 Data Input/Output 23	I/O

3.3.13 LVDS

Table 3-32 LVDS Signal Description

Signal Name[1]	Description[2]	Type[3]
LVDS0-CKP	LVDS0 Differential Clock (Positive)	AO
LVDS0-CKN	LVDS0 Differential Clock (Negative)	AO
LVDS0-D0P	LVDS0 Differential Data 0 (Positive)	AO
LVDS0-D0N	LVDS0 Differential Data 0 (Negative)	AO
LVDS0-D1P	LVDS0 Differential Data 1 (Positive)	AO
LVDS0-D1N	LVDS0 Differential Data 1 (Negative)	AO
LVDS0-D2P	LVDS0 Differential Data 2 (Positive)	AO
LVDS0-D2N	LVDS0 Differential Data 2 (Negative)	AO
LVDS0-D3P	LVDS0 Differential Data 3 (Positive)	AO
LVDS0-D3N	LVDS0 Differential Data 3 (Negative)	AO
VCC18-LVDS	LVDS and DSI Combo PHY Power Supply	P

3.3.14 MIPI DSI

Table 3-33 MIPI DSI Signal Description

Signal Name[1]	Description[2]	Type[3]
DSI-CKP	DSI Differential Clock (Positive)	AO
DSI-CKN	DSI Differential Clock (Negative)	AO
DSI-D0P	DSI Differential Data Line 0 (Positive)	A I/O
DSI-D0N	DSI Differential Data Line 0 (Negative)	A I/O
DSI-D1P	DSI Differential Data Line (Positive)	AO
DSI-D1N	DSI Differential Data Line (Negative)	AO
DSI-D2P	DSI Differential Data Line (Positive)	AO
DSI-D2N	DSI Differential Data Line (Negative)	AO
DSI-D3P	DSI Differential Data Line (Positive)	AO
DSI-D3N	DSI Differential Data Line (Negative)	AO

3.3.15 UART

Table 3-34 UART Signal Description

Signal Name[1]	Description[2]	Type[3]
UART0-RX	UART0 Data Receiver	I
UART0-TX	UART0 Data Transmitter	O
UART1-RX	UART1 Data Receiver	I
UART1-TX	UART1 Data Transmitter	O
UART1-CTS	UART1 Clear to Send	I
UART1-RTS	UART1 Request to Send	O
UART2-RX	UART2 Data Receiver	I
UART2-TX	UART2 Data Transmitter	O
UART2-CTS	UART2 Clear to Send	I
UART2-RTS	UART2 Request to Send	O
UART3-RX	UART3 Data Receiver	I
UART3-TX	UART3 Data Transmitter	O
UART3-CTS	UART3 Clear to Send	I
UART3-RTS	UART3 Request to Send	O

Signal Name[1]	Description[2]	Type[3]
UART4-RX	UART4 Data Receiver	I
UART4-TX	UART4 Data Transmitter	O
UART4-CTS	UART4 Clear to Send	I
UART4-RTS	UART4 Request to Send	O
UART5-RX	UART5 Data Receiver	I
UART5-TX	UART5 Data Transmitter	O
UART5-CTS	UART5 Clear to Send	I
UART5-RTS	UART5 Request to Send	O

3.3.16 TWI

Table 3-35 TWI Signal Description

Signal Name[1]	Description[2]	Type[3]
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O

3.3.17 PWM

Table 3-36 PWM Signal Description

Signal Name[1]	Description[2]	Type[3]
PWM0-0	PWM0 Wave Output /Capture Wave Input 0	I/O
PWM0-1	PWM0 Wave Output /Capture Wave Input 1	I/O
PWM0-2	PWM0 Wave Output /Capture Wave Input 2	I/O
PWM0-3	PWM0 Wave Output /Capture Wave Input 3	I/O

3.3.18 IR_RX

Table 3-37 IR_RX Signal Description

Signal Name[1]	Description[2]	Type[3]
IR-RX	Consumer Infrared Receiver	I

3.3.19 TPADC

Table 3-38 TPADC Signal Description

Signal Name[1]	Description[2]	Type[3]
TP-X1	Touch Panel X1 Input	AI
TP-X2	Touch Panel X2 Input	AI
TP-Y1	Touch Panel Y1 Input	AI
TP-Y2	Touch Panel Y2 Input	AI

3.3.20 JTAG

Table 3-39 JTAG Signal Description

Signal Name[1]	Description[2]	Type[3]
RJTAG-MS	RISC-V JTAG Mode Selection	I
RJTAG-CK	RISC-VJTAG Clock Signal	I
RJTAG-DI	RISC-V JTAG Data Input	I
RJTAG-DO	RISC-V JTAG Data Output	O
DJTAG-MS	DAP JTAG Mode Selection	I
DJTAG-CK	DAPJTAG Clock Signal	I
DJTAG-DI	DAP JTAG Data Input	I
DJTAG-DO	DAP JTAG Data Output	O

3.3.21 Power

Table 3-40 Power Signal Description

Signal Name[1]	Description[2]	Type[3]
VCC-PE-PD	Digital Port D and Port E Power Supply	P
VCC33-PC-PF	Digital Port C, Port F and ALDO Power Supply	P
VCC18-EFUSE-LDOA	Power Supply for EFUSE Program Mode and LDOA	P
VCC33-PB-USB	Power Supply for Port B, USB and LDOA	P

3.3.22 Interrupt

Table 3-41 Interrupt Signal Description

Signal Name[1]	Description[2]	Type[3]
PA-EINT [3:0]	Port A Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PB-EINT [3:0]	Port B Interrupt	I
PC-EINT [5:0]	Port C Interrupt	I
PD-EINT [22:0]	Port D Interrupt	I
PE-EINT [9:0]	Port E Interrupt	I
PF-EINT [6:0]	Port F Interrupt	I

3.3.23 GPADC

Table 3-42 GPADC Signal Description

Signal Name[1]	Description[2]	Type[3]
GPADC	General Purpose ADC Input	AI

3.3.24 PWM_BL

Table 3-43 PWM_BL Signal Description

Signal Name[1]	Description[2]	Type[3]
BOOST0-PWM	PWM Backlight Output 0	O
BOOST0-FB	PWM Backlight Input 0	I
BOOST1-PWM	PWM Backlight Output 1	O
BOOST1-FB	PWM Backlight Input 1	I

4 Electrical characteristics

4.1 Parameter Conditions

4.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at Ta = 25 °C and Ta = Ta max.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

4.1.2 Typical Values

Unless otherwise specified, the typical data are based on Ta = 25 °C. They are given only as design guidelines.

4.1.3 Temperature Definitions

- Ambient Temperature— the temperature of the surrounding environment.
- Junction Temperature— the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature— the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature— the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

4.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. The following table specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 4-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under section 4.3 Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 4-1 Absolute Maximum Ratings

Supply Name	Description	Min(1)	Max(1)	Unit
VCC-DRAM0	IO Power Supply for DRAM0 PHY	-0.3	1.8	V
VCC-DRAM1	IO Power Supply for DRAM1 PHY	-0.3	1.8	V
VCC18-PLL-HPVCC	Headphone Power	-0.3	2.1	V
AVCC	Power Supply for Analog Part	-0.3	2.1	V
VCC18-LVDS	LVDS and DSI Combo PHY Power Supply	-0.3	2.1	V
VCC-PE-PD	Digital Port D and Port E Power Supply	-0.3	3.6	V
VCC33-PC-PF	Digital Port C, Port F and ALDO Power Supply	-0.3	3.6	V
VCC18-EFUSE-LDOA	Power Supply for EFUSE Program Mode and LDOA	-0.3	2.1	V
VCC33-PB-USB	Power Supply for Port B, USB and LDOA	-0.3	3.6	V
VDD-CORE0 VDD-CORE1 VDD-CORE2	CPU/SYS Power Supply	-0.3	1.2	V
V_{ESD}(2)	Human Body Model (HBM)(3)	TBD	TBD	V
	Charged Device Model (CDM)(4)	TBD	TBD	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(5)	TBD		
	Latch-up over-voltage performance voltage injection on each IO pin(6)	TBD		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.

(5) Based on JESD78E; each device is tested with IO pin injection of ±150 mA at room temperature.

(6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

4.3 Recommended Operating Conditions

The following table describes operating conditions of the device.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 4-2 Recommended Operating Conditions

Supply Name	Description	Min	Typ	Max	Unit
VCC-DRAM0	IO Power Supply for DRAM0 PHY	1.425	1.5	1.575	V
VCC-DRAM1	IO Power Supply for DRAM1 PHY	1.425	1.5	1.575	V
VCC18-PLL-HPVCC	Headphone Power	1.782	1.8	1.818	V
AVCC	Power Supply for Analog Part	1.782	1.8	1.818	V
VCC18-LVDS	LVDS and DSI Combo PHY Power Supply	1.71	1.8	1.89	V
VCC-PE-PD	Digital Port D and Port E Power Supply	2.97	3.3	3.63	V
VCC33-PC-PF	Digital Port C, Port F and ALDO Power Supply	2.97	3.3	3.63	V
VCC18-EFUSE-LDOA	Power Supply for EFUSE Program Mode and LDOA	1.8	1.8	1.98	V
VCC33-PB-USB	Power Supply for Port B, USB and LDOA	3.07	3.3	3.6	V
VDD-CORE0 VDD-CORE1 VDD-CORE2	CPU/SYS Power Supply	0.9	0.92	0.99	V

4.4 GPIO DC Electrical Characteristics

Table 4-3 summarizes the GPIO DC electrical characteristics of the device.

Table 4-3 GPIO DC Electrical Characteristics(1)

(VCC: VCC33-PB-USB/VCC-PE-PD/VCC18-LVDS/VCC33-PC-PF/VCC18-PLL-HPVCC)

Symbol	Parameter		Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage		0.7 * VCC	-	1.1 * VCC	V
V_{IL}	Low-Level Input Voltage		-0.3	-	0.25 * VCC	V
R_{PU}	Output Pull-up Resistance	PC1, PC2, PC3, PC4, PE3, PF3,PF6	9	15	21	kΩ
		PE0, PE1, PE4, PE5, PF0, PF1, PF4, PF5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
R_{PD}	Output Pull-down Resistance	PC1, PC2, PC3, PC4, PE3, PF3,PF6	9	15	21	kΩ
		PE0, PE1, PE4, PE5, PF0, PF1, PF4, PF5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
I_{IH}	High-Level Input Current		-	-	10	uA
I_{IL}	Low-Level Input Current		-	-	10	uA
V_{OH}	High-Level Output Voltage		VCC – 0.3	-	VCC	V
V_{OL}	Low-Level Output Voltage		0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current		-10	-	10	uA
C_{IN}	Input Capacitance		-	-	5	pF
C_{OUT}	Output Capacitance		-	-	5	pF

(1) Guaranteed by design.

4.5 SMHC Electrical Characteristics

The SMHC electrical parameters are related to different supply voltage.

Figure 4-1 SMHC Voltage Waveform

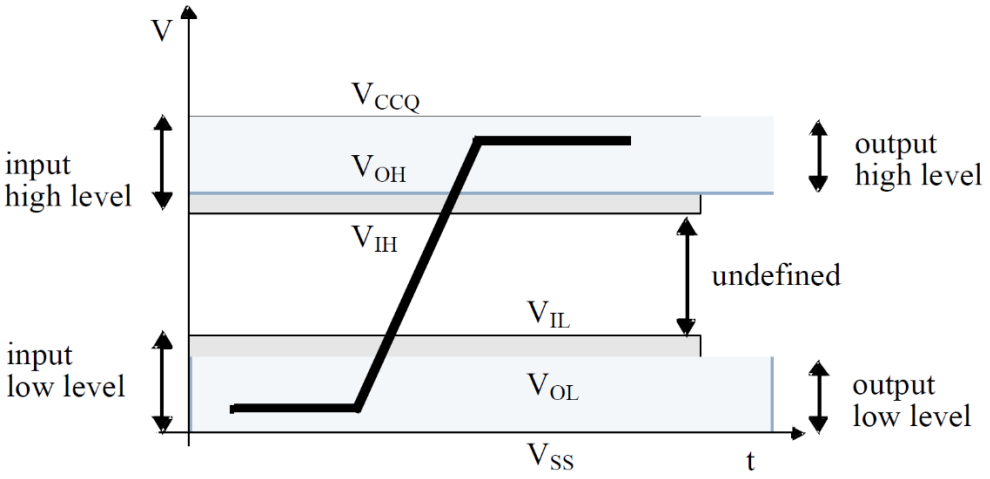


Table 4-4 shows 3.3 V SMHC electrical parameters.

Table 4-4 3.3 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125 * V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 4-5 shows 1.8 V SMHC electrical parameters.

Table 4-5 1.8 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.65 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V

Symbol	Parameter	Min	Typ	Max	Unit
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

4.6 GPADC Electrical Characteristics

Table 4-6 lists the GPADC electrical characteristics.

Table 4-6 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Sampling Rate	-	-	1	MHz

4.7 TPADC Electrical Characteristics

Table 4-7 lists the TPADC electrical characteristics.

Table 4-7 TPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Sampling Rate	-	-	750	kHz

4.8 Audio Codec Electrical Characteristics

Test Conditions

AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, 16-bit audio data unless otherwise stated.

Table 4-8 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	DAC to HPOUTL or HPOUTR(R=100K)					
	Full-scale	0dBFS 1kHz	-	545	-	mVrms
	SNR(A-weighted)	0data	-	99	-	dB
	THD+N	0dBFS 1kHz	-	-85	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-90	-	dB

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	DAC to HPOUTL or HPOUTR(R=16Ω)					
	Full-scale	0dBFS 1kHz	-	500	-	mVrms
	SNR(A-weighted)	0data	-	99	-	dB
	THD+N(10mW)	1kHz	-	-85	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-90	-	dB
	DAC to HPOUTL or HPOUTR(R=32Ω)					
	Full-scale	0dBFS 1kHz	-	530	-	mVrms
	SNR(A-weighted)	0data	-	99	-	dB
	THD+N(8.8mW)	0dBFS 1kHz	-	-85	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-90	-	dB
	DAC to LINEOUTLP/N or LINEOUTRP/N(R=100K)					
	Full-scale	0dBFS 1kHz	-	1080	-	mVrms
	SNR(A-weighted)	0data	-	100	-	dB
	THD+N	0dBFS 1kHz	-	-90	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-110	-	dB
ADC Path	**MICIN via ADC**					
	Output Level	MICP=3.3Vpp/2 MICN=3.3Vpp/2 1kHz, 0dB Gain	-	920	-	mFFS
	SNR(A-weighted)		-	95	-	dB
	THD+N		-	-90	-	dB
	Output Level	MICP=1.65Vpp/2 MICN=1.65Vpp/2 1kHz, 6dB Gain	-	920	-	mFFS
	SNR(A-weighted)		-	90	-	dB
	THD+N		-	-90	-	dB
	Output Level	MICP=0.828Vpp/2 MICN=0.828Vpp/2 1kHz, 12dB Gain	-	920	-	mFFS
	SNR(A-weighted)		-	80	-	dB
	THD+N		-	-90	-	dB
	Output Level	MICP=0.414Vpp/2 MICN=0.414Vpp/2 1kHz, 18dB Gain	-	920	-	mFFS
	SNR(A-weighted)		-	80	-	dB
	THD+N		-	-85	-	dB

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Output Level	MICP=0.208Vpp/2 MICN=0.208Vpp/2 1kHz, 24dB Gain	-	920	-	mFFS
	SNR(A-weighted)		-	85	-	dB
	THD+N		-	-80	-	dB
	Output Level	MICP=0.104Vpp/2 MICN=0.104Vpp/2 1kHz, 30dB Gain	-	920	-	mFFS
	SNR(A-weighted)		-	80	-	dB
	THD+N		-	-75	-	dB
	Output Level	MICP=0.053Vpp/2 MICN=0.053Vpp/2 1kHz, 36dB Gain	-	920	-	mFFS
	SNR(A-weighted)		-	80	-	dB
	THD+N		-	-70	-	dB
	LINEINLR via ADC					
	Output Level	LINEINL=1.65Vpp LINEINR=1.65Vpp 1kHz, 0dB Gain	-	905	-	mFFS
	SNR(A-weighted)		-	95	-	dB
	THD+N		-	-85	-	dB
	FMINLR via ADC					
	Output Level	FMINL=1.65Vpp FMINR=1.65Vpp 1kHz, 0dB Gain	-	905	-	mFFS
	SNR(A-weighted)		-	95	-	dB
	THD+N		-	-85	-	dB

4.9 MIPI DPHY Electrical Characteristics

This section describes some test parameters for MIPI DPHY based on D-PHY Physical Layer Conformance Test Suite Version 1.00.

Table 4-9 MIPI DPHY CTS Reference

Symbol	Parameters	Min	Typ	Max	Unit
Data Lane HS-TX Parameters					
$V_{OD(0)}$	Data Lane HS-TX Differential Voltages	-	222.4		mV
$V_{OD(1)}$	Data Lane HS-TX Differential Voltages	-	220.6	-	mV
ΔV_{OD}	Data Lane HS-TX Differential Voltage Mismatch	-	3	-	mV
t_R	Data Lane HS-TX 20%-80% Rise Time	-	0.305	-	UI
t_F	Data Lane HS-TX 80%-20% Fall Time		0.301	-	UI

Symbol	Parameters	Min	Typ	Max	Unit
Clock Lane HS-TX Parameters					
$V_{OD(0)}$	Clock Lane HS-TX Differential Voltages	-	264		mV
$V_{OD(1)}$	Clock Lane HS-TX Differential Voltages	-	224	-	mV
ΔV_{OD}	Clock Lane HS-TX Differential Voltage Mismatch	-	40	-	mV
t_R	Clock Lane HS-TX 20%-80% Rise Time	-	0.32	-	UI
t_F	Clock Lane HS-TX 80%-20% Fall Time		0.33	-	UI

4.10 External Clock Source Electrical Characteristics

4.10.1 High-speed Crystal/Ceramic Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 4-10 High-speed 24 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
f_{X24M_IN}	Crystal parallel resonance frequency	-	24	-	MHz
	Crystal frequency stability and tolerance at 25 °C (1)	-50	-	+50	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	6.5	-	pF

1. The 50 ppm frequency stability and tolerance can meet the requirement of the device. We recommend selecting 20 ppm crystal devices. If the REFCLK (24 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.
2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 4-11 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer

Symbol	Parameter
C_{shunt}	Total shunt capacitance

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1, C_2, and C_{shunt}.

The total load capacitance is $C_L = [(C_1 * C_2)/ (C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.
- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance (C_{pkg} + C_{PCB}) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

4.11 Interface Timing Characteristics

4.11.1 SMHC Interface Timing

4.11.1.1 HS-SDR Mode

NOTE

IO voltage is 1.8V or 3.3V.

Figure 4-2 SMHC HS-SDR Mode Output Timing Diagram

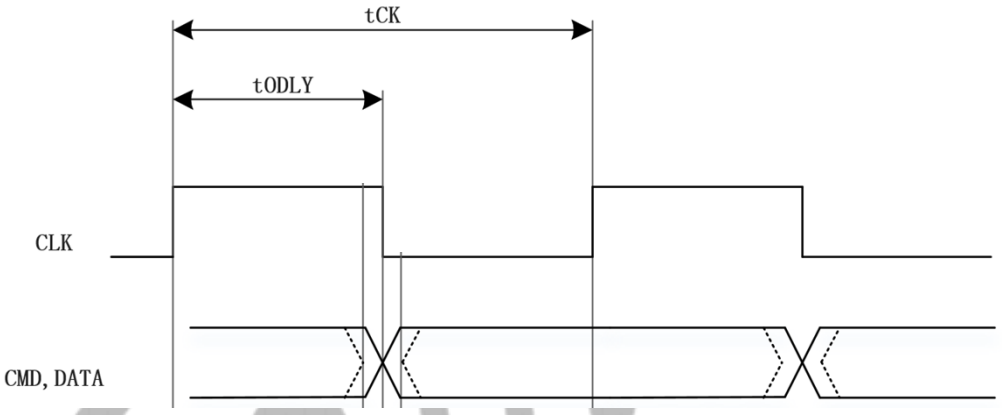


Table 4-12 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	30	50	70	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 4-3 SMHC HS-SDR Mode Input Timing Diagram

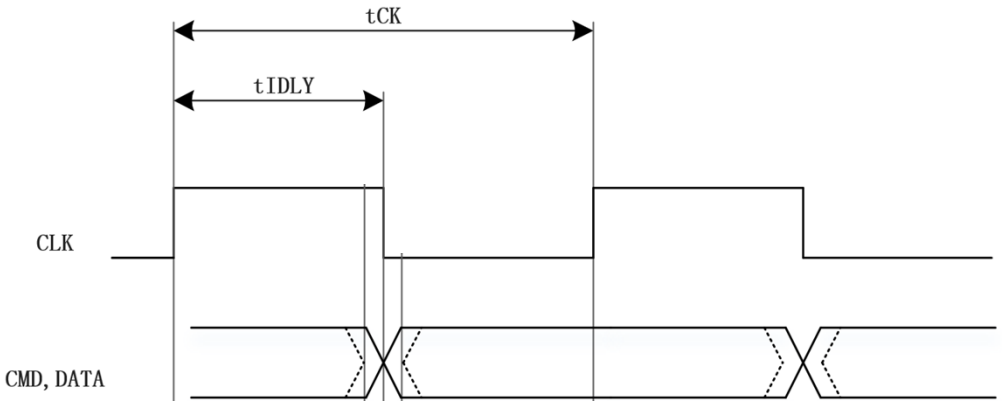


Table 4-13 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	30	50	70	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY	-	-	20	ns
The driver strength level of GPIO is 2 for test.					

4.11.1.2 HS-DDR Mode

Figure 4-4 SMHC HS-DDR Mode Output Timing Diagram

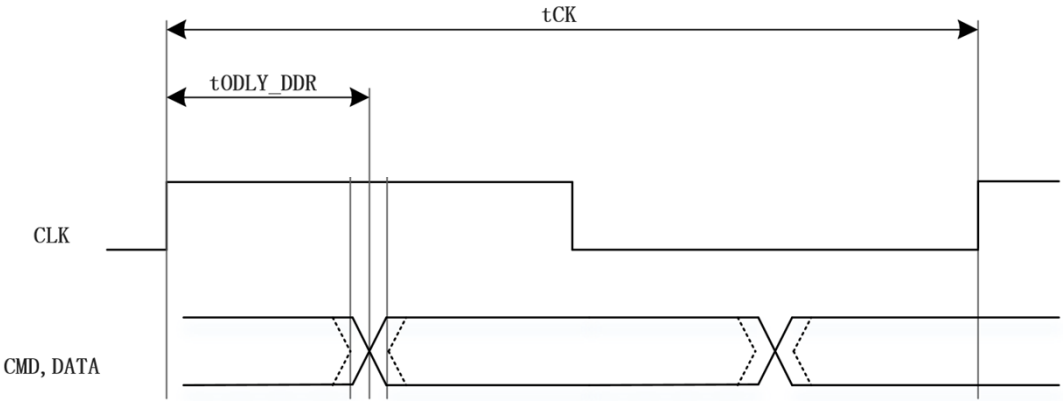


Table 4-14 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY-DDR	-	0.25	0.25	UI
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 4-5 SMHC HS-DDR Mode Input Timing Diagram

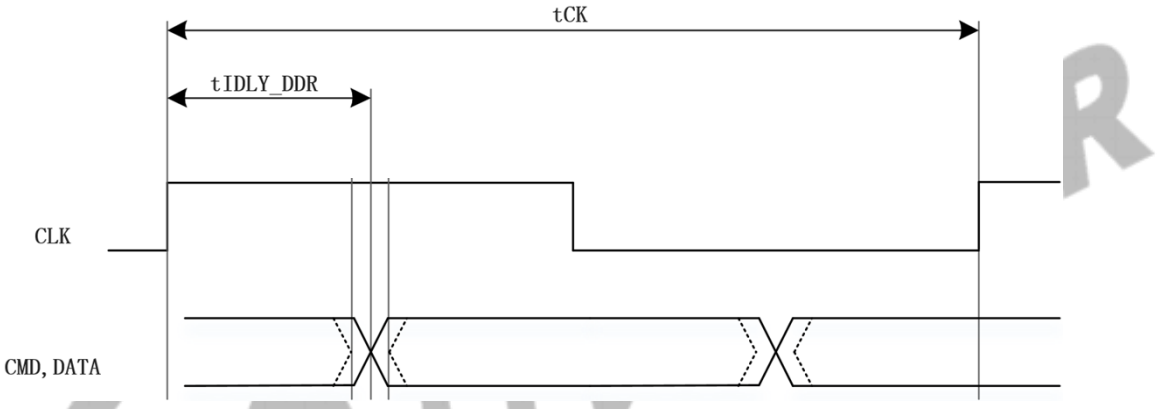


Table 4-15 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY-DDR	-	-	8.3	ns
The driver strength level of GPIO is 2 for test.					

4.11.1.3 SDR104 Mode

Figure 4-6 SMHC SDR104 Mode Host Output Timing and Device Input Timing Diagram

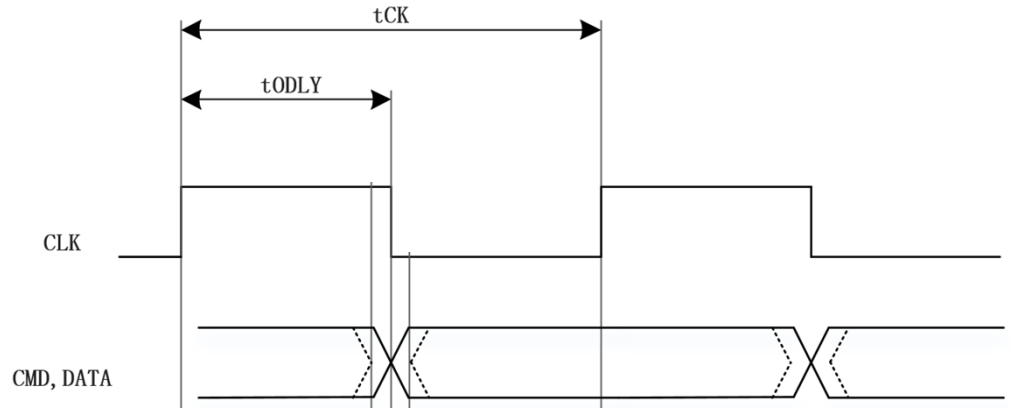


Table 4-16 SMHC SDR104 Mode Host Output Timing and Device Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	-	-	100	MHz
Duty Cycle	DC	30	50	70	%
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI
Host Output CMD, DATA (referenced to CLK)					
Host CMD, Data output delay time	tODLY	-	0.25	0.5	UI
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.					

Figure 4-7 SMHC SDR104 Mode Host Input Timing and Device Output Timing Diagram

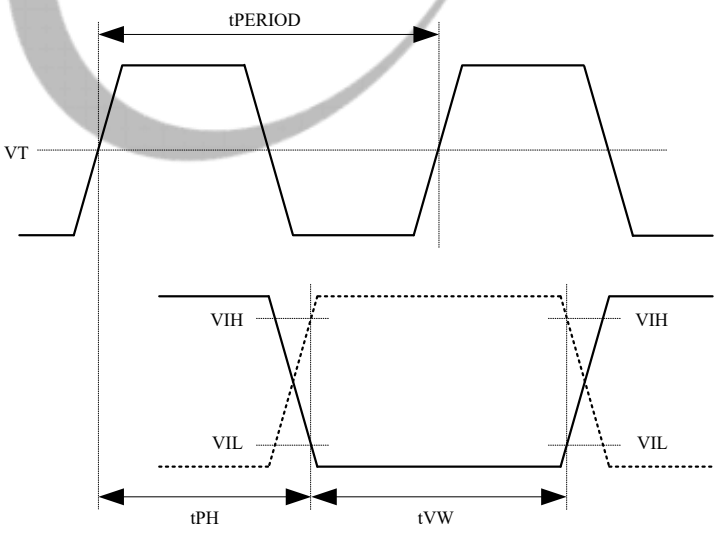


Table 4-17 SMHC SDR104 Mode Host Input Timing and Device Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	10	-	-	ns	Max: 100 MHz
Duty Cycle	DC	30	50	70	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Host Input CMD, DATA (referenced to CLK)						
Device Output delay	tPH	0	-	2	UI	
Device Output delay variation due to temperature change after tuning	dPH	-350(3)	-	1550(4)	ps	
Device CMD, Data valid window	tVW	0.575	-	-	UI	

(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.

(2) The driver strength level of GPIO is 3 for test.

(3) Temperature variation: -20 °C.

(4) Temperature variation: 90 °C.

4.11.2 LCD Interface Timing

Figure 4-8 HV_IF Vertical Timing

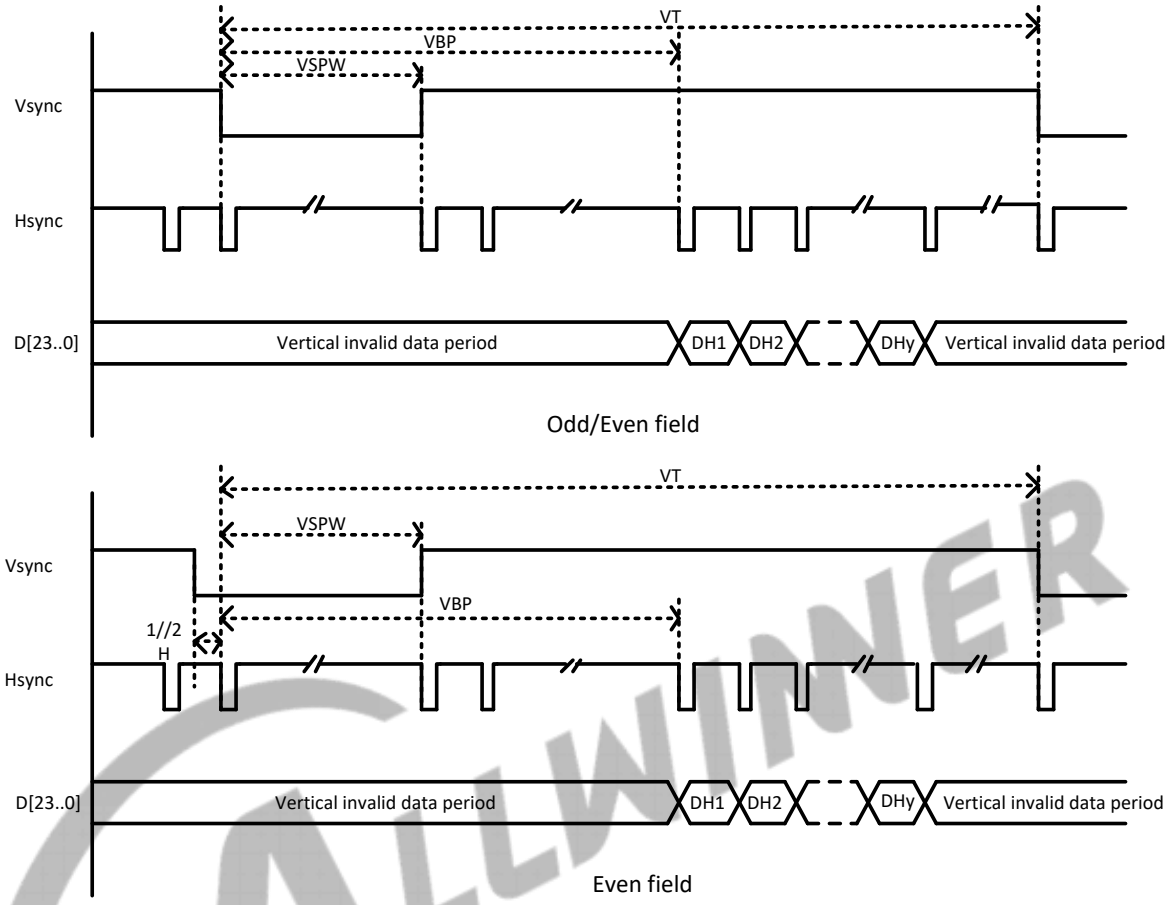
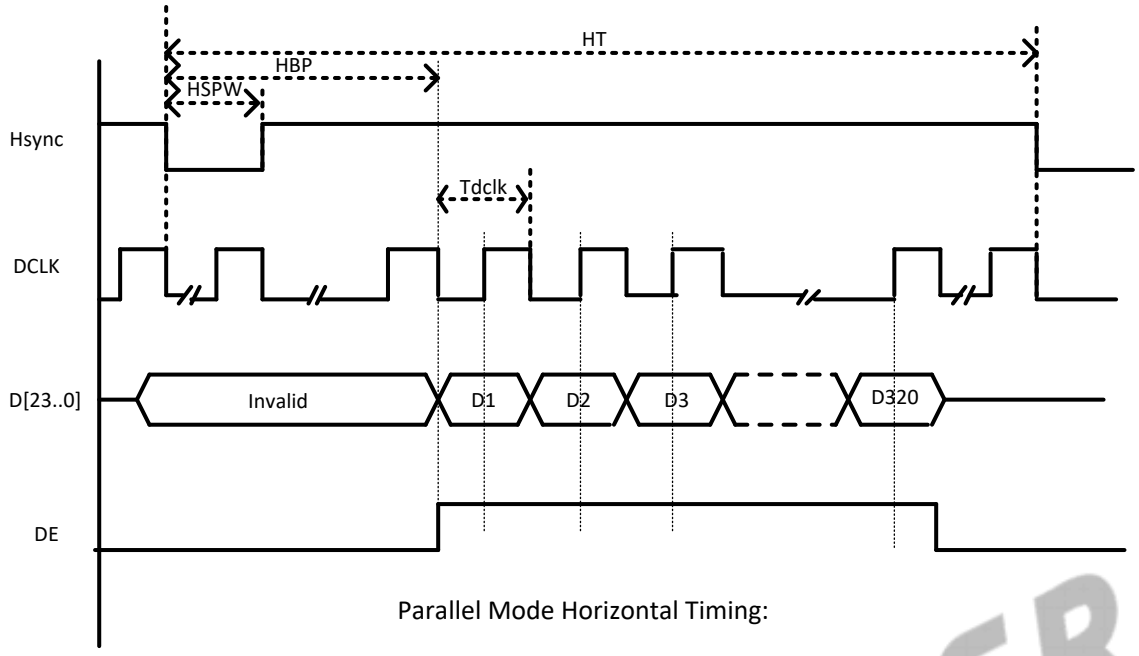
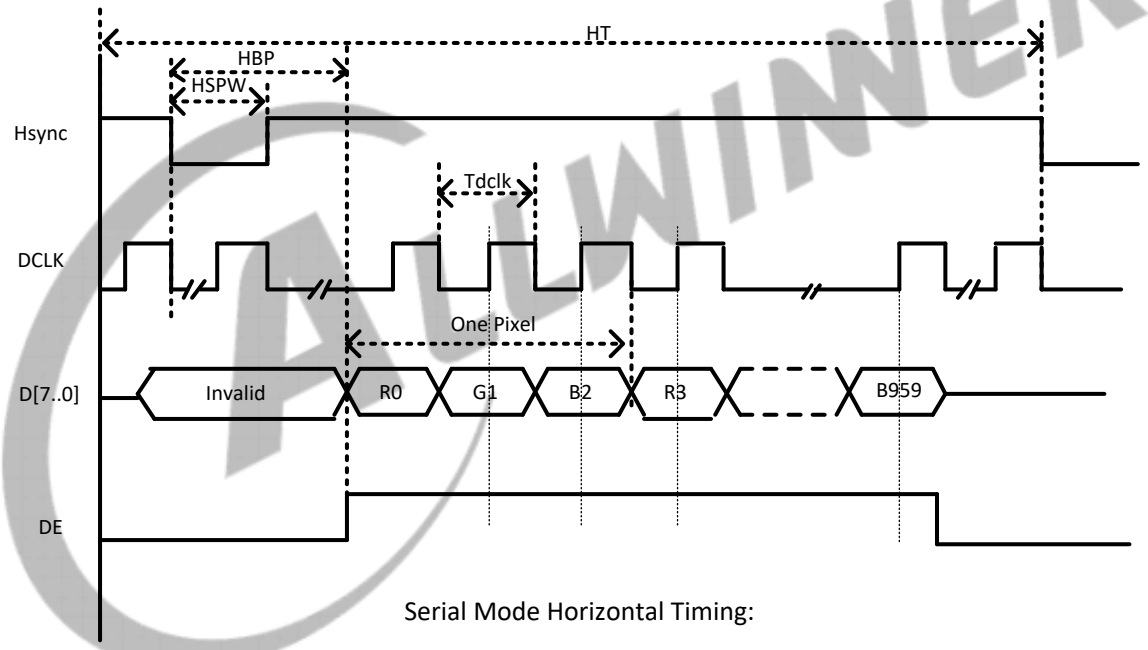


Figure 4-9 HV_IF Horizontal Timing



Parallel Mode Horizontal Timing:



Serial Mode Horizontal Timing:

Table 4-18 LCD HV_IF Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK Cycle Time	tDCLK	5.9	-	-	ns
Hsync Period Time	tHT	-	HT+1	-	tDCLK
Hsync Width	tHSPW	-	HSPW+1	-	tDCLK
Hsync Back Porch	tHBP	-	HBP+1	-	tDCLK
Vsync Period Time	tVT	-	VT/2	-	tHT
Vsync Width	tVSPW	-	VSPW+1	-	tHT

Parameter	Symbol	Min	Typ	Max	Unit
Vsync Back Porch	tVBP	-	VBP+1	-	tHT
(1) Vsync: Vertical sync, indicates one new frame. (2) Hsync: Horizontal sync, indicate one new scan line. (3) DCLK: Dot clock, pixel data are sync by this clock. (4) LDE: LCD data enable. (5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.					

4.11.3 Parallel CSI Interface Timing

Figure 4-10 Parallel CSI Data Sample Timing

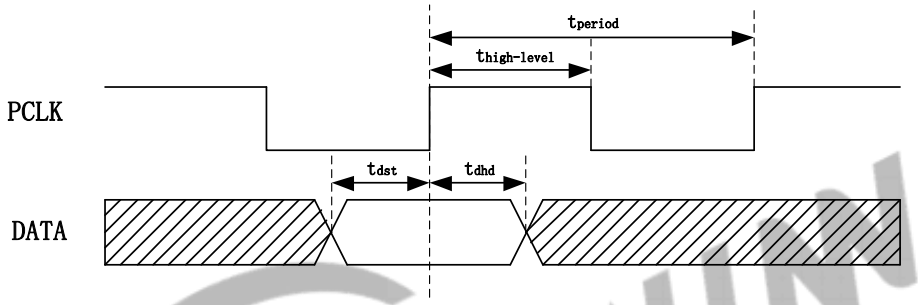


Table 4-19 Parallel CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.73	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

4.11.4 MIPI DPHY Interface Timing

Figure 4-11 MIPI DPHY Timing

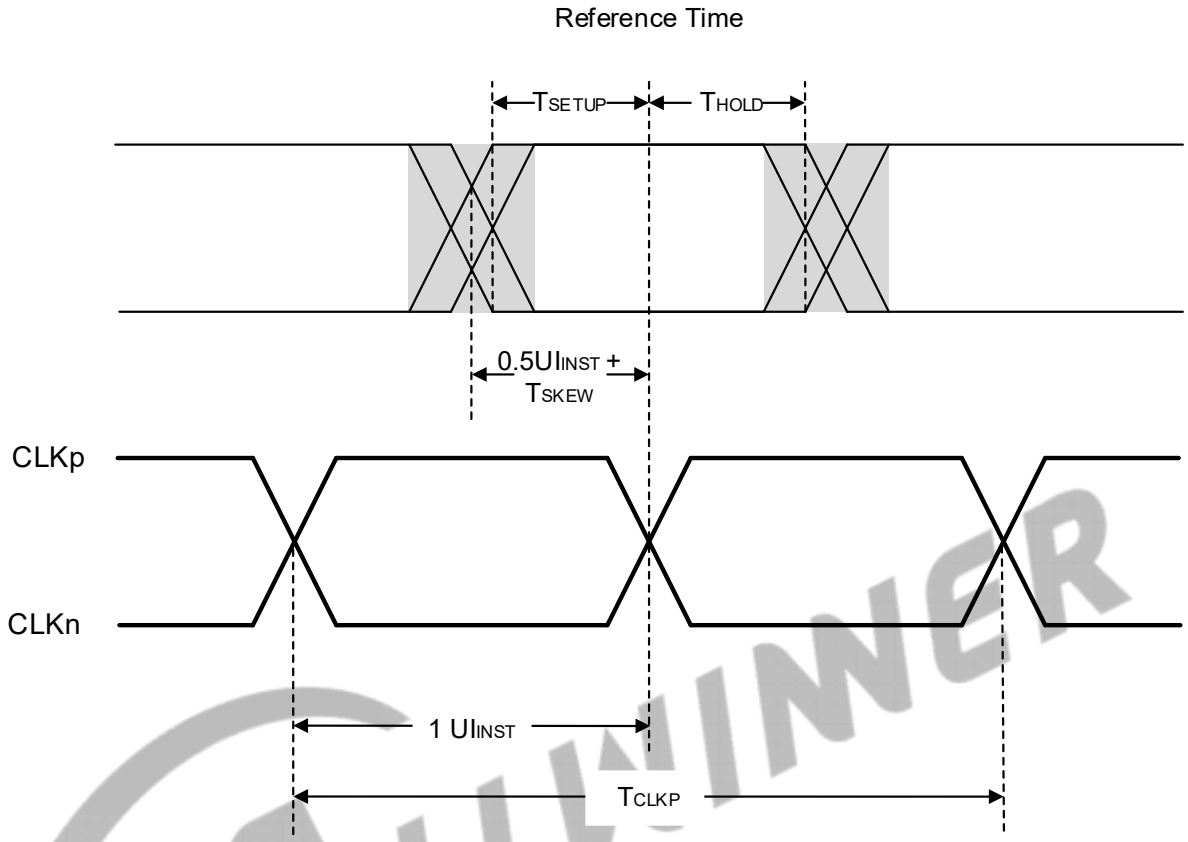


Table 4-20 MIPI DPHY Timing Constants

Parameter	Symbol	Units in Ulinst			Oprational Frequency in Gbps	
		Min	Max	Total	Min	Max
Data to Clock Skew	$T_{skew[tx]}$	-0.15	0.15	0.3	0.08	1.0
		-0.20	0.20	0.4	>1.0	1.5
Data to Clock Setup Time	$T_{setup[rx]}$	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5
Clock to Data Hold Time	$T_{hold[rx]}$	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5

4.11.5 SPI Interface Timing

Figure 4-12 SPI Writing Timing

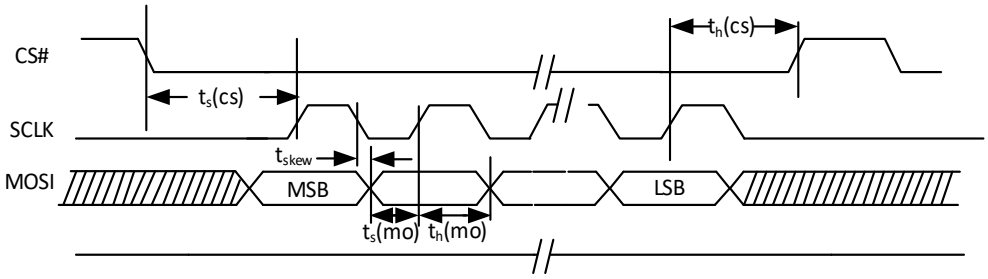


Figure 4-13 SPI Reading Timing

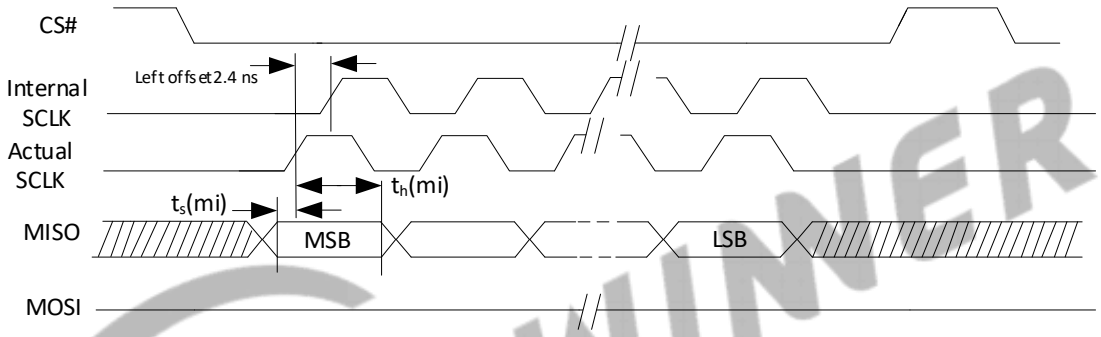


Table 4-21 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	t_s(cs)	2T(1)	-	-	ns
CS# Active Hold Time	t_h(cs)	2T(1)	-	-	ns
CLK/Data output skew time	t_{skew}(2)	-	-	1	ns
Data output Delay Time	t_v(mo)	T(1)/2-t_{skew}	-	T(1)/2+t_{skew}	ns
Data output Hold Time	t_h(mo)	T(1)/2-t_{skew}	-	T(1)/2+t_{skew}	ns
Data In Setup Time	t_s(mi)	0.2(master mode) 4.5(slave mode)	-	-	ns
Data In Hold Time	t_h(mi)	0.2(master mode) 2(slave mode)	-	-	ns

(1) T is the cycle of clock.

(2) t_{skew} is the output skew time between SCLK and MOSI. SCLK may be either faster or slower than MOSI.

4.11.6 SPI-DBI Interface Timing

Figure 4-14 DBI 3-line Serial Interface Timing

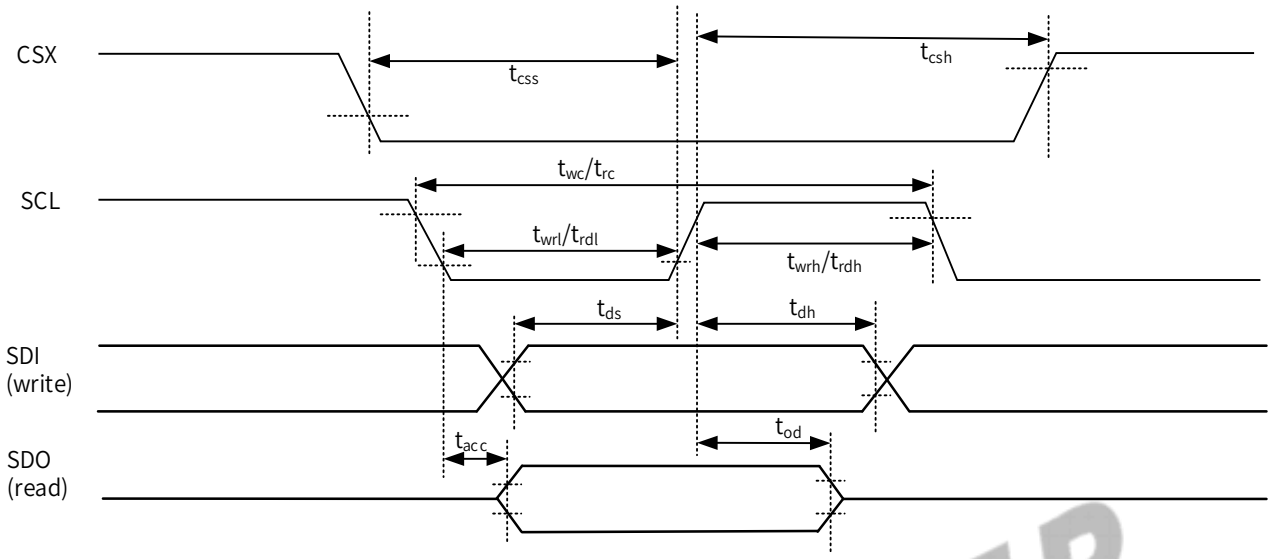


Table 4-22 DBI 3-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 4-23 DBI 3-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	10(1)	50	ns
	Output disable time	t_{od}	15(1)	50	ns

Signal	Parameter	Symbol	Min	Max	Unit
Note: Range of required clock frequency: 0-6.67 MHz.					

Figure 4-15 DBI 4-line Serial Interface Timing

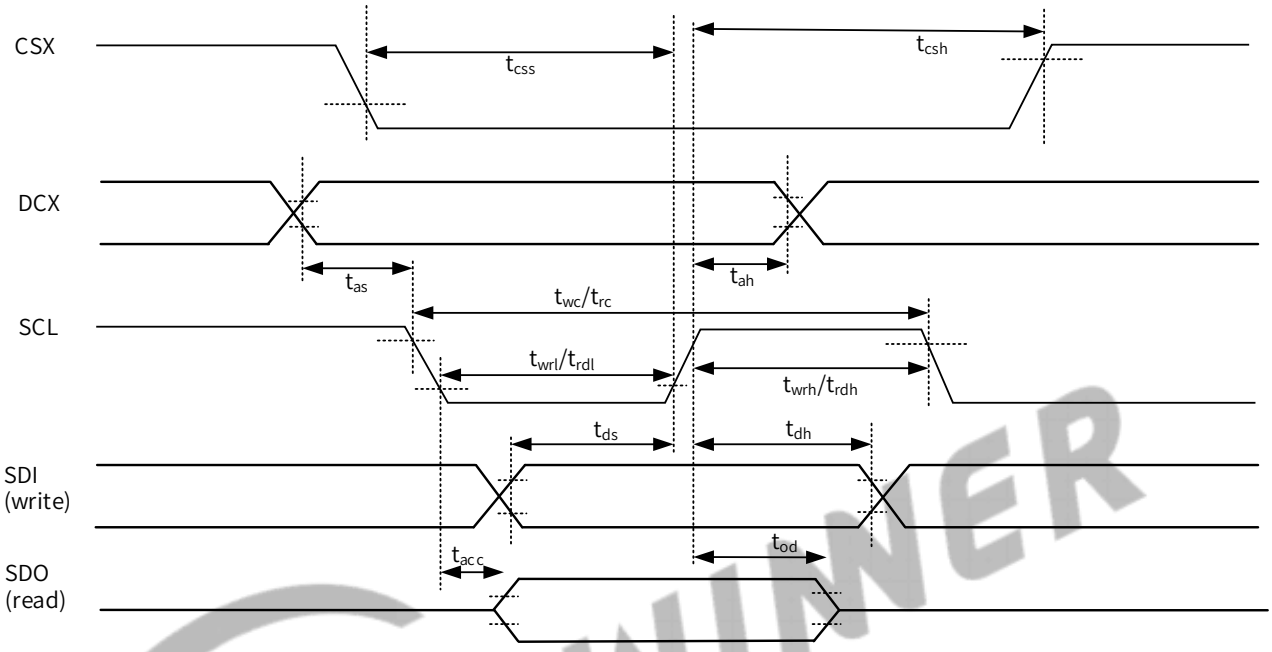


Table 4-24 DBI 4-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 4-25 DBI 4-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-6.67 MHz.					

4.11.7 SPI Flash Interface Timing

4.11.7.1 Controller Output to Target Input Timing

Figure 4-16 xSPI Target Data Input Timing

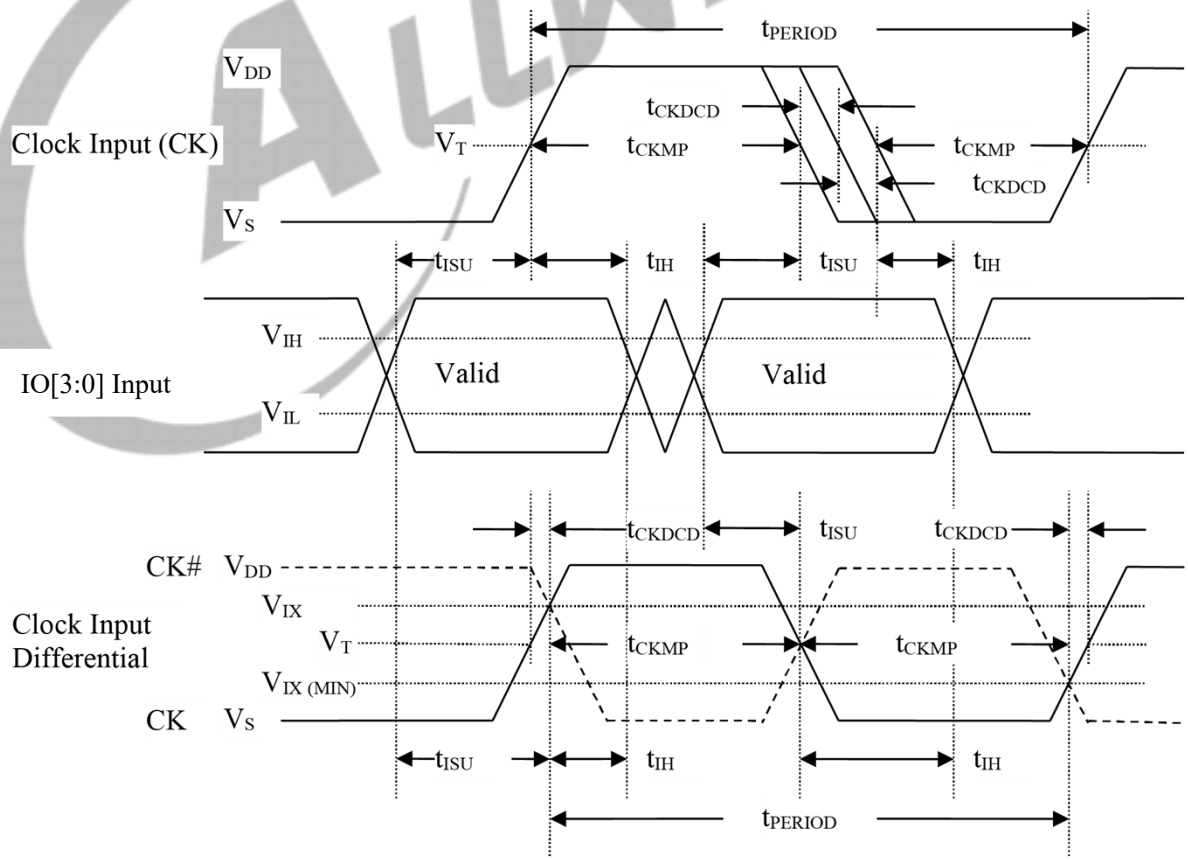


Table 4-26 Clock Input Threshold Levels

Parameter	Symbol	Min	Max	Unit
Clock Input Threshold (AC)	VT (AC)	0.50 * VDD	0.50 * VDD	V
Input differential crossing (AC)	VIX (AC)	0.4 * VDD	0.60 * VDD	V

Table 4-27 xSPI Device Input Timing

Parameter	Symbol	xSPI-333(1)		xSPI-266(2)		xSPI-200(3)		Unit	Comments
		Min	Max	Min	Max	Min	Max		
Input CK									
Cycle Time Data Transfer Mode	tPERIOD	6.66	-	7.5	-	10	-	ns	150 MHz (max) between the rising edges with respect to VT.
Slew Rate	SR	0.94	-	0.75	-	0.56	-	V/ns	With respect to VIH/VIL.
Duty Cycle Distortion	tCKDCD	0.0	0.3	0.0	0.375	0.0	0.5	ns	Allowable deviation from an ideal 50% duty cycle with respect to VT. Includes jitter and phase noise.
Minimum Pulse Width	tCKMPW	2.7	-	3.375	-	4.5	-	ns	With respect to VT.
Input Signals (Referenced to CK)									
Input Setup Time (DTR)	tISUddr	0.6	-	0.8	-	1.0	-	ns	With respect to VIH/VIL.
Input Hold Time (DTR)	tIHddr	0.6	-	0.8	-	1.0	-	ns	With respect to VIH/VIL.
Input Setup Time (STR)	tISU	1	-	2	-	2	-	ns	With respect to VIH/VIL.
Input Hold Time (STR)	tIH	1	-	2	-	2	-	ns	With respect to VIH/VIL.
Slew Rate @ 1.8 V	SR	0.94	--	0.75	-	0.56	-	V/ns	With respect to VIH/VIL and xSPI reference load.
Slew Rate @ 3.0 V	SR	1.72	-	1.37	-	1.03	-	V/ns	With respect to VIH/VIL and xSPI reference load.
Note:									

Parameter	Symbol	xSPI-333(1)		xSPI-266(2)		xSPI-200(3)		Unit	Comments
		Min	Max	Min	Max	Min	Max		
xSPI-333: Up to 166 MHz; up to 333 MT/s. xSPI-266: Up to 133 MHz; up to 266 MT/s. xSPI-200: Up to 100 MHz; up to 200 MT/s.									

4.11.7.2 Target Output to Controller Input Timing

Figure 4-17 xSPI Target Data Output Timing

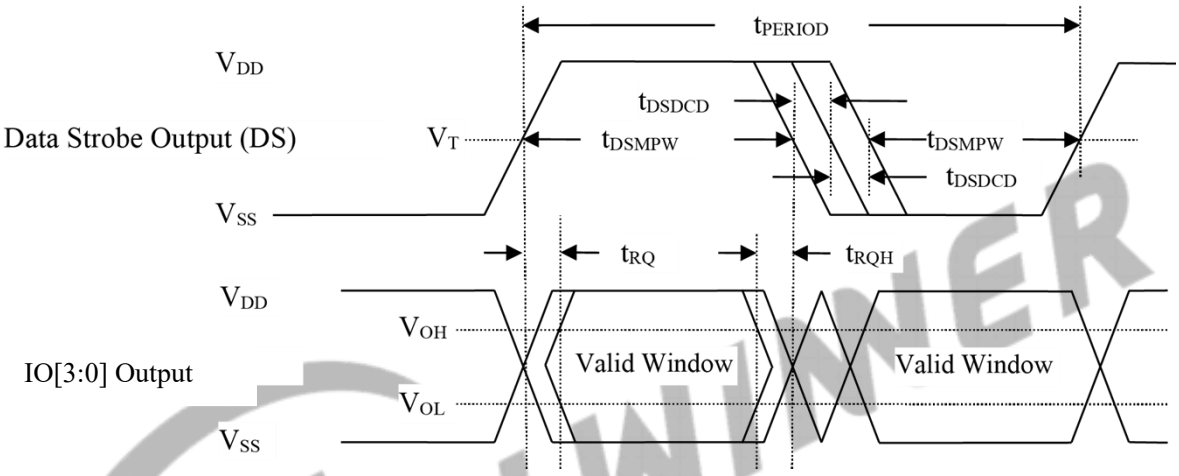


Table 4-28 xSPI Device Output Timing

Parameter	Symbol	xSPI-200(1)		Unit	Comments
		Min	Max		
Data Strobe(2)					
Cycle Time Data Transfer Mode	tPERIOD	10	-	ns	100 MHz (max) between the rising edges with respect to VT.
Duty Cycle Distortion	tDSDCD	0.0	0.4	ns	Allowable deviation from the input clock duty cycle distortion (tCKDCD) with respect to VT. Includes jitter and phase noise.
Minimum Pulse Width	tDSMPW	4.1	-	ns	Minimum Pulse Width of DS is smaller than that of CK since the target is allowed to add distortion when generating DS from CK. With respect to VT.
Output DATA (Referenced to DS)					
Output skew	tRQ	-	0.8	ns	With respect to VOH/VOL and xSPI reference load.

Parameter	Symbol	xSPI-200(1)		Unit	Comments
		Min	Max		
Output hold skew	tRQH	-	0.8	ns	With respect to VOH/VOL and xSPI reference load.
Note: (1) xSPI-200: Up to 100 MHz; up to 200 MT/s. (2) Controller CK edges are the trigger for target IO and DS edges. IO and DS edges therefore always follow their related (triggering) CK edges.					

4.11.8 UART Interface Timing

Figure 4-18 UART RX Timing

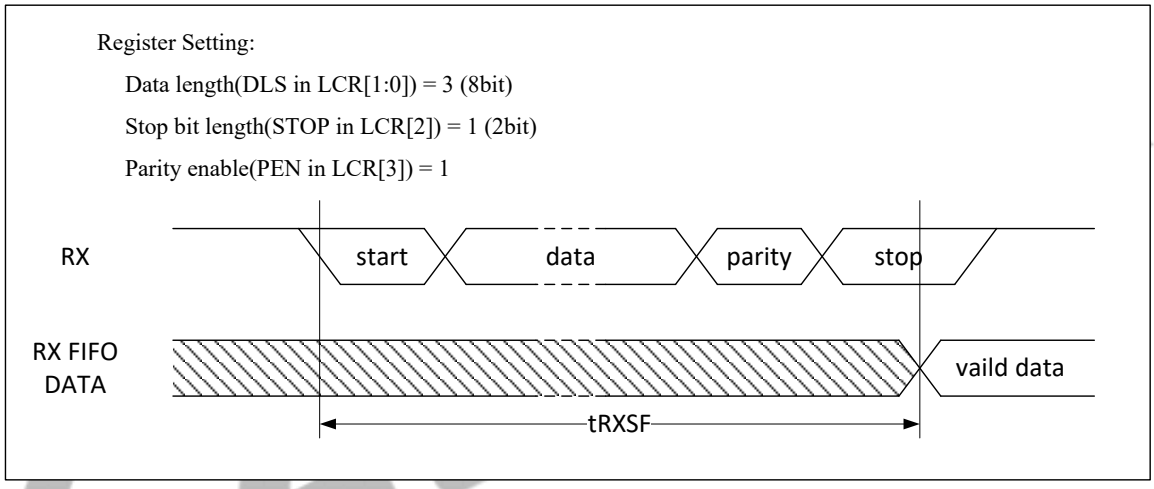


Figure 4-19 UART nCTS Timing

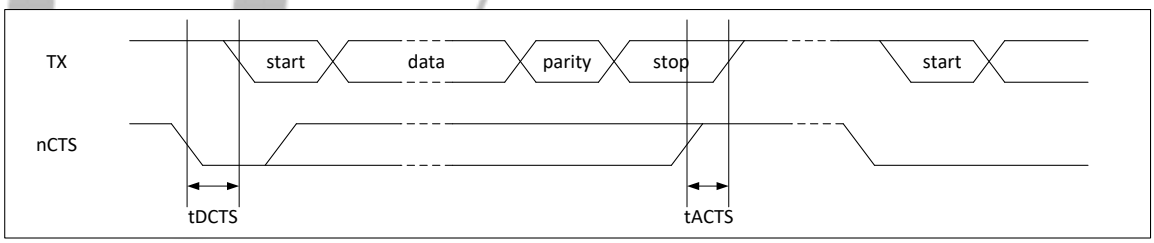


Figure 4-20 UART nRTS Timing

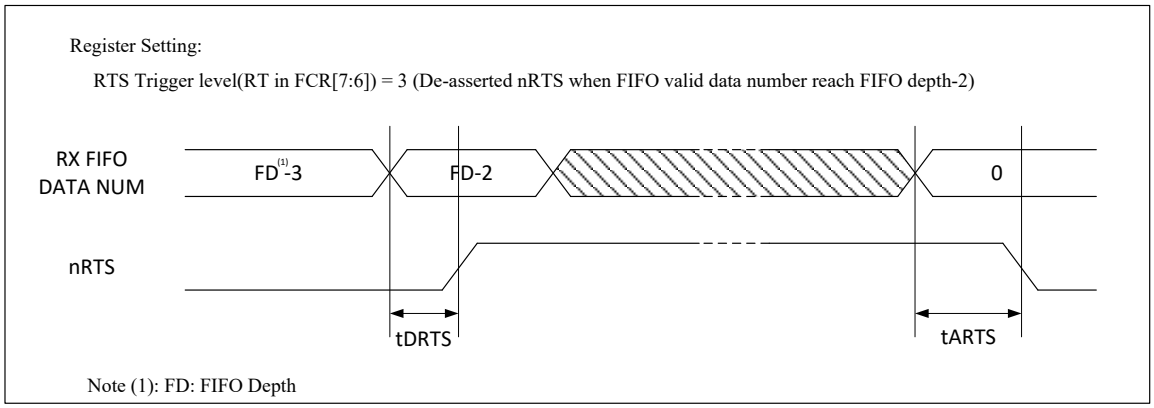


Table 4-29 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5*BRP(1)	-	11*BRP(1)	ns
Delay time of de-asserted nCTS to TX strat	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1) /4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
(1) BRP: Baud-Rate Period.					

4.11.9 TWI Interface Timing

Figure 4-21 TWI Timing

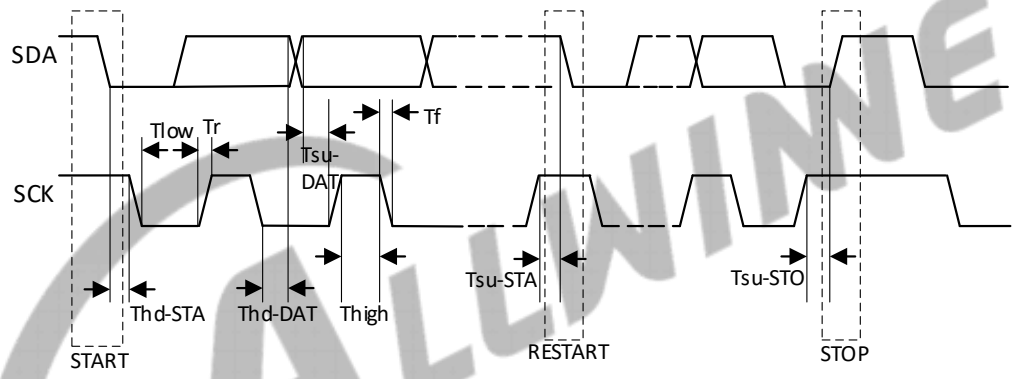


Table 4-30 TWI Timing Parameters

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data (I2C-bus devices)	Thd-DAT	0	-	0	-	us
Setup Time In Stop	Tsu-STO	4.0	-	0.6	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us
SCK High level Time	Thigh	4.0	-	0.6	-	us
SCK/SDA Falling Time	Tf	-	300	20	300	ns

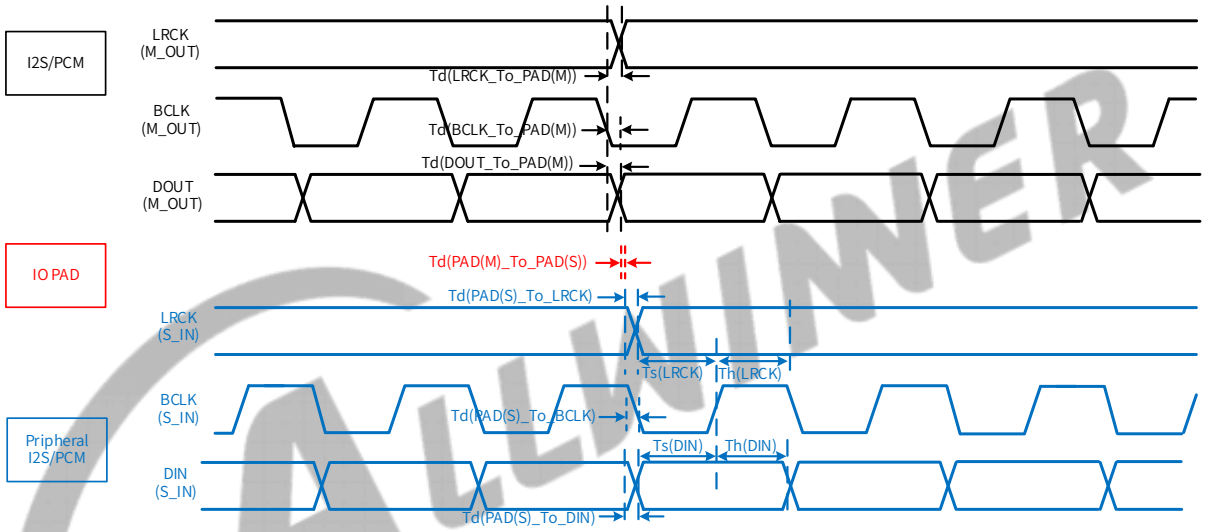
Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

4.11.10 I2S/PCM Interface Timing

4.11.10.1 Data Output timing of I2S/PCM in Master mode

The Data Output timing of I2S/PCM in Master mode and the Data Input timing of Peripheral I2S/PCM in Slave mode show in Figure 4-22.

Figure 4-22 Data Output Timing of I2S/PCM in Master Mode



The Data Output timing parameters of I2S/PCM in Master mode and The Data Input timing parameters of Peripheral I2S/PCM in Slave mode show in Table 4-31.

Table 4-31 Data Output Timing Parameters of I2S/PCM in Master Mode

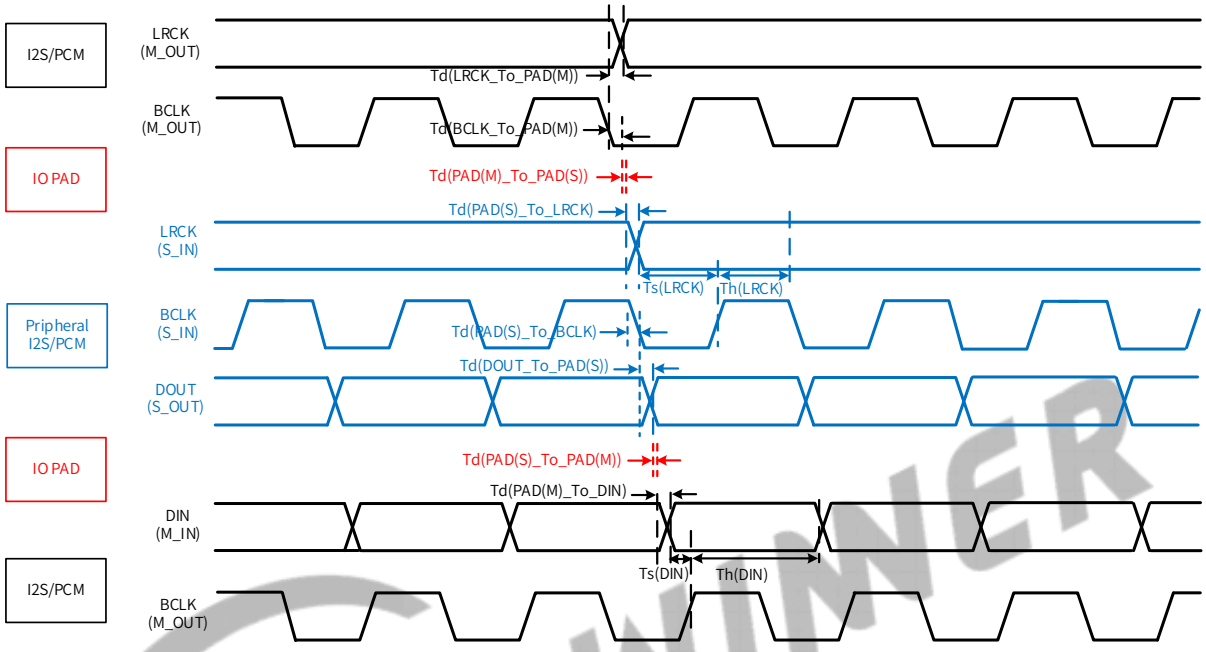
Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
T_d(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5 (restriction)	T_w1<2.5(requirement)	ns
T_d(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(restriction)		
T_d(DOUT_To_PAD(M))	DOUT to PAD(M) Delay	/	T3<6.5(restriction)		

Parameter		Min	Max	Skew	Units
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
T_d(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T4*<7.0(estimation)	T_w2*<1.0(requirement)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay	/	T5*<7.0(estimation)		
	DOUT PAD(M) to DIN PAD(S) Delay	/	T6*<7.0(estimation)		
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
T_d(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T7*<6.5(assumption)	T_w3*<2.5(requirement)	ns
T_d(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T8*<6.5(assumption)		
T_d(PAD(S)_To_DIN)	PAD(S) to DIN Delay	/	T9*<6.5(assumption)	/	/
T_s(LRCK)	LRCK Setup Slack	T10*(analysis)	/	/	ns
T_h(LRCK)	LRCK Hold Slack	T11*(analysis)	/	/	ns
T_s(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
T_h(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

4.11.10.2 Data Input timing of I2S/PCM in Master mode

The Data Input timing of I2S/PCM in Master mode and the Data Output timing of Peripheral I2S/PCM in Slave mode show in Figure 4-23.

Figure 4-23 Data Input Timing of I2S/PCM in Master Mode



The Data Input timing parameters of I2S/PCM in Master mode and The Data Output timing parameters of Peripheral I2S/PCM in Slave mode are shown in Table 4-32.

Table 4-32 Data Input Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5(requirement)	Tw1<2.5 (estimation)	ns
Td(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(requirement)		ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T3*<7.0(requirement)	Tw2*<1.0 (estimation)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay		T4*<7.0(requirement)		

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T5*<6.5(requirement)	Tw3*<2.5 (estimation)	ns
Td(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T6*<6.5(requirement)		ns
Td(DOUT_To_PAD(S))	DOUT to PAD(S) Delay	/	T7*<6.5(requirement)	/	ns
Ts(LRCK)	LRCK Setup Slack	T8*(analysis)	/	/	ns
Th(LRCK)	LRCK Hold Slack	T9*(analysis)	/	/	ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_PAD(M))	DOUT PAD(S) to DIN PAD(M) Delay	/	T10*<7.0(requirement)	/	ns
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(PAD(M)_To_DIN)	PAD(M) to DIN Delay	/	T11<6.5(requirement)	/	ns
Ts(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
Th(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

4.11.11 OWA Interface Timing

Figure 4-24 OWA Timing

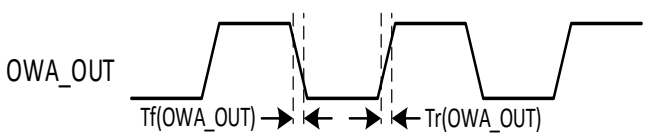


Table 4-33 OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit

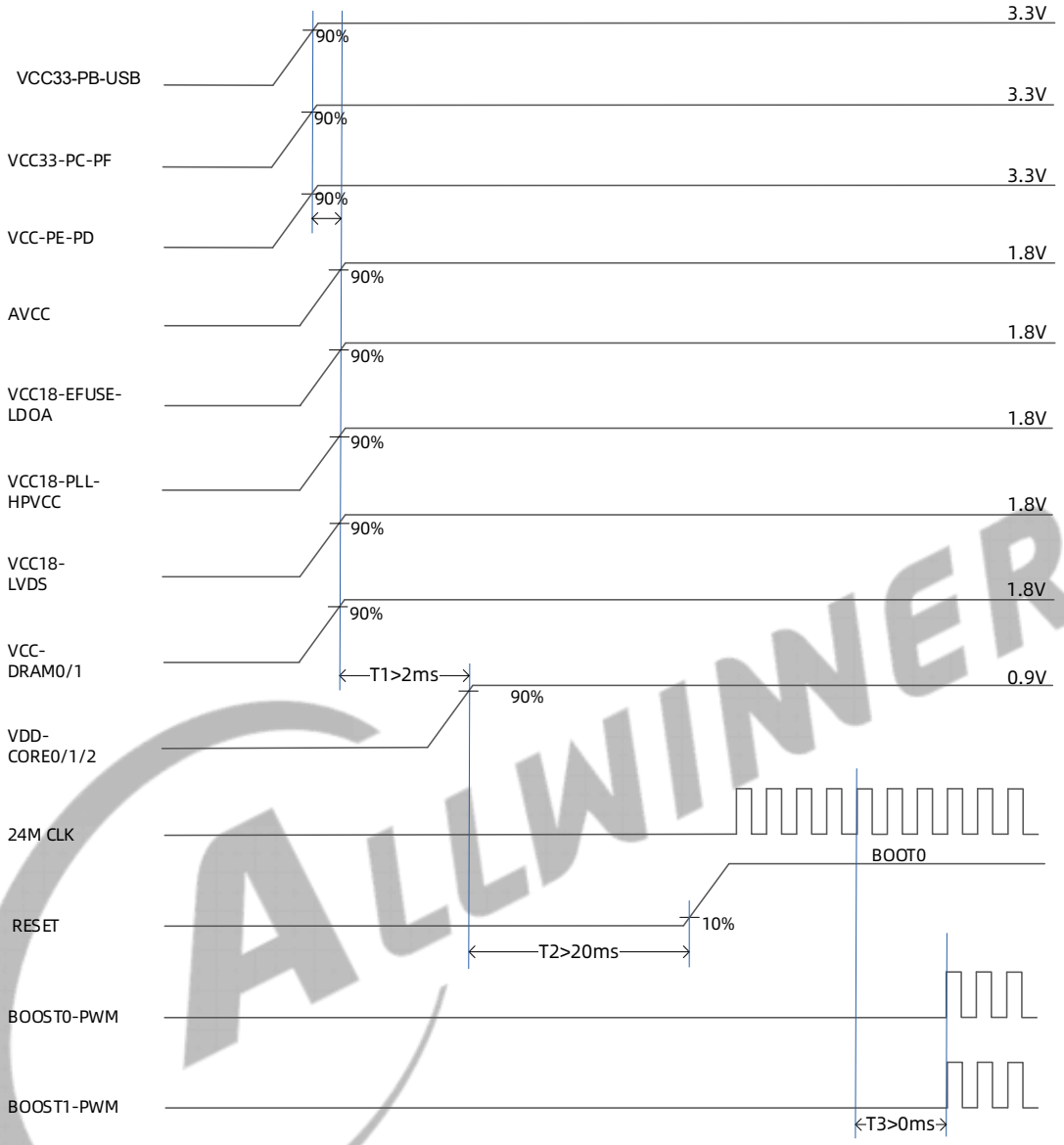
Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT Rise Time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT Fall Time	Tf(OWA_OUT)	-	-	8	ns

4.12 Power-Up and Power-Down Sequence

4.12.1 Power-Up Sequence

The following figure shows an example of the power-up sequence for the SoC.

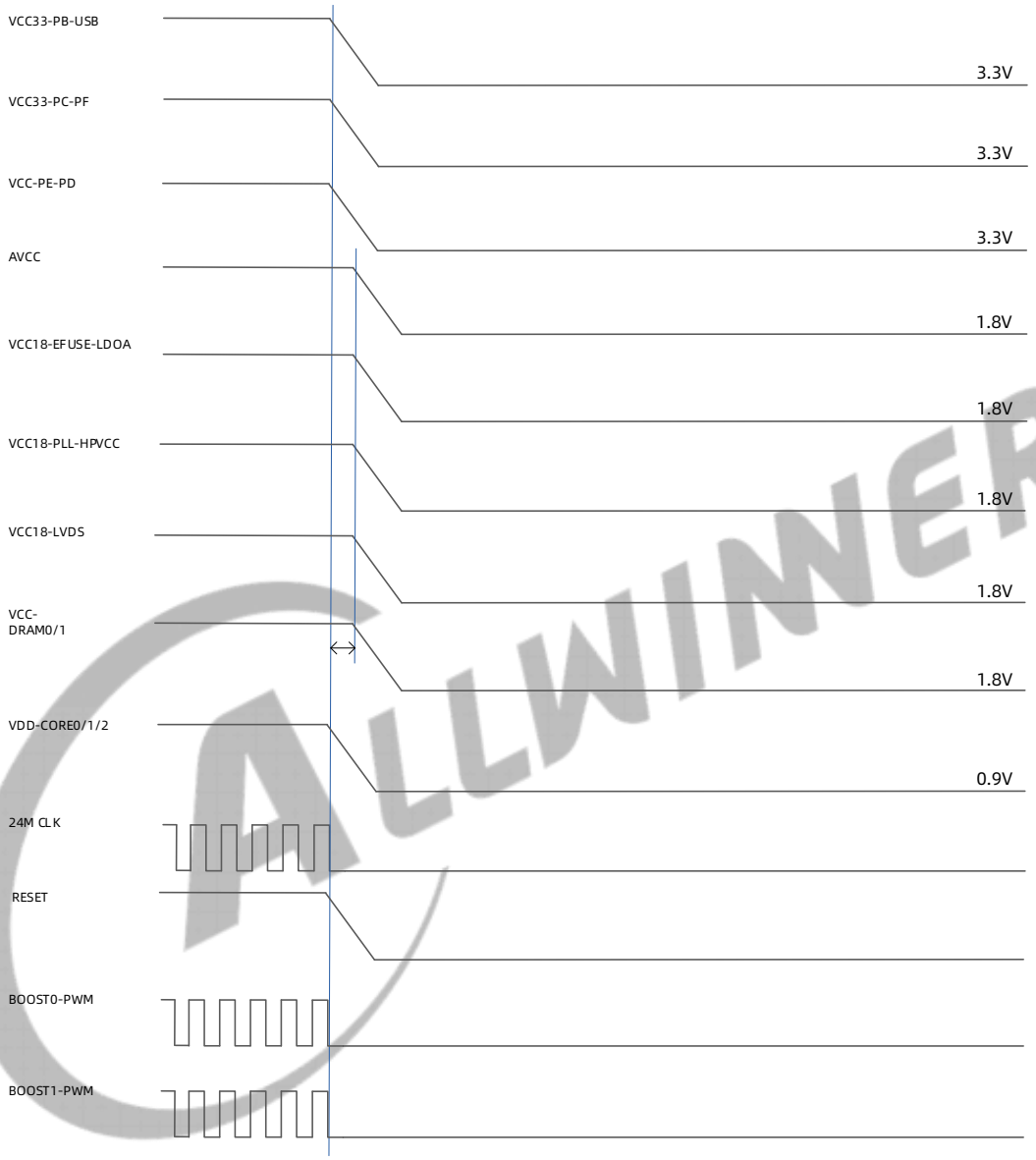
Figure 4-25 Power-Up Sequence



4.12.2 Power-Down Sequence

The following figure shows an example of the power-down sequence for the SoC.

Figure 4-26 Power-Down Sequence



5 Temperature and Thermal Characteristics

5.1 Temperature

The following tables describe the temperature of the device

Table 5-1 Operating and Storage Temperature

Symbol	Parameter	Min	Max	Unit
T_a	Ambient Operating Temperature	-15	65	°C
T_{STG}	Storage Temperature	-40	150	°C

Table 5-2 Junction Temperature

Chip	Recommended Operating Temperature (T_j)		Absolute Maximum Junction Temperature	Unit
	Min	Max		
F102MX	TBD	TBD	TBD	°C

5.2 Package Thermal Characteristics

The maximum chip junction temperature ($T_{J\ max}$) must never exceed the values given in Table 5-2 Junction Temperature.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the device. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 5-3 Package Thermal Characteristics

Symbol	Parameter	Min	Typ(1)(2)	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	23.8	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	18.44	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	4	-	°C/W

(1) Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

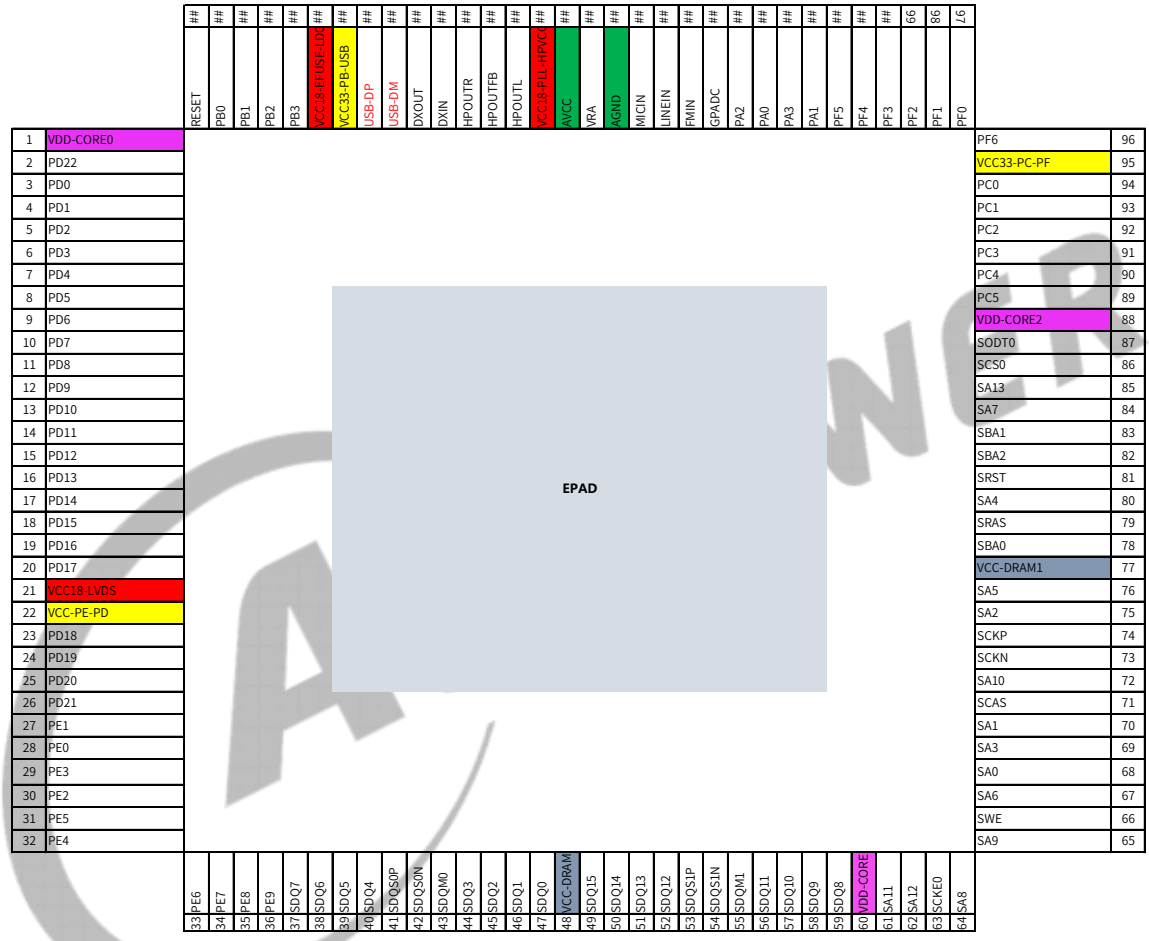
(2) The testing PCB is 4 layers, 114.5 mm x 76.2 mm body, and 1.6 mm thickness. Ambient temperature is 25 °C.

6 Pin Assignment

6.1 Pin Map

The following shows the QFN 128 pins, 12.3 mm x 12.3 mm pin map.

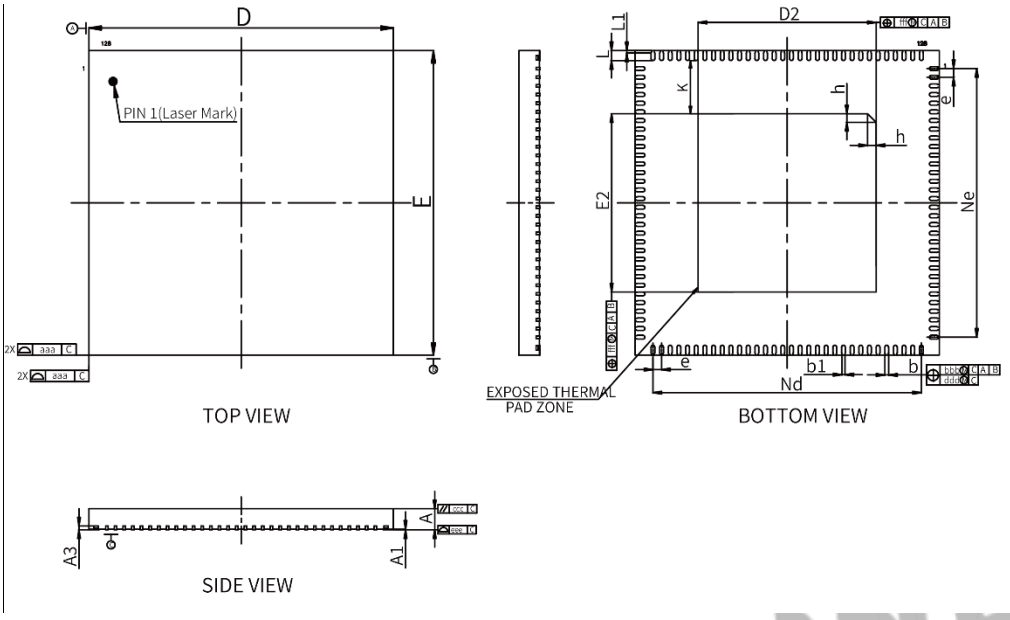
Figure 6-1 Pin Map



6.2 Package Dimension

The following figure shows the top, bottom, and side views of the package.

Figure 6-2 Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.10	0.15	0.18
b1	0.100REF		
A3	0.152REF		
D	12.20	12.30	12.40
D2	7.10	7.20	7.30
e	0.35BSC		
Nd	10.85BSC		
E	12.20	12.30	12.40
E2	7.10	7.20	7.30
Ne	10.85BSC		
L	0.30	0.40	0.50
L1	0.10REF		
h	0.30	0.35	0.40
K	2.15REF		
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

7 Carrier, Storage and Backing Information

7.1 Carrier

The following table shows matrix tray carrier information.

Table 7-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	322.6 mm x 135.9 mm x 7.62 mm	152 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

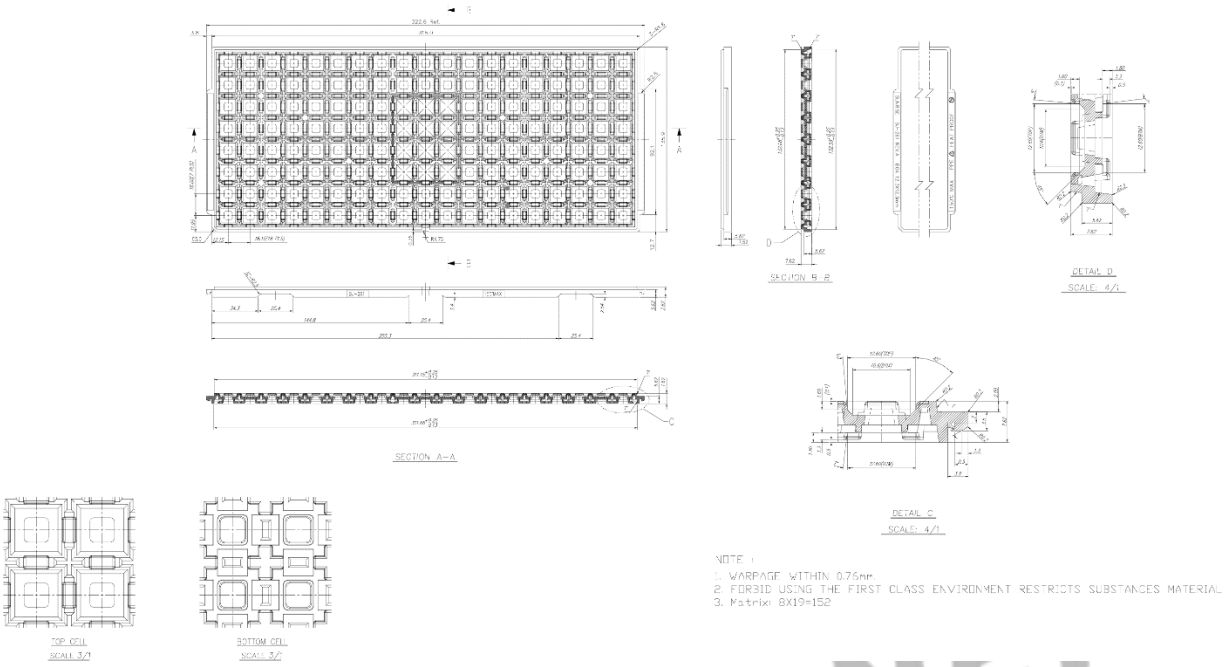
The following table shows packing quantity.

Table 7-2 Packing Quantity Information

Sample	Size	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
F102MX	12.3 mm x 12.3 mm	152	10	1520	6	9120

The following figure shows tray dimension drawing.

Figure 7-1 Tray Dimension Drawing



7.2 Storage

Reliability is affected if any condition specified in section 7.2.2 and section 7.2.3 has been exceeded.

7.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 7-3 defines all MSL.

Table 7-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label (TOL)	≤30°C / 60%RH

NOTE

The F102MX device samples are classified as MSL3.

7.2.2 Bagged Storage Conditions

The following table defines the shelf life.

Table 7-4 Bagged Storage Conditions

Packing Mode	**Vacuum packing**
Storage Temperature	20–26°C
Storage Humidity	40%–60%RH
Shelf Life	12 months

7.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration is as follows.

Table 7-5 Out-of-bag Duration

Storage Temperature	20–26°C
Storage Humidity	40%–60%RH
Moisture Sensitive Level (MSL)	3
Floor Life	168 hours

For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

7.3 Baking

It is not necessary to bake chips if the conditions specified in section 7.2.2 and section 7.2.3 have not been exceeded. It is necessary to bake chips if any condition specified in section 7.2.2 and section 7.2.3 has been exceeded.

It is necessary to bake chips if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.

8 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

The following figure shows the appropriate reflow profile.

Figure 8-1 Lead-free Reflow Profile

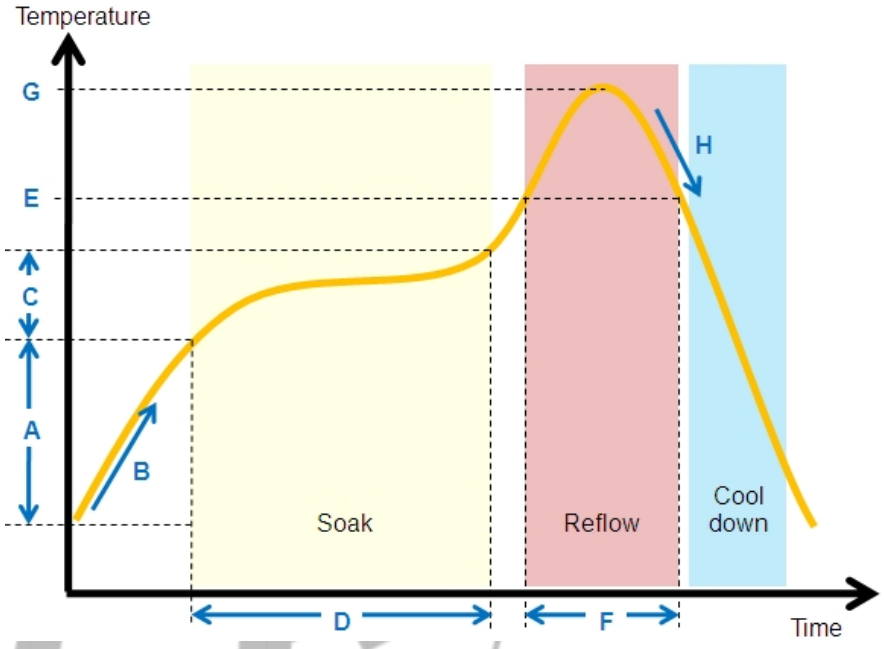


Table 8-1 Lead-free Reflow Profile Conditions

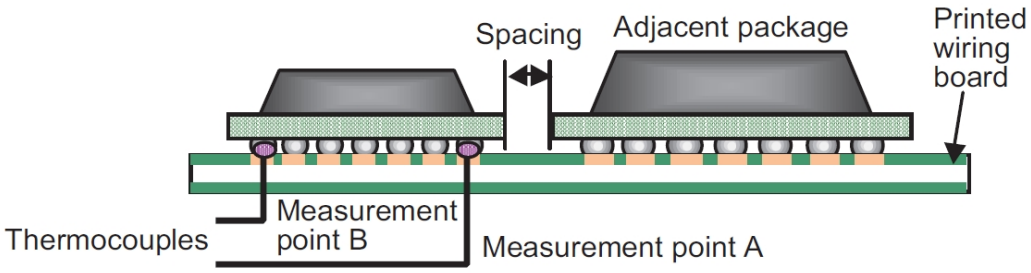
	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C -> 150 °C
B	Preheat ramp up rate	1.5–2.5 °C/s
C	Soak temperature range	150 °C -> 190 °C
D	Soak time	80–110 s
E	Liquidus temperature	217°C
F	Time above liquidus	60–90 s

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
G	Peak temperature	240–250 °C
H	Cool down temperature rate	⩽4°C/s

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 10 2.

Figure 8-2 Measuring the Reflow Soldering Process



NOTE

To measure the temperature of the QFN-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

9 Part Marking

9.1 F102MX-XXX

The following figure shows the F102MX-XXX marking.

Figure 9-1 F102MX-XXX Marking

The following table describes the F102MX-XXX marking definitions.

Table 9-1 F102MXM2-CXX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	F102MX-XXX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

Allwinner Technology Co.,Ltd.
No.9 Technology Road 2, High-Tech Zone,
Zhuhai, Guangdong Province, China

Contact US:
Service@allwinnertech.com
www.allwinnertech.com