

REV	Description	DATE	BY
A4A	Initial production Release.	11/19/2012	GC
A5	On the initial production release the processors were to be found incorrect as supplied by TI. Parts while marked AM3359 were actually AM3352. This revision uses the correct parts.	1/2/2013	GC
A5A	<ol style="list-style-type: none"> Deleted R29-R44 from the LCD lines. Added 47pf capacitors C156-C173 to LCD data lines to ground. Changed schematic revision to A5A. Changed a few footprints after PCB update for above changes. Added access point for the battery function of the TPS65217C. Added Ferrite beads in series with LED power and 5V power rail of the USB host connector. Required to pass FCC/CE testing due to noise emissions on that pin. Added power button to enable sleep, wakeup, power down and power up features on the system. Added Modification to add 100K ohm resistor to ground to prevent crosstalk when serial cable is not plugged in. 	2/8/2013	GC
A5B	<ol style="list-style-type: none"> Added 100K pulldown on J1 pin 4 to prevent crosstalk when serial cable is not connected into PCB layout. Changed the LED resistors to 4.75K to lower the brightness. 	5/21/2013	GC
A5C	<ol style="list-style-type: none"> Changed R46, R47, R48 to 0 ohms. Changed R45 to 22 Ohms. Change was made due to production failures on some boards due to differences in impedances.	6/12/2013	GC
A6	<ol style="list-style-type: none"> Moved the enable for the VDD_3V3B regulator to VDD_3V3A rail. Change was made to reduce the delay between the ramp up of the 3.3V rails. Added a AND gate to the SYS_RESETh circuitry. There is a small chance that on power up the nRESETOUT signal on the processor may go high, causing the SYS_RESETh signal to go HI before it should. This change reinforces the reset with the PORZn reset signal. Added optional zero ohm resistor to tie GND_OSC0 to system ground. 	7/25/2013	GC
A6A	<ol style="list-style-type: none"> Added optional zero ohm resistor to tie GND_OSC1 to system ground. Changed C106 to a 1uF capacitor. Changed C24 to a 2.2uF capacitor. Made R8 installed and R9 not installed. 	12/13/2013	GC
B	1.Changed the processor to the AM3358BZCZ100.	1/20/2014	GC
C	<ol style="list-style-type: none"> Changed eMMC into NAND Flash. Removed HDMI 	2/14/2019	GC

This schematic is ***NOT SUPPORTED*** and DOES NOT constitute a reference design. Only "community" support is allowed via resources at BeagleBoard.org/discuss.

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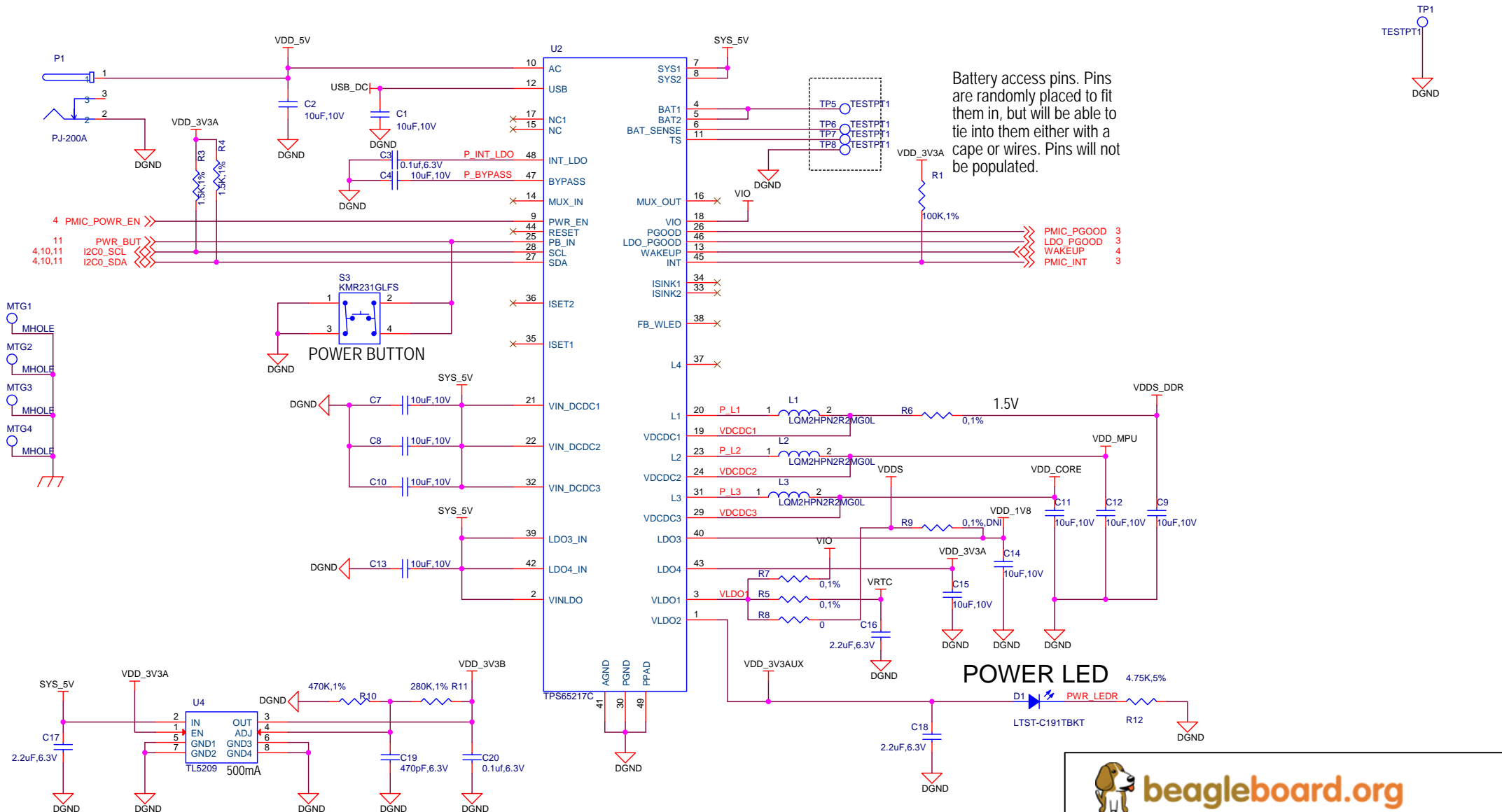
PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, UAB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	NAND FLASH
9	10/100 ETHERNET
10	EXP CONN, uSD

NOTE: PCB Revision for this board is Rev B6



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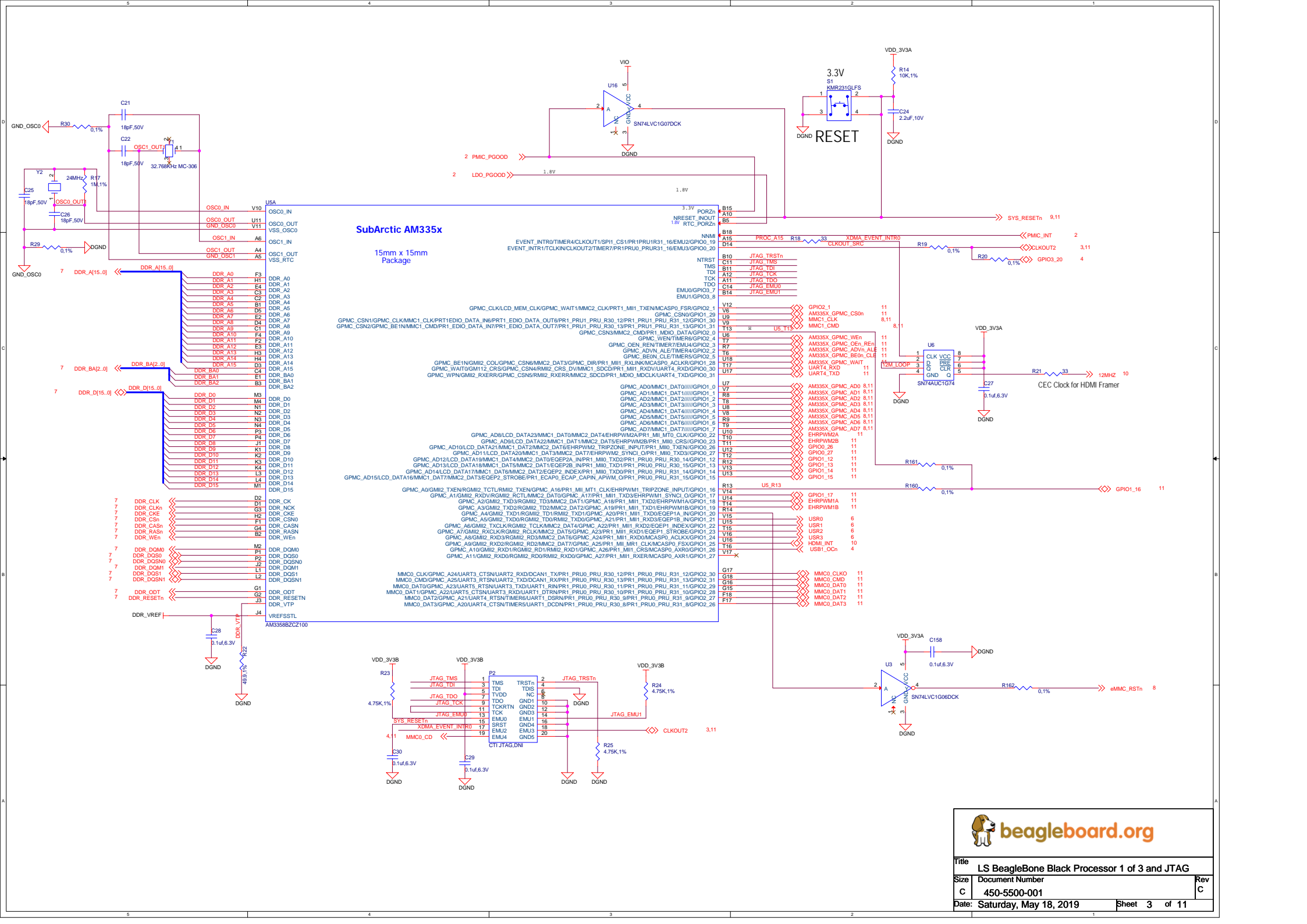
Title		LS BeagleBone Black Cover Page
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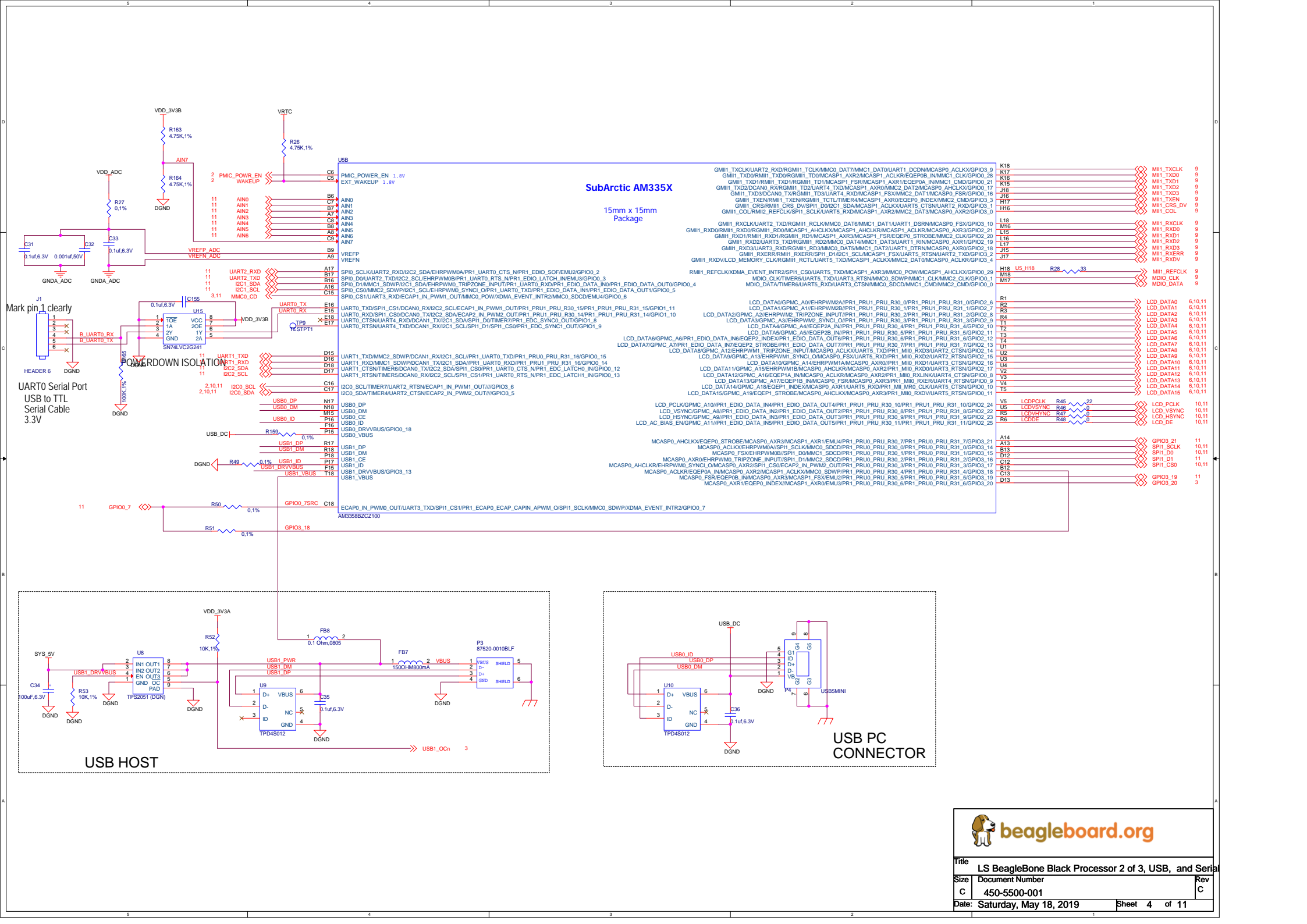


Battery access pins. Pins are randomly placed to fit them in, but will be able to tie into them either with a cape or wires. Pins will not be populated.



Title		
BeagleBone Black Power Management		
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SubArctic AM335X

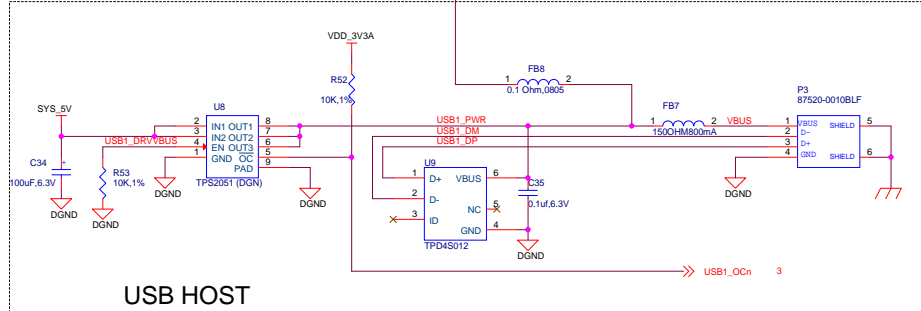
15mm x 15mm Package

11	AIN0	B6	AIN0
11	AIN1	B7	AIN1
11	AIN2	A7	AIN2
11	AIN3	C6	AIN3
11	AIN4	B8	AIN4
11	AIN5	B9	AIN5
11	AIN6	B5	AIN6
11	AIN7	A9	AIN7
11	UART2_RXD	A17	UART2_RXD
11	UART2_TXD	B17	UART2_TXD
11	I2C1_SDA	A16	I2C1_SDA
11	I2C1_SCL	C15	I2C1_SCL
11	MMIO_CD	3,11	MMIO_CD
11	UART1_TXD	E16	UART1_TXD
11	UART1_RXD	B17	UART1_RXD
11	I2C2_SDA	E18	I2C2_SDA
11	I2C2_SCL	X E18	I2C2_SCL
11	UART1_TXD	D15	UART1_TXD
11	UART1_RXD	D16	UART1_RXD
11	I2C2_SDA	D17	I2C2_SDA
11	I2C2_SCL	D17	I2C2_SCL
11	UART1_TXD	C16	UART1_TXD
11	UART1_RXD	C17	UART1_RXD
11	UART1_TXD	N17	UART1_TXD
11	UART1_RXD	N18	UART1_RXD
11	UART1_TXD	M15	UART1_TXD
11	UART1_RXD	M16	UART1_RXD
11	UART1_TXD	F16	UART1_TXD
11	UART1_RXD	F15	UART1_RXD
11	UART1_TXD	T18	UART1_TXD
11	UART1_RXD	T18	UART1_RXD
11	UART1_TXD	C18	UART1_TXD
11	UART1_RXD	C18	UART1_RXD
11	UART1_TXD	C18	UART1_TXD
11	UART1_RXD	C18	UART1_RXD

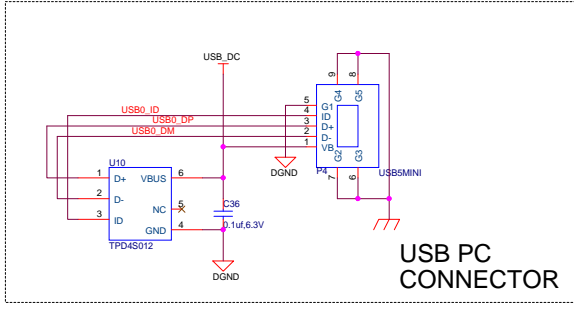
K18	MI1_TXCLK	9
K17	MI1_TXD0	9
K16	MI1_TXD1	9
K15	MI1_TXD2	9
J18	MI1_TXD3	9
J16	MI1_TXEN	9
H17	MI1_CRS_DV	9
H16	MI1_CCL	9
L18	MI1_RXCLK	9
M16	MI1_RXD0	9
L15	MI1_RXD1	9
L14	MI1_RXD2	9
L17	MI1_RXD3	9
J15	MI1_RXERR	9
J17	MI1_RXDV	9
H17	MI1_REFCLK	9
M18	MIO_CLK	9
M17	MIO_DATA	9
R1	LCD_DATA0	6,10,11
R2	LCD_DATA1	6,10,11
R3	LCD_DATA2	6,10,11
R4	LCD_DATA3	6,10,11
T1	LCD_DATA4	6,10,11
T2	LCD_DATA5	6,10,11
T3	LCD_DATA6	6,10,11
U1	LCD_DATA7	6,10,11
U2	LCD_DATA8	6,10,11
U3	LCD_DATA9	6,10,11
U4	LCD_DATA10	6,10,11
U5	LCD_DATA11	6,10,11
V4	LCD_DATA12	6,10,11
V5	LCD_DATA13	6,10,11
T5	LCD_DATA14	6,10,11
T6	LCD_DATA15	6,10,11
V5	LCD_PCLK	10,11
U5	LCD_VSYNC	10,11
R5	LCD_VSYNC	10,11
R6	LCD_DE	10,11
A14	GPIO3_21	11
A13	SPH1_SCLK	10,11
D12	SPH1_D0	10,11
C12	SPH1_D1	10,11
B12	SPH1_CS0	10,11
C13	GPIO3_19	11
D13	GPIO3_20	3

Mark pin 1 clearly

UART0 Serial Port
USB to TTL
Serial Cable
3.3V



USB HOST



USB PC CONNECTOR

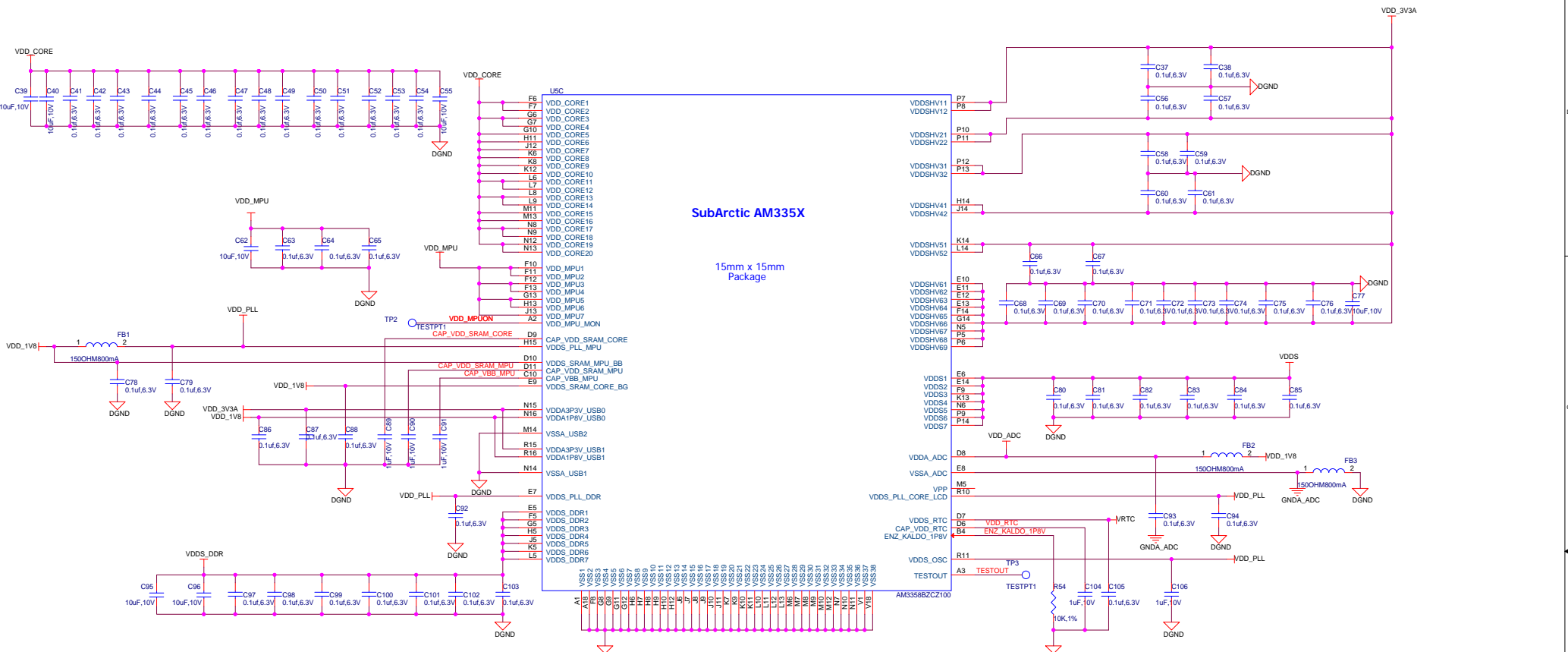
Title: **LS BeagleBone Black Processor 2 of 3, USB, and Serial**

Size: Document Number


C: 450-5500-001

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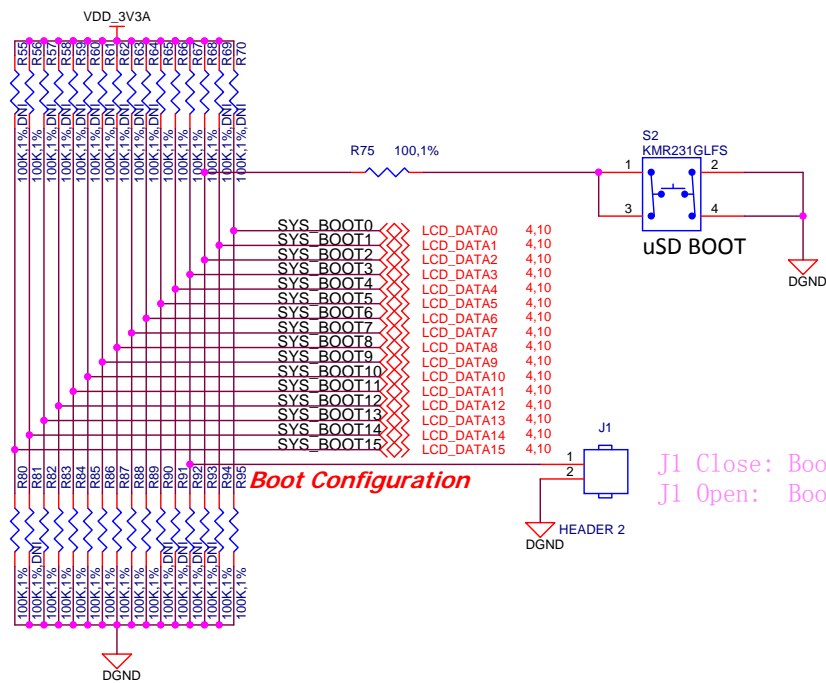


SubArctic AM335X
15mm x 15mm Package



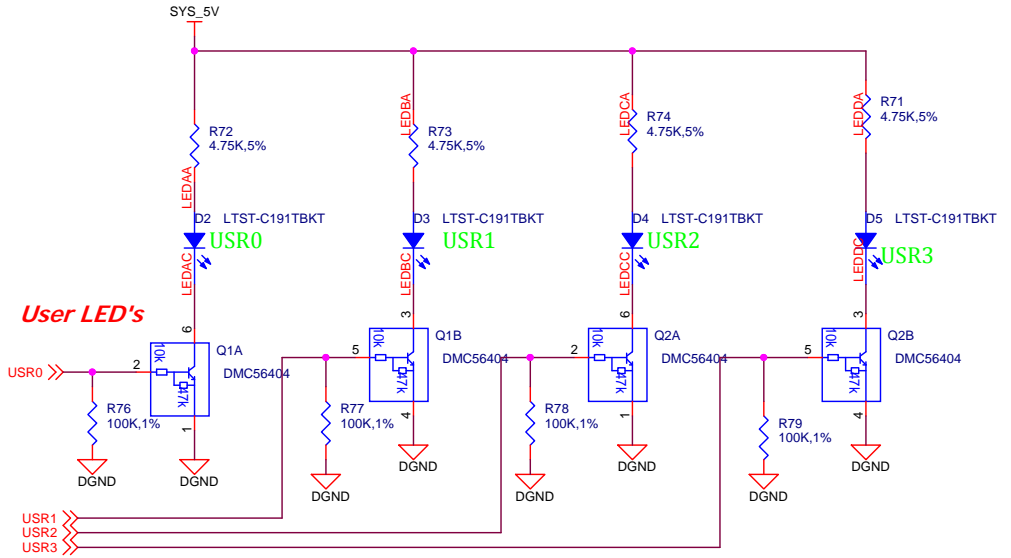
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Title	LS BeagleBone Black Process 3 of 3	
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Boot Configuration

J1 Close: Boot from microSD
 J1 Open: Boot from Nand flash



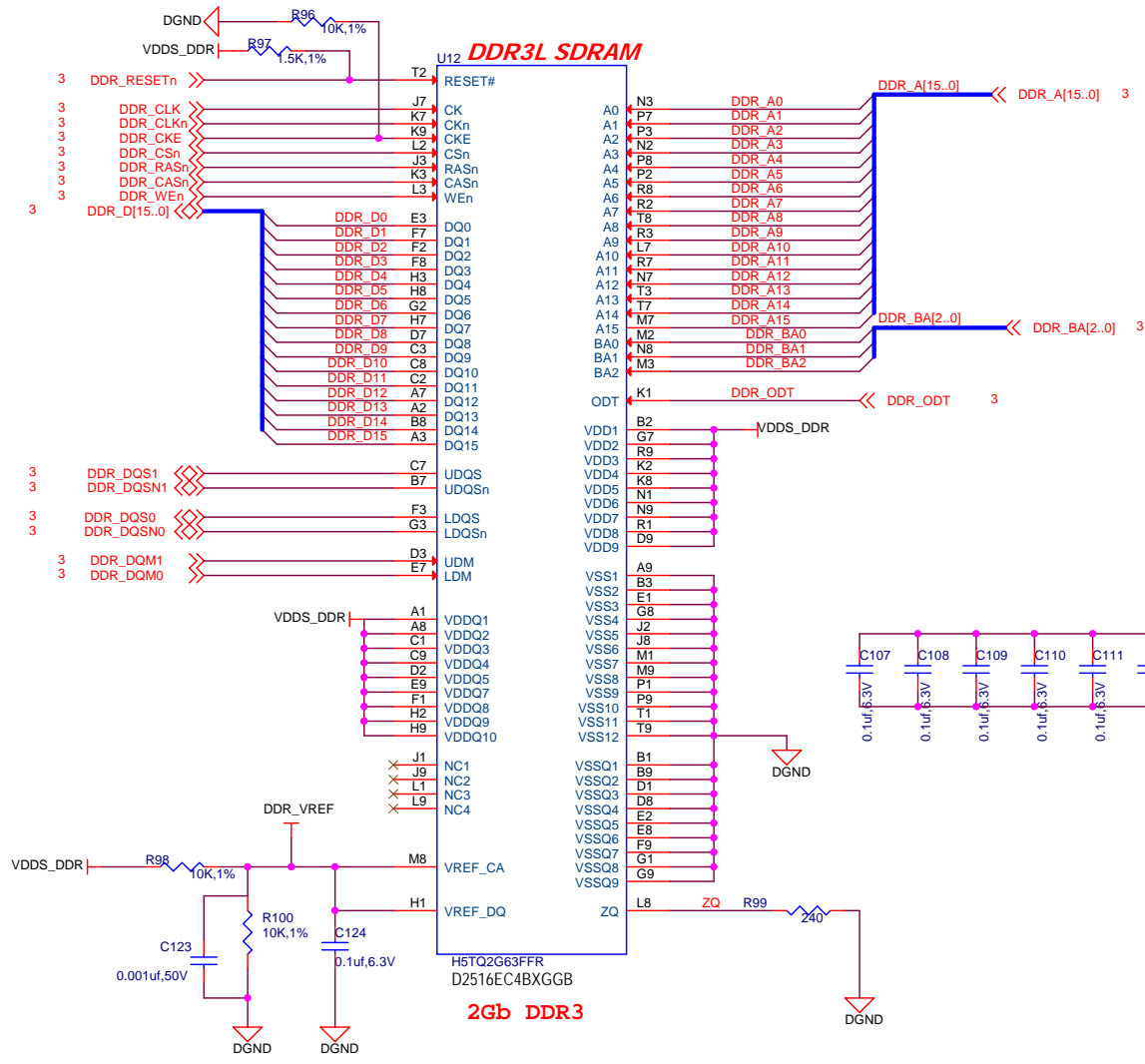
User LED's

SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5] 1	UART0



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Title		LS BeagleBone Black LED, Configuration, and Reset
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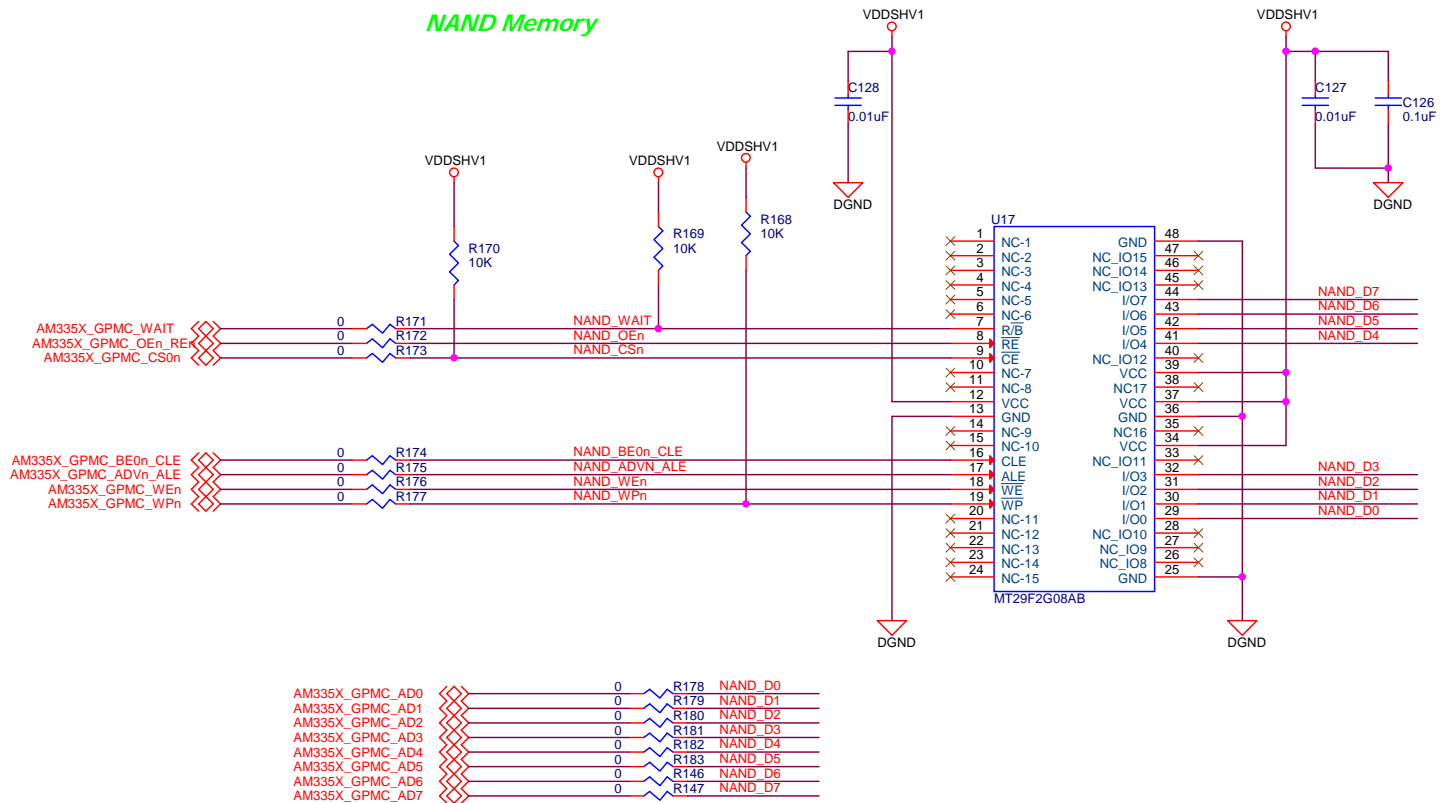
DDR3L SDRAM

2Gb DDR3



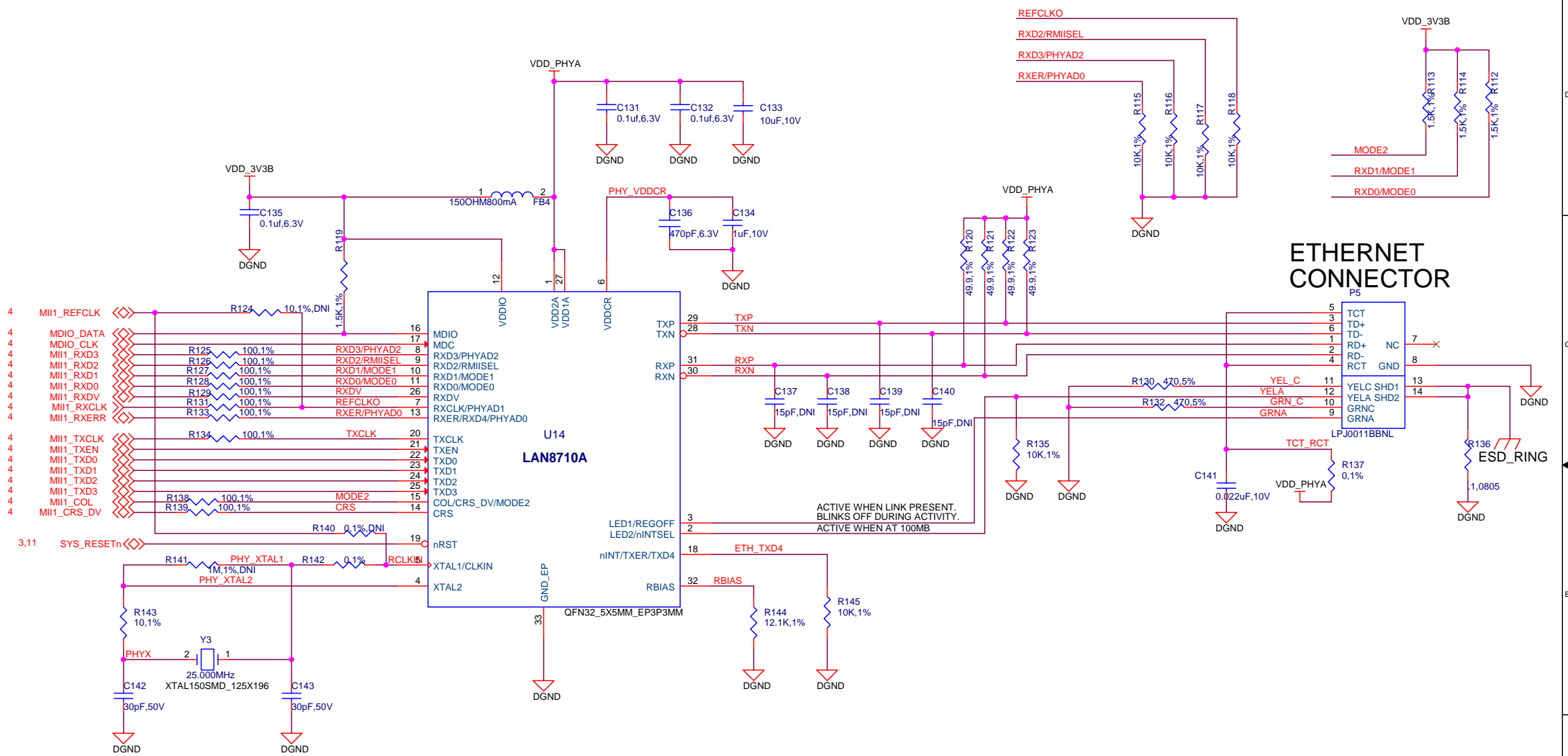
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BeagleBone Black DDR3 Memory		
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NAND Memory

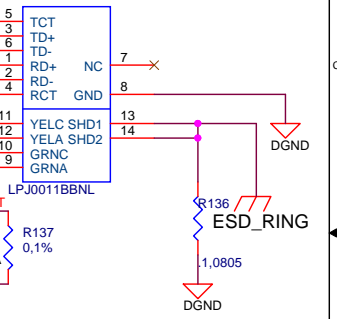


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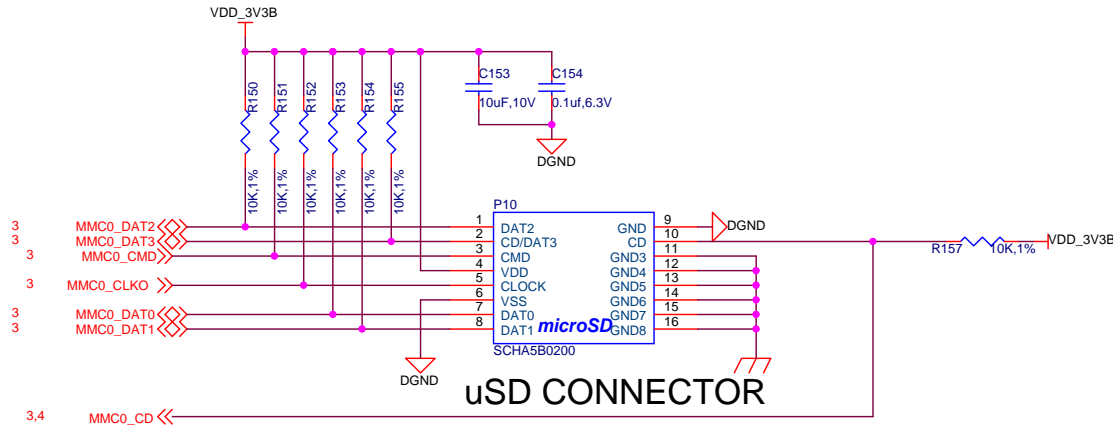
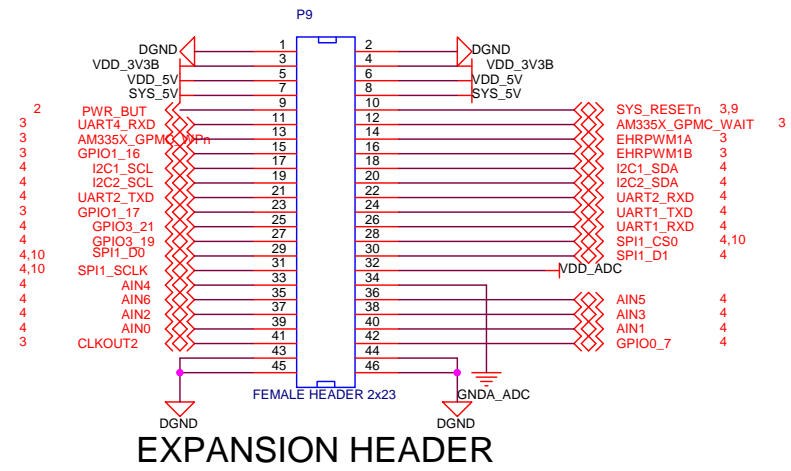
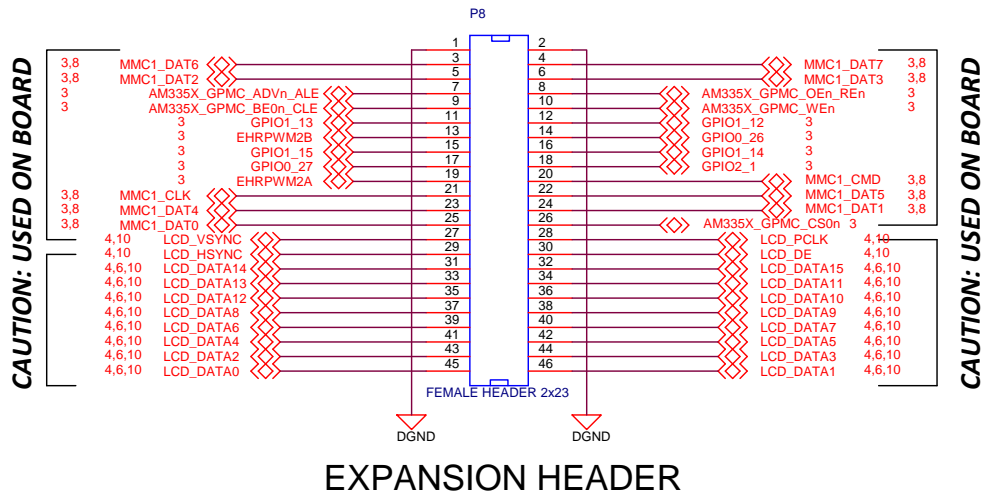
Title		LS Beagle BoneBlack NAND
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ETHERNET CONNECTOR



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Title
LS BeagleBone Black Expansion Headers, uSDX

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