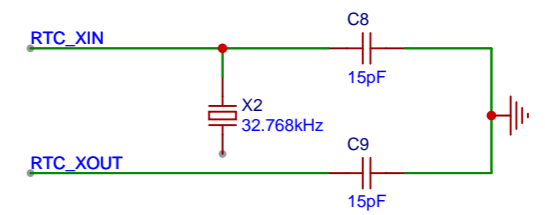
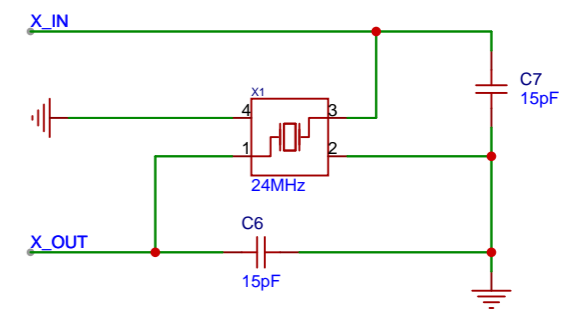
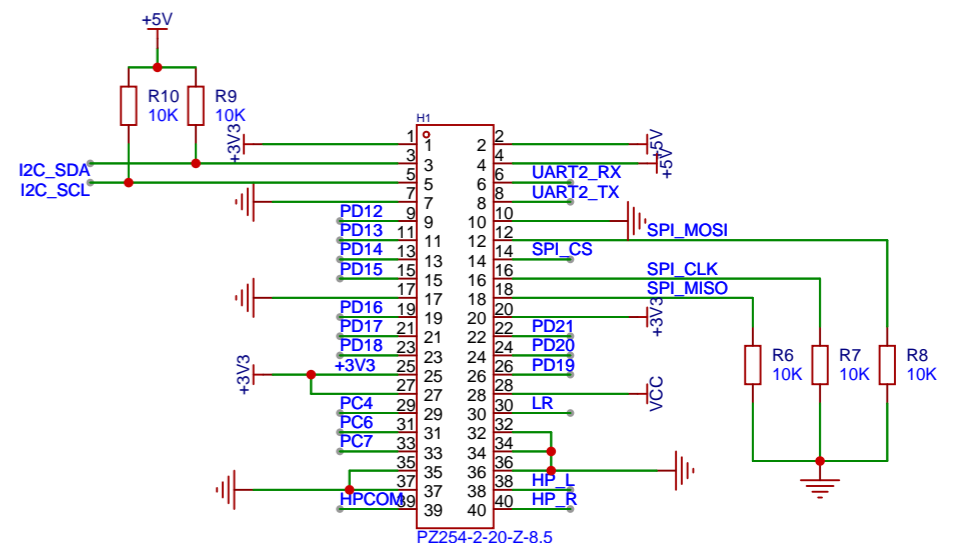
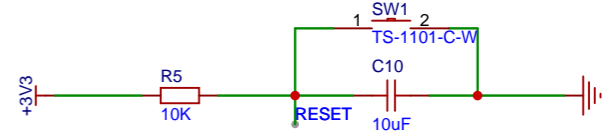


CORE



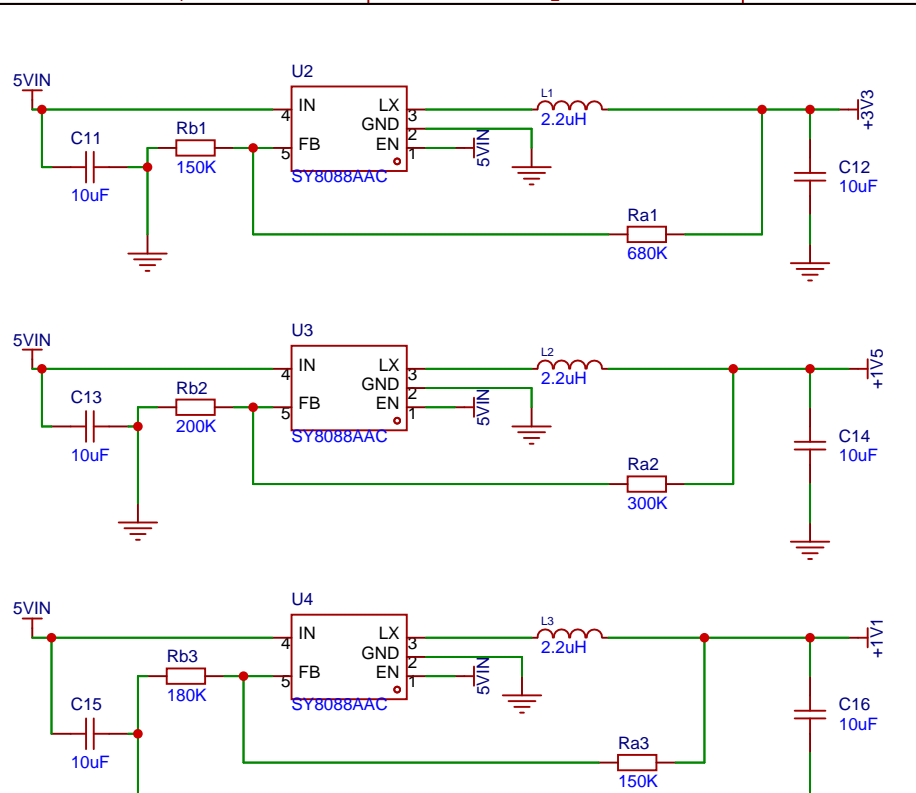
TIME&RESET



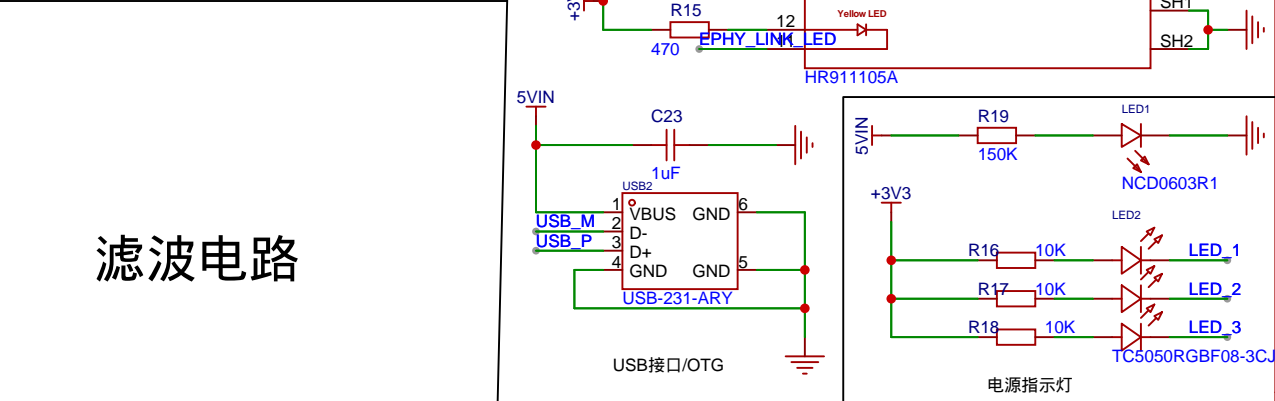
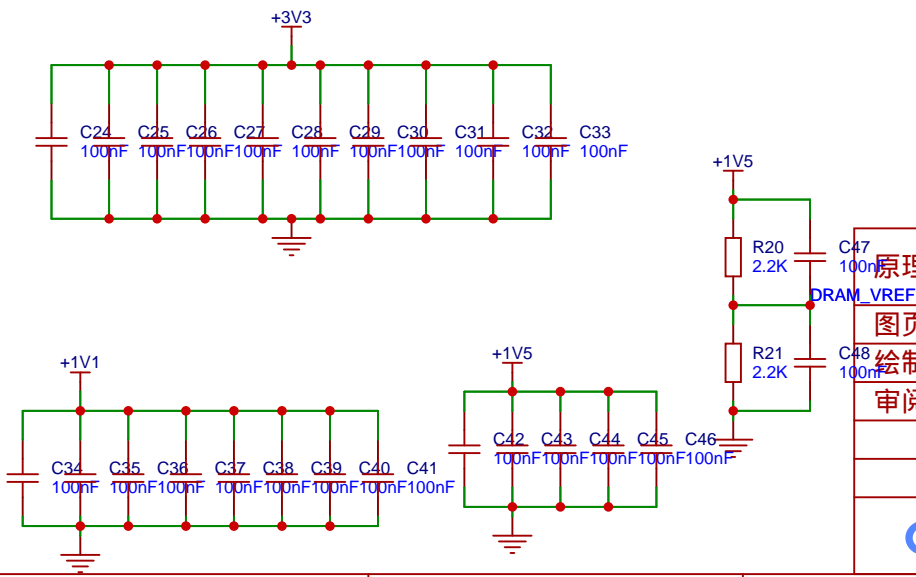
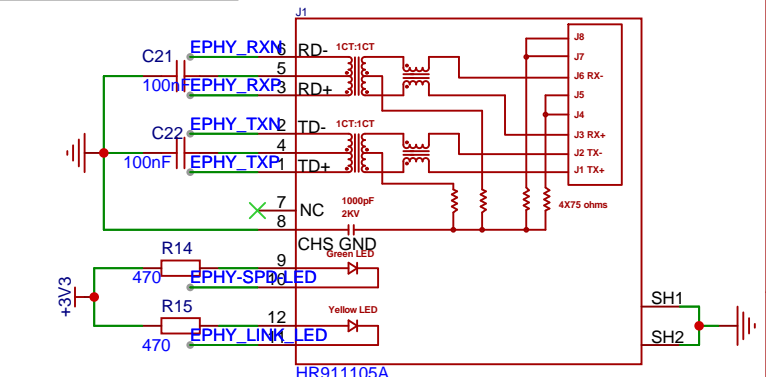
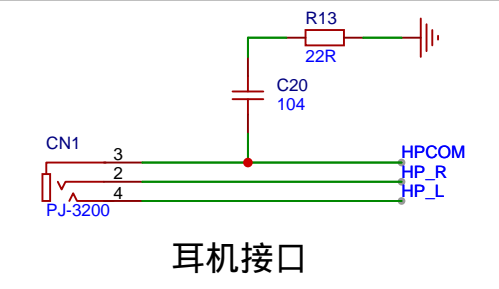
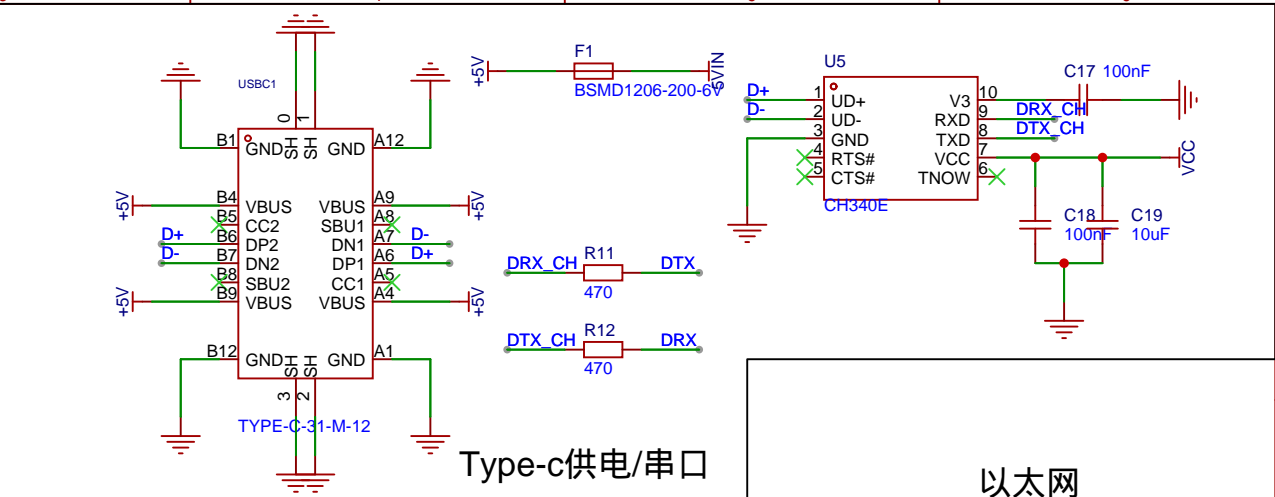
外接IO

原理图	Schematic1		更新日期	2023-10-13
图页	Core.Schematic1		创建日期	2023-10-09
绘制			物料编码	
审阅			全志V3X_xcy	
			版本	尺寸
			V1.0	A4
			页	1 共 3
嘉立创EDA			嘉立创EDA	



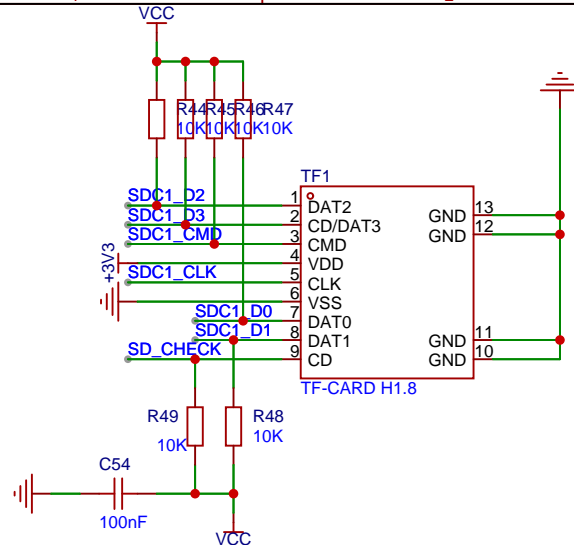


$V_{out} = 0.6 \cdot (1 + R_a/R_b)$
电源管理

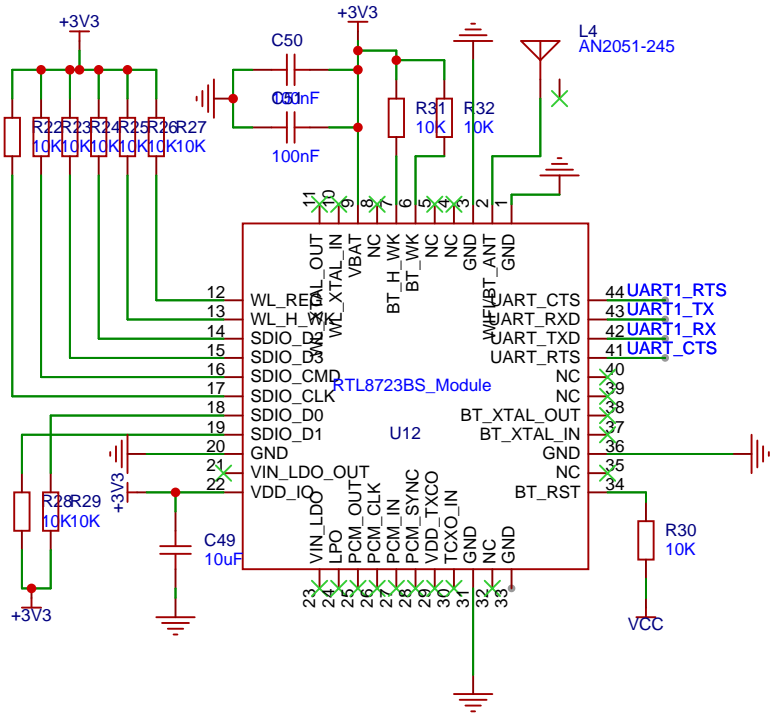


原理图	Schematic1		更新日期	2023-10-13
图页	PERI.Schematic1		创建日期	2023-10-10
绘制			物料编码	
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		V1.0	A4	嘉立创EDA

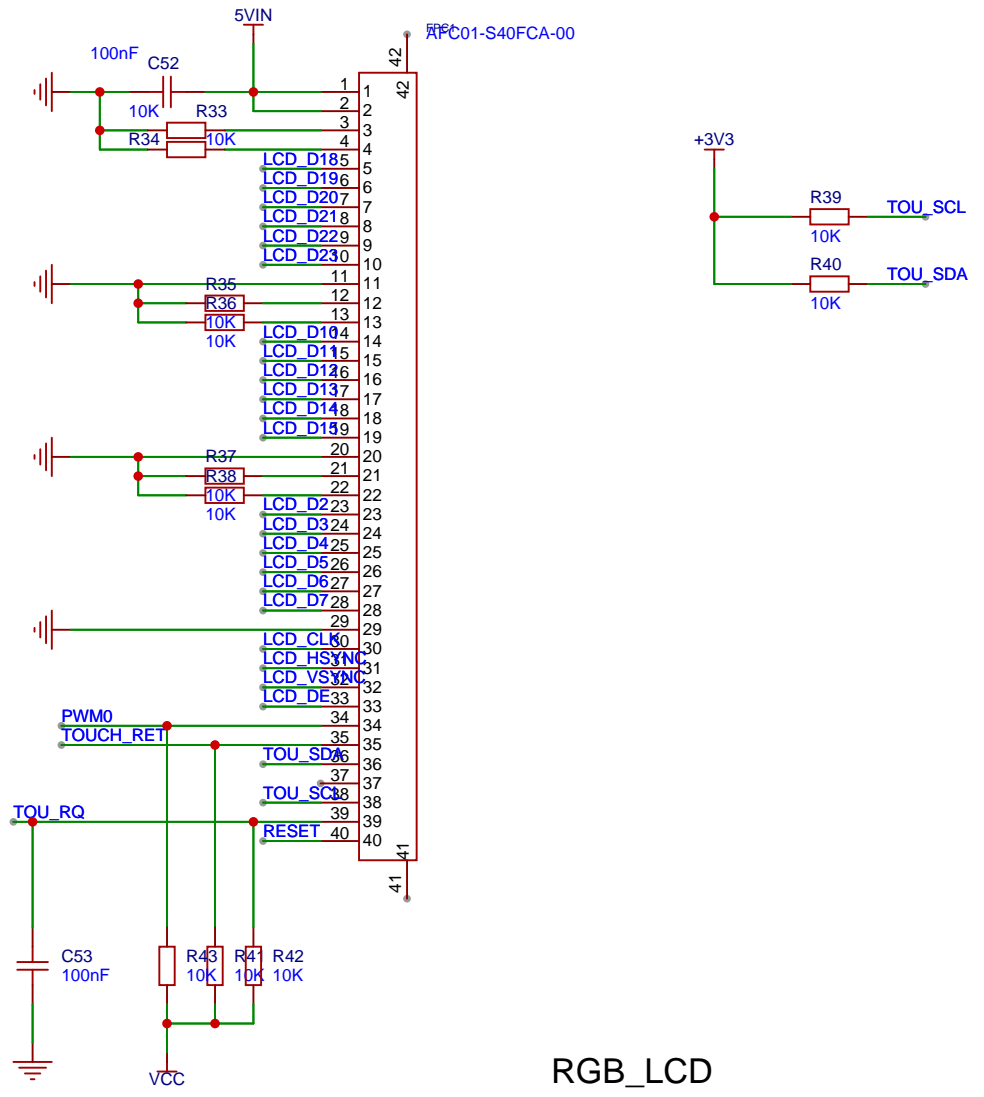




SD_Card



RTL8723bs_module



RGB_LCD

原理图	Schematic1		更新日期	2023-10-13
图页	TF/LCD.Schematic1		创建日期	2023-10-10
绘制			物料编码	
审阅			全志V3X_xcy	
	版本	尺寸	页	3 共 3
嘉立创EDA		V1.0	A4	嘉立创EDA