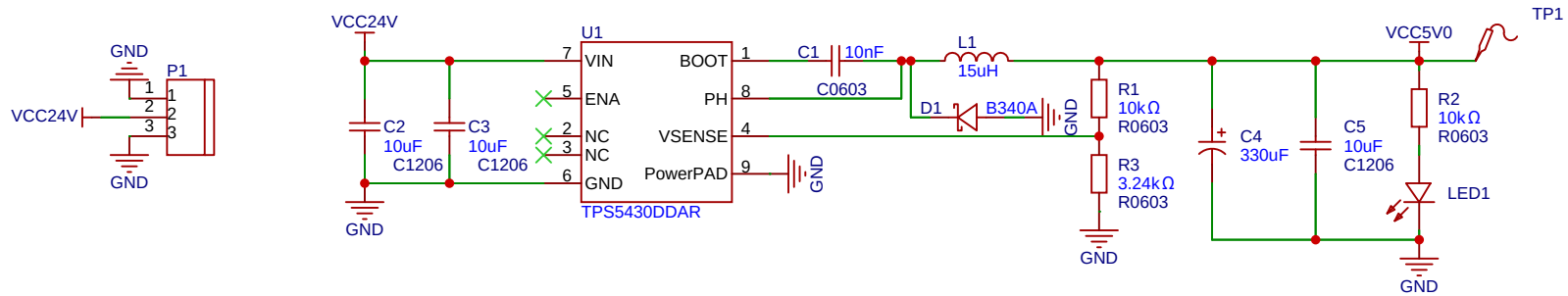

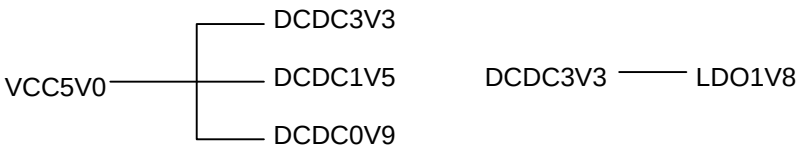

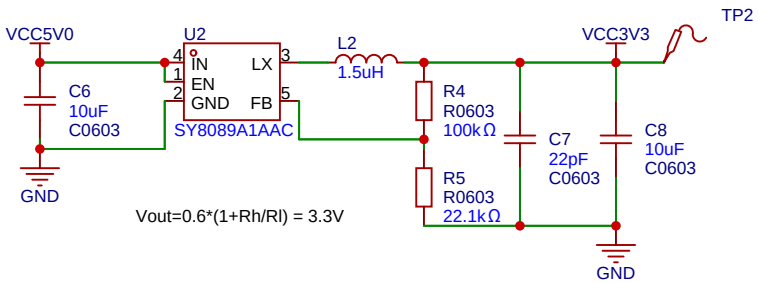

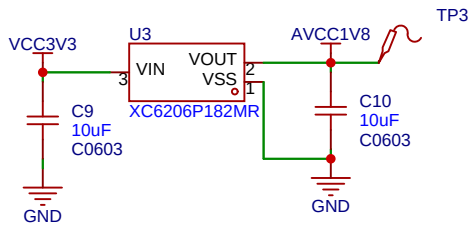

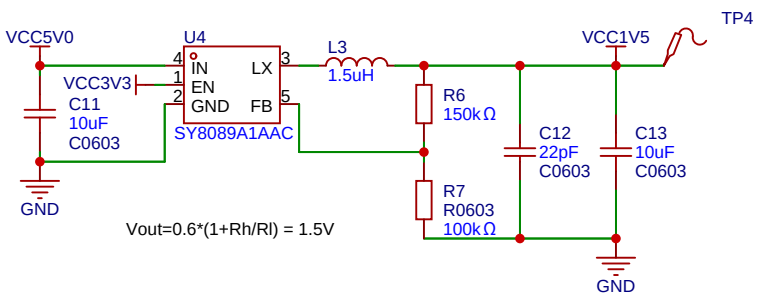

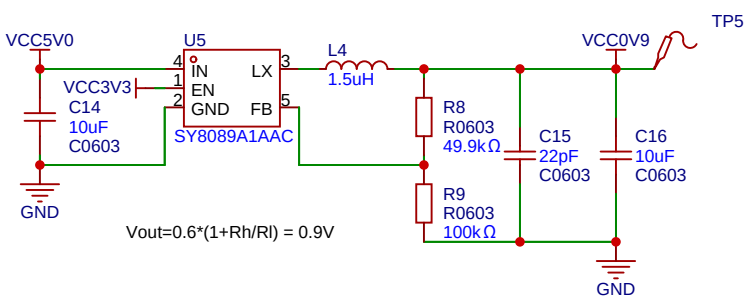

电源域

VCC3V3——VCC-PE——VCC-PG——VCC-PD——VCC-IO——VCC-TVOUT——LDO-IN

VCC0V9——VDD-CORE——VDD-SYS

LDO1V8——VCC-RTC——VCC-PLL——VCC-LVDS——VDD18-DRAM——LDOA_OUT

VCC1V5——VCC-DRAM

AVCC1V8——AVCC——HPVCC——VCC-TVIN

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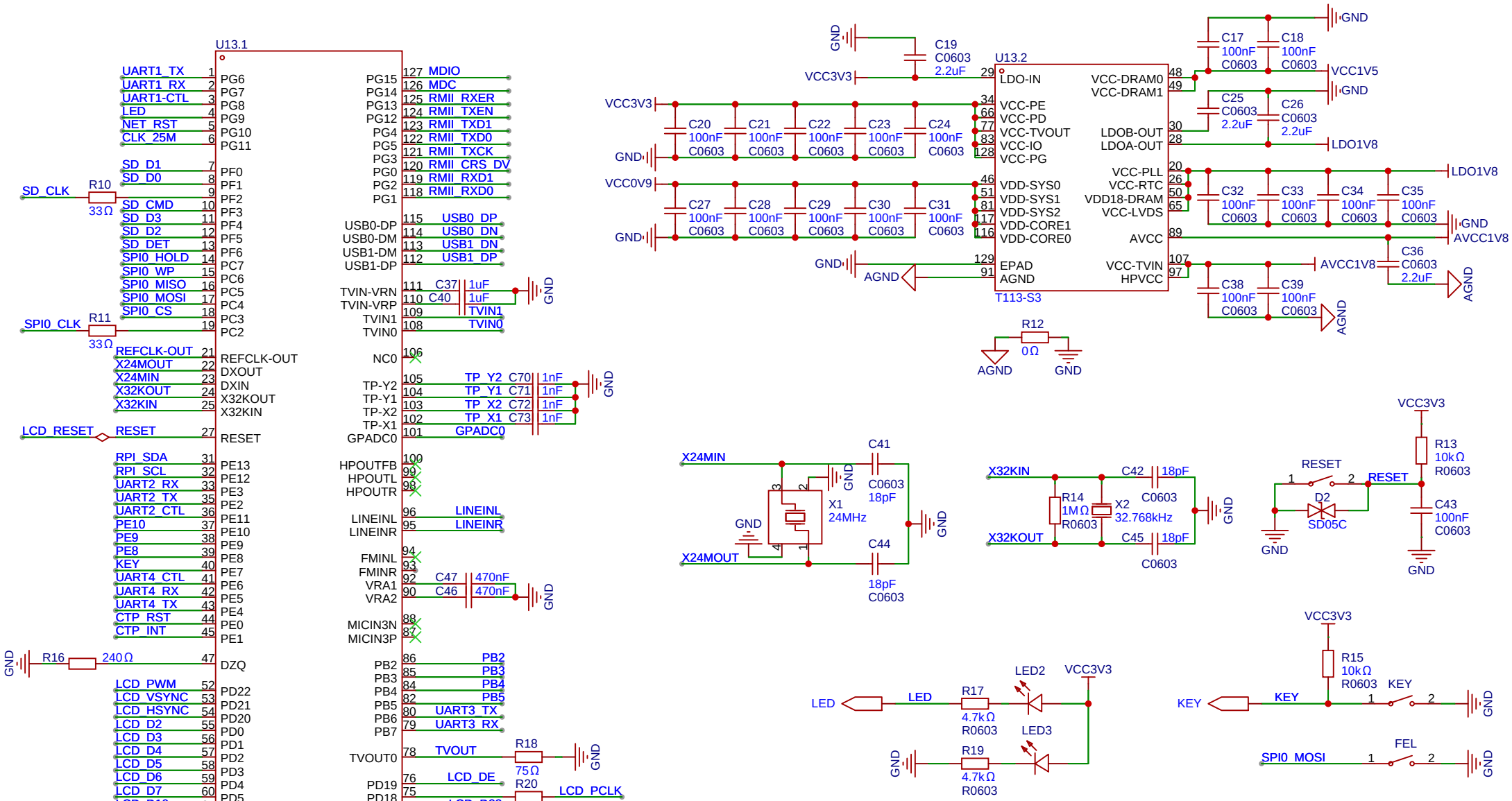
U13.1
T113-S3
U13.2
T113-S3
UART1_TX
UART1_RX
UART1-CTL
LED
NET_RST
CLK_25M
SD_D1
SD_D0
SD_CLK
R10
33Ω
SD_CMD
SD_D3
SD_D2
SD_DET
SPI0_HOLD
SPI0_WP
SPI0_MISO
SPI0_MOSI
SPI0_CS
SPI0_CLK
R11
33Ω
REFCLK-OUT
X24MOUT
X24MIN
X32KOUT
X32KIN
LCD_RESET
RESET
RPI_SDA
RPI_SCL
UART2_RX
UART2_TX
UART2_CTL
PE10
PE9
PE8
KEY
UART4_CTL
UART4_RX
UART4_TX
CTP_RST
CTP_INT
GND
R16
240Ω
DZQ
LCD_PWM
LCD_VSYNC
LCD_HSYNC
LCD_D2
LCD_D3
LCD_D4
LCD_D5
LCD_D6
LCD_D7
LCD_D10
LCD_D11
LCD_D12
LCD_D13
PG6
PG7
PG8
PG9
PG10
PG11
PF0
PF1
PF2
PF3
PF4
PF5
PF6
PC7
PC6
PC5
PC4
PC3
PC2
REFCLK-OUT
DXOUT
DXIN
X32KOUT
X32KIN
RESET
PE13
PE12
PE3
PE2
PE11
PE10
PE9
PE8
PE7
PE6
PE5
PE4
PE0
PE1
DZQ
PD22
PD21
PD20
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PD8
PD9
PG15
PG14
PG13
PG12
PG4
PG5
PG3
PG0
PG2
PG1
USB0-DP
USB0-DM
USB1-DM
USB1-DP
TVIN-VRN
TVIN-VRP
TVIN1
TVIN0
NC0
TP-Y2
TP-Y1
TP-X2
TP-X1
GPADC0
HPOUTFB
HPOUTL
HPOUTR
LINEINL
LINEINR
FMINL
FMINR
VRA1
VRA2
MICIN3N
MICIN3P
PB2
PB3
PB4
PB5
PB6
PB7
TVOUT0
PD19
PD18
PD17
PD16
PD15
PD14
PD12
PD13
PD11
PD10
MDIO
MDC
RMII_RXER
RMII_TXEN
RMII_TXD1
RMII_TXD0
RMII_TXCK
RMII_CRS_DV
RMII_RXD1
RMII_RXD0
USB0_DP
USB0_DN
USB1_DN
USB1_DP
C37
1uF
C40
1uF
TVIN1
TVIN0
TP_Y2
C70
1nF
TP_Y1
C71
1nF
TP_X2
C72
1nF
TP_X1
C73
1nF
GPADC0
LINEINL
LINEINR
C47
470nF
C46
470nF
UART3_TX
UART3_RX
R18
75Ω
TVOUT
LCD_DE
R20
33Ω
LCD_PCLK
LCD_D23
LCD_D22
LCD_D21
LCD_D20
LCD_D18
LCD_D19
LCD_D15
LCD_D14
GND
C19
C0603
2.2uF
VCC3V3
C20
C21
C22
C23
C24
100nF
C0603
VCC0V9
C27
C28
C29
C30
C31
AGND
LDO-IN
VCC-PE
VCC-PD
VCC-TVOUT
VCC-IO
VCC-PG
VDD-SYS0
VDD-SYS1
VDD-SYS2
VDD-CORE1
VDD-CORE0
EPAD
AGND
T113-S3
R12
0Ω
VCC-DRAM0
VCC-DRAM1
LDOB-OUT
LDOA-OUT
VCC-PLL
VCC-RTC
VDD18-DRAM
VCC-LVDS
AVCC
VCC-TVIN
HPVCC
C17
C18
C25
C26
2.2uF
VCC1V5
LDO1V8
C32
C33
C34
C35
C36
AVCC1V8
C38
C39
X24MIN
X24MOUT
C41
C44
18pF
X1
24MHz
X32KIN
X32KOUT
C42
C45
R14
1MΩ
R0603
X2
32.768kHz
RESET
D2
SD05C
R13
10kΩ
C43
LED
LED2
LED3
R17
4.7kΩ
R19
KEY
R15
FEL
SPI0_MOSI
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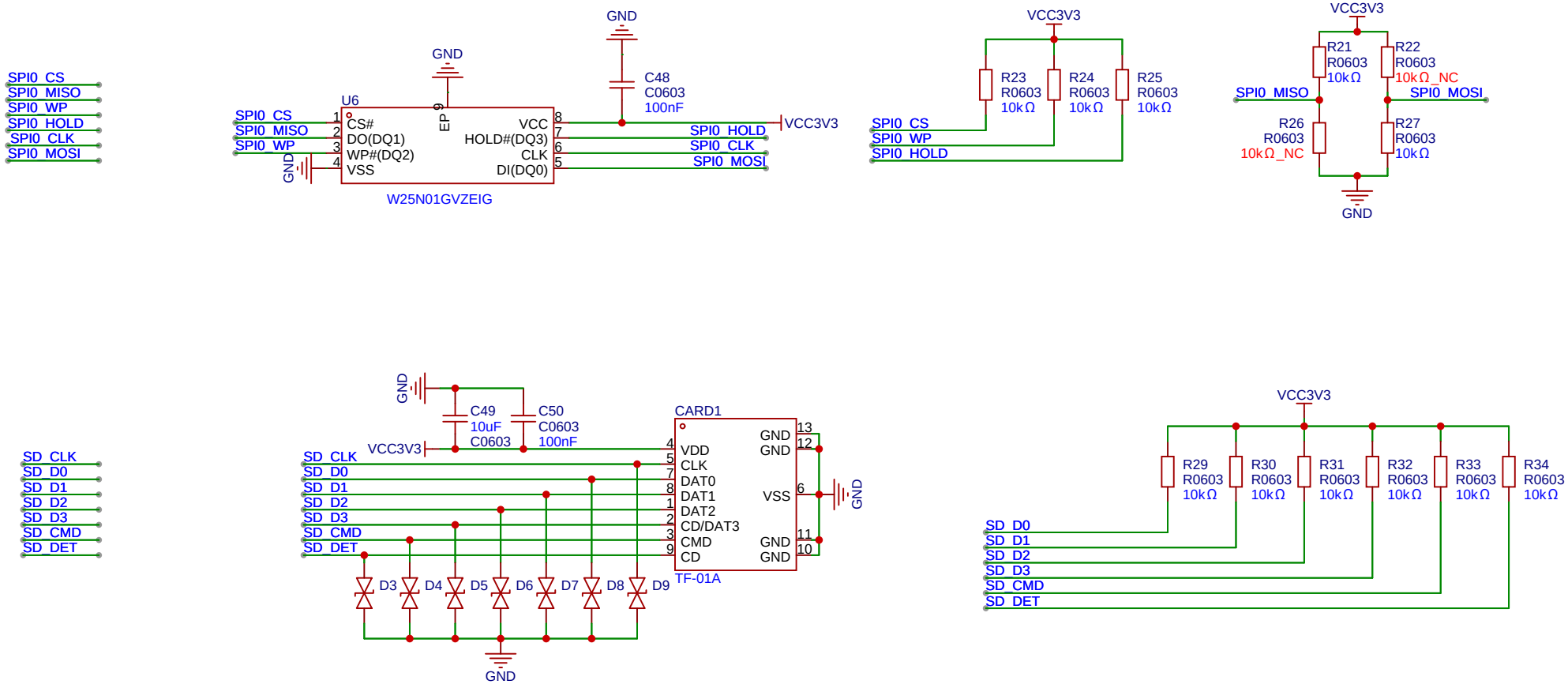

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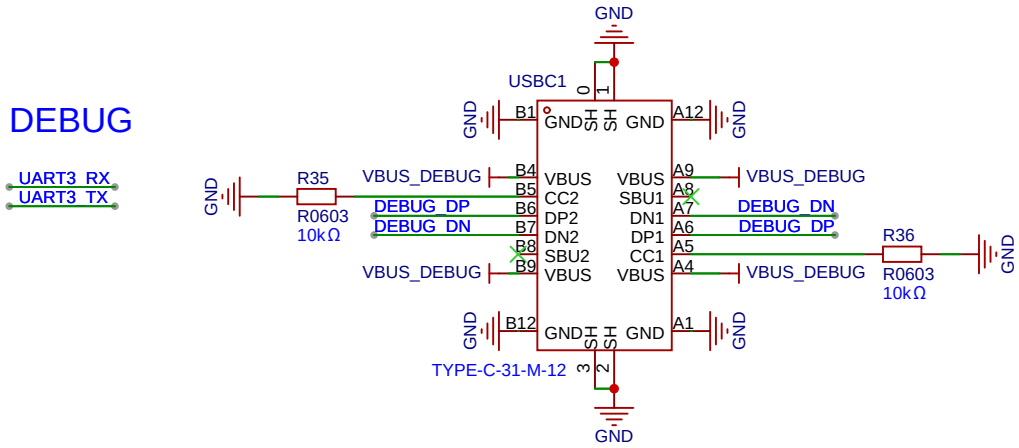
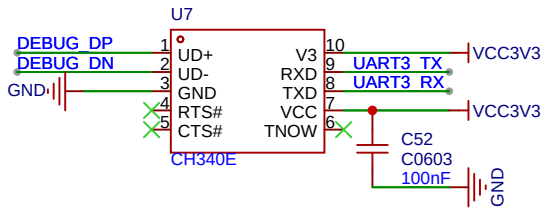
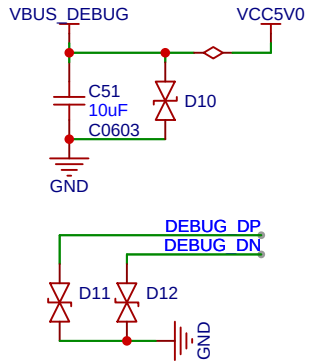
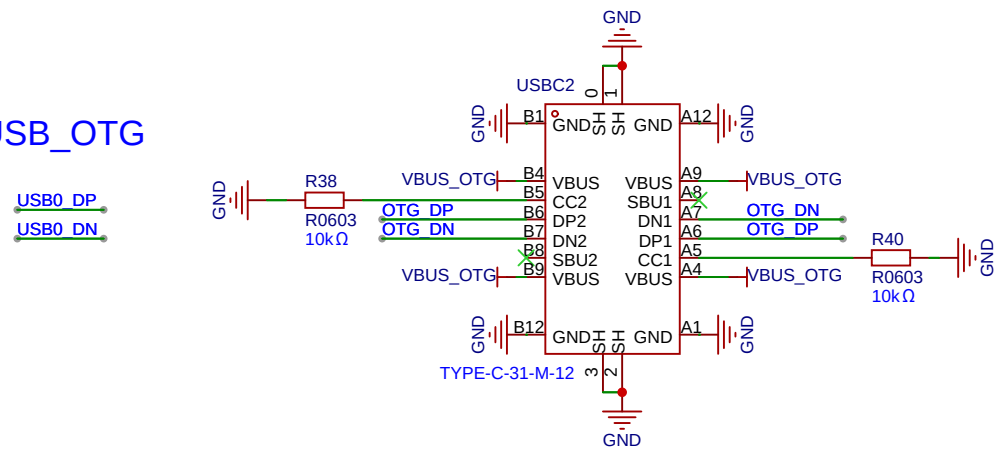
DEBUG

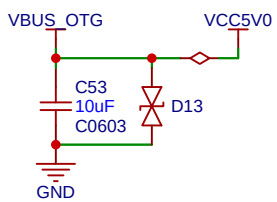


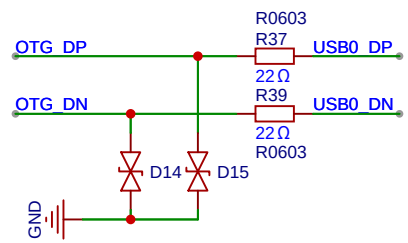




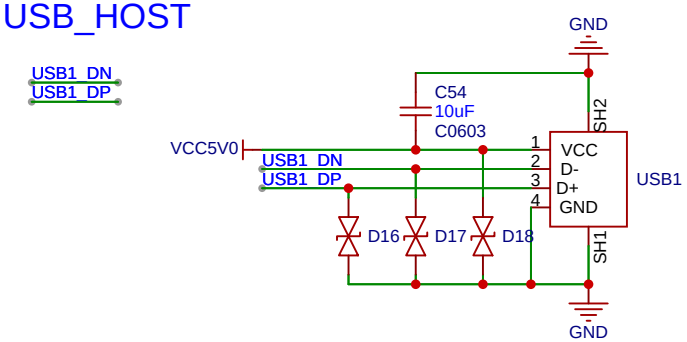
USB_OTG







USB_HOST



原理图	Schematic1	更新日期	2024-02-29
		创建日期	2024-02-27
图页	USB.Schematic1	物料编码	
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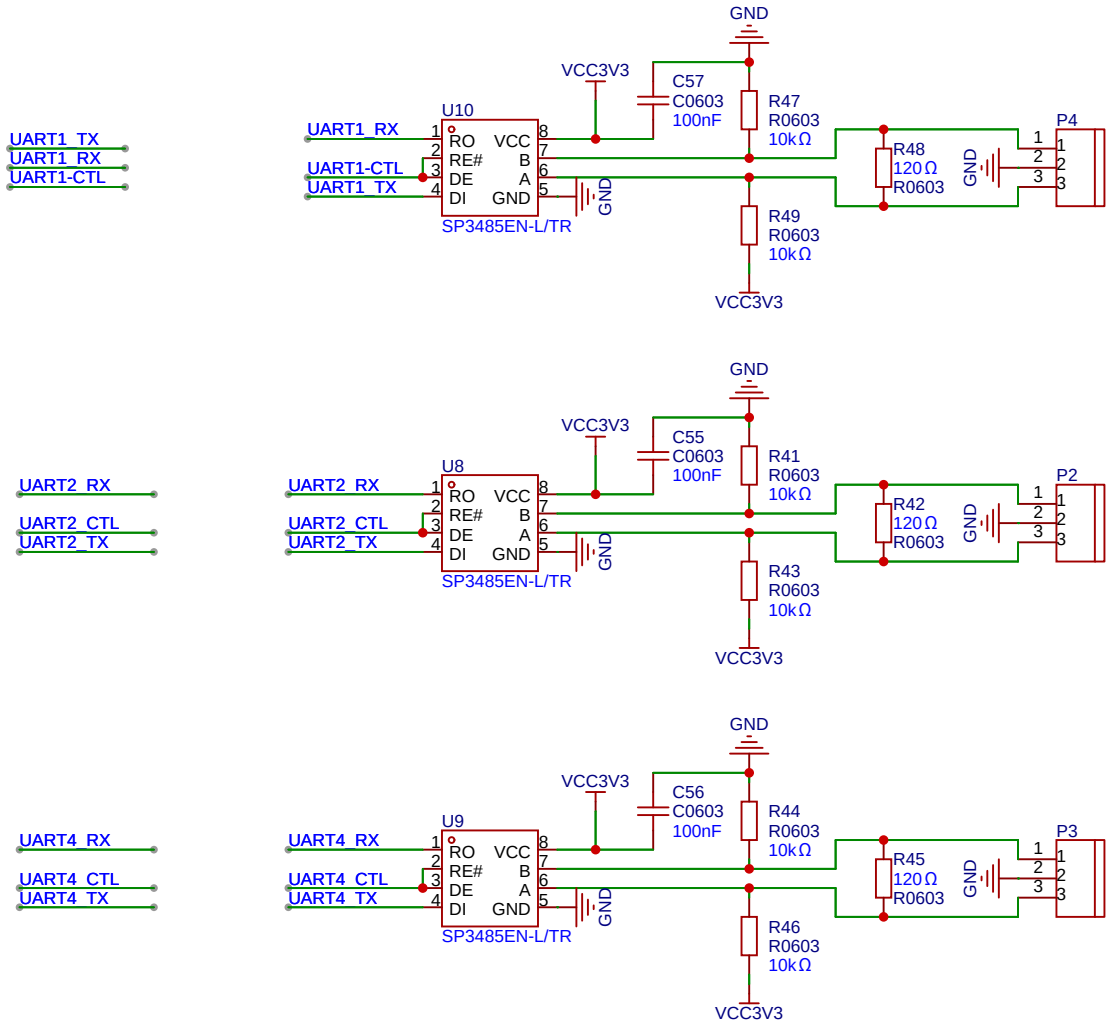

原理图	Schematic1	更新日期	2024-02-29
		创建日期	2024-02-27
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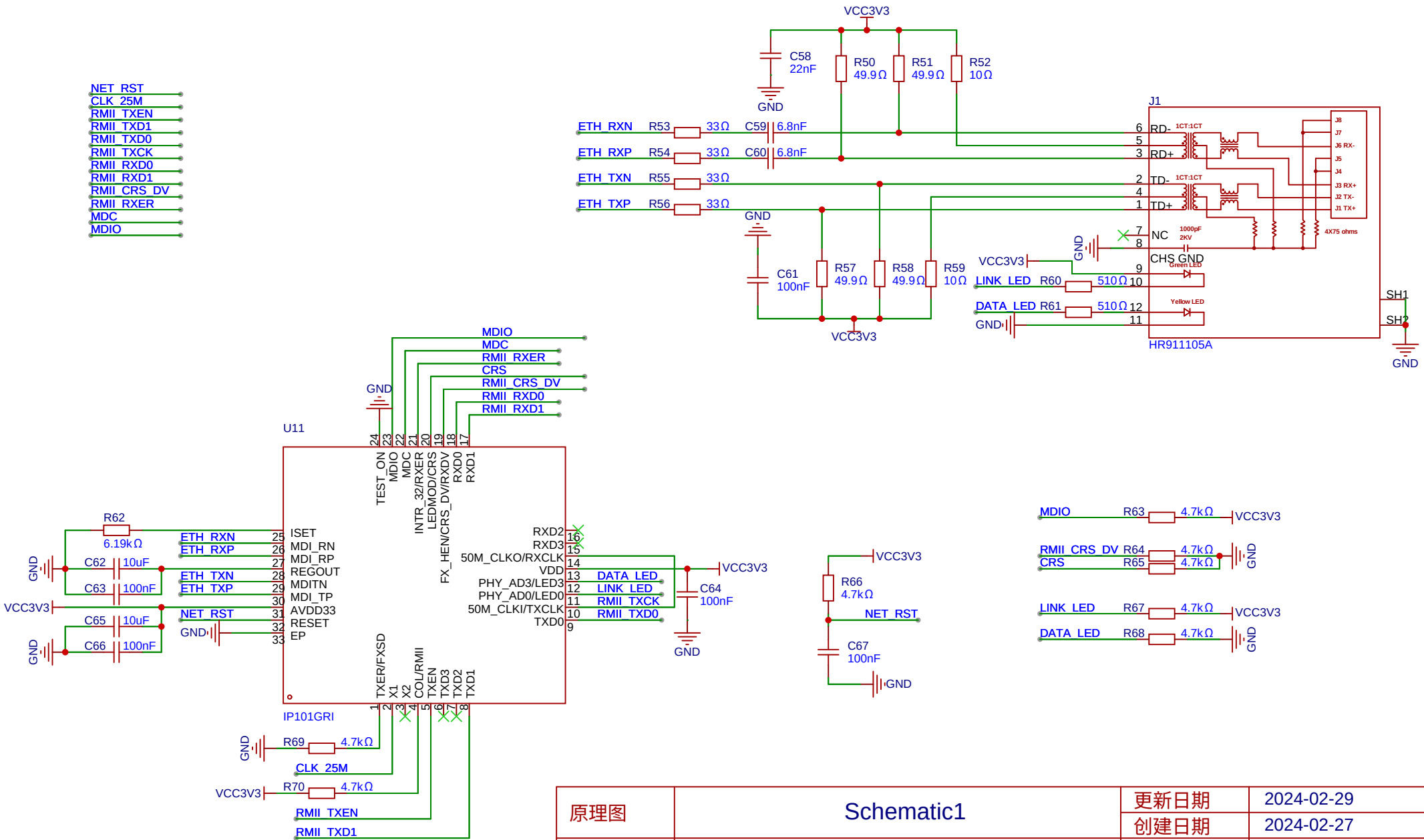

原理图	Schematic1	更新日期	2024-02-29
		创建日期	2024-02-27
图页	PHY.Schematic1	物料编码	
绘制			
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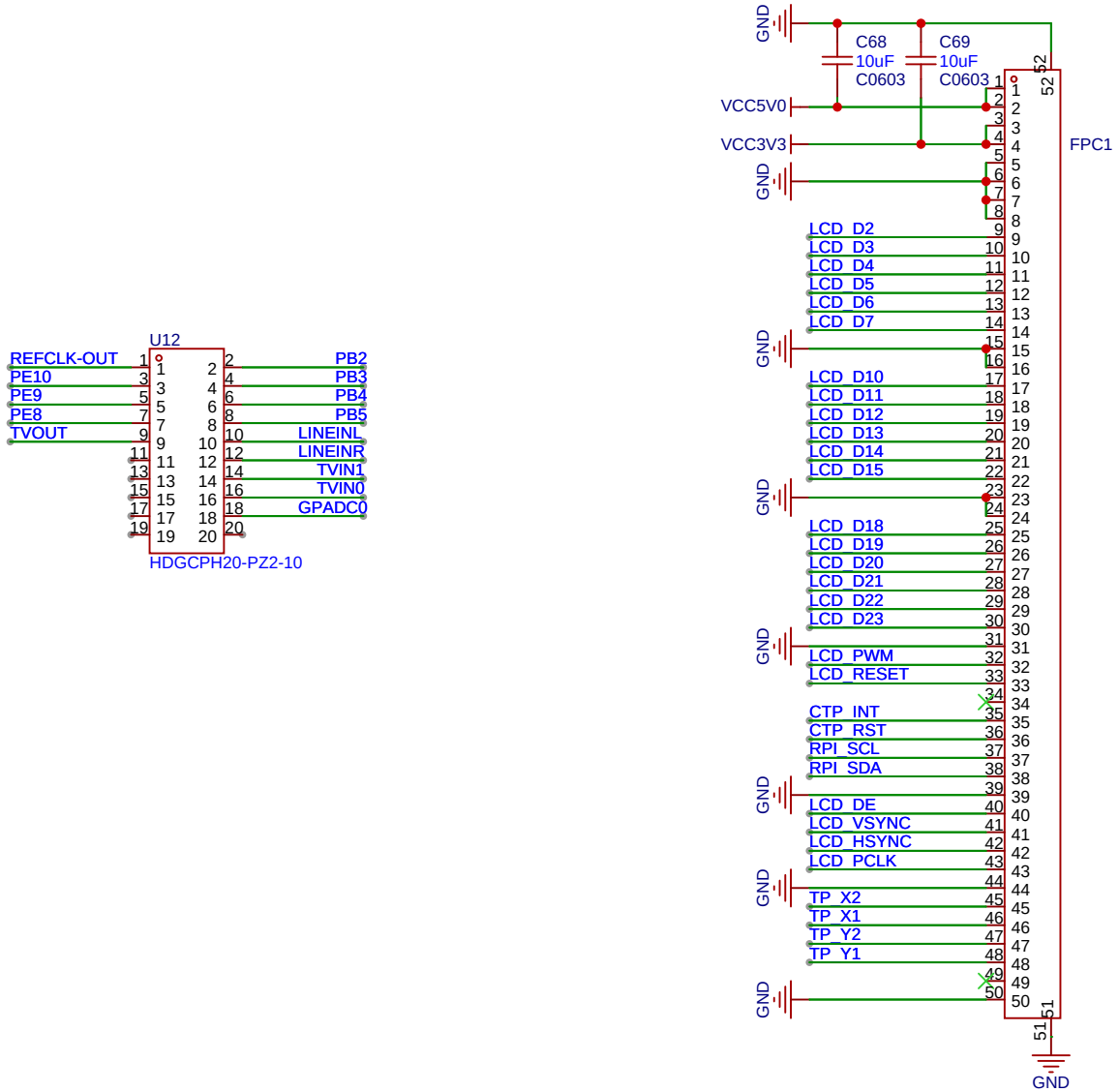
嘉立创EDA		V1.0	A4	嘉立创EDA



原理图	Schematic1	更新日期	2024-02-29
		创建日期	2024-02-29
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绘制		T113网关方案	
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