POLLUX Data Sheet

POLLUX

Data Sheet

MDPOLLUXDS
Ver Preliminary 0.90 / Dec 5, 2007
POLLUX
Data Sheet for POLLUX Application Processor

Preliminary

Release Version 0.90

Document Release
2007/ 12/ 5

Important Notice

Information in this document is provided solely to enable system and software implementers to use MagicEyes products. MagicEyes have checked the information in this document carefully and believe the accuracy. However MagicEyes assumes no responsibility for possible errors or omissions herein.

MagicEyes reserves the right to make changes in its products or product specifications at anytime without notice and is not required to update this documentation to reflect such changes.

MagicEyes makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does MagicEyes assumes any liability arising out of the application or use of any product or circuit and specifically disclaims any and all liability, including without limitation consequential or incidental damages.

"Typical" parameters which may be provided in this documents can and do vary in different application. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts.

MagicEyes does not convey any license under its patent rights nor the rights of others. MagicEyes products are not designed, intended, or authorized for use as components in system intended for surgical implant into the body, for other applications intended to support or sustain life, or for any other application in which the failure of the MagicEyes product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use a MagicEyes product for any such unintended or unauthorized application, the Buyer shall indemnify and hold MagicEyes and its officers, employees, subsidiaries, affiliates and distributors harmless against all claims, costs, damages, expenses and reasonable attorney fees arising out of, either directly or indirectly, any claim or personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that MagicEyes was negligent regarding the design or manufacture of said product.

HOW TO REACH US:
MagicEyes Digital Co., Ltd.
463-824, Uniquest BD 4F, 271-2 Seohyeon-Dong, Bundang-Gu Seongnam-City, Gyeonggi-Do, Korea
TEL : 82-31-788-0300
FAX : 82-31-707-5765

HOME PAGE:
http://www.mesdigital.com

UPDATE HISTORY

Ver 0.80 : First release

Ver 0.81 : 2007/10/2

- **Chapter 1.**
  - 1.2 Functional Specification → Add
    - 1.2.21 IDCT (Inverse Discrete Cosine Transform)

CHAPTER 1.

INTRODUCTION

1. Introduction

1.1. Overview

This document describes the POLLUX 32bit RISC Processor developed by MagicEyes Digital Co., Ltd. POLLUX is a complete product designed for Handheld, Low Cost and Low Power Consumption products.

POLLUX incorporates a 32bit CPU Processor, 3D Graphic Accelerator, USB 2.0 Device and a variety of I/O peripheral components. POLLUX can significantly reduce system costs by eliminating not only the system control CPU, but also the Graphic IC, as well as the USB 1.1 Host/ USB 2.0 Device IC. POLLUX helps system designers reduce engineering effort and time taken to develop a new system, by adding only memory and I/O devices such as the LCD panel and human I/F devices.

1.1.1. Features

- 90nm, CMOS Process Technology.
- 288 pin FBGA (Fine BGA) Package
- 32bit CPU Embedded Architecture : 533MHz ARM926EJ with 16KByte I-Cache and 16KByte D-Cache.
- High performance 3D Graphics Accelerator
- USB 1.1 Host Controller, USB 2.0 Device, 4Ch UART
- LCD Controller, 8Ch DMA, Timer, Interrupt Controller, RTC
- SD/MMC
- I^2S
- I^2C, SSP, ADC, GPIOs, PWM, Power Manager

1.1.2. Block Diagram

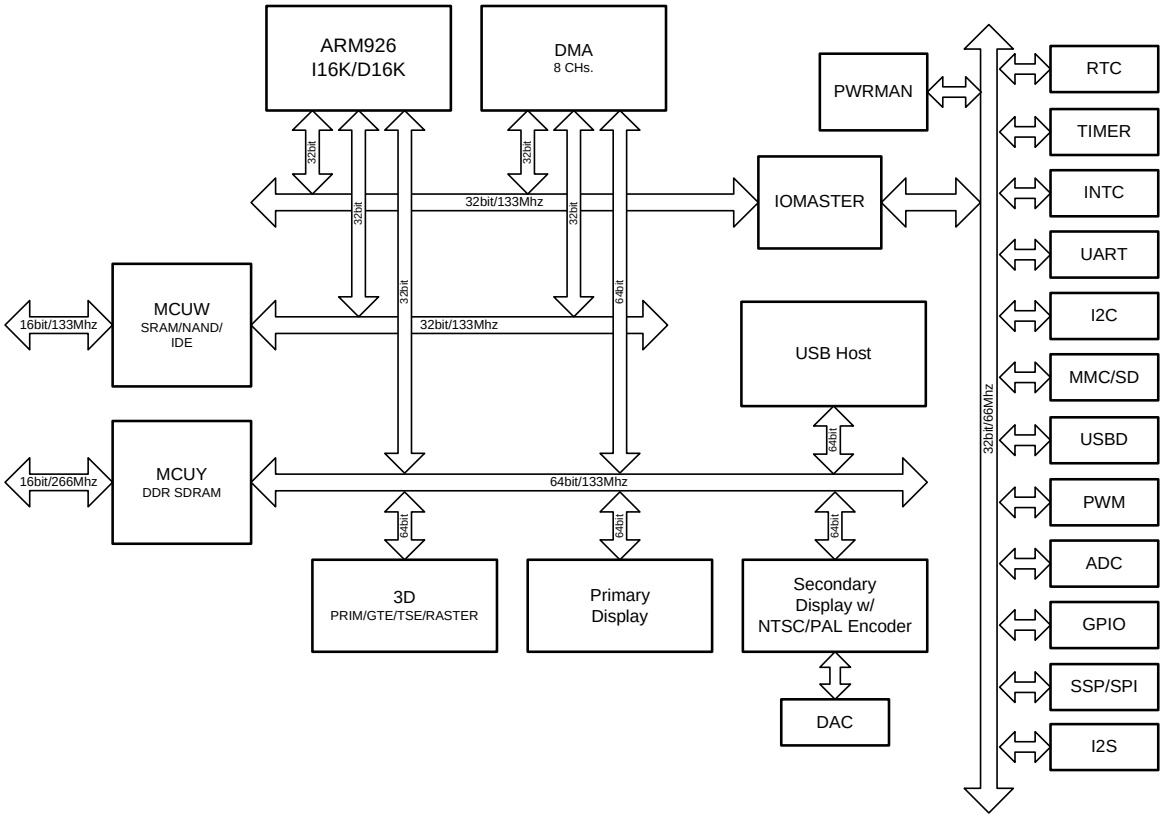


Figure 1-1. POLLUX Block Diagram

1.2. Functional Specification

1.2.1. Architecture

- 533MHz, ARM926EJ CPU Core
- 16KByte Instruction Cache, 16KByte Data Cache, Write Buffer to reduce the effect of main memory bandwidth and latency on performance.
- 16/32 bit RISC architecture and powerful instruction set with CPU core.

1.2.2. Clock and Power Manager

- Frequency is changed by Programmable Divider (PDIV, MDIV, SDIV)
- Number of PLLs are 2.

1.2.3. GPIO Controller

- Total 84 General Purpose I/O (GPIO) Pins
- Various GPIO Interrupt Mode (Rising Edge, Falling Edge, High Level and Low Level Detect)
- Individual Interrupt Generation Enabled/ disable is possible.

1.2.4. Memory Controller

- Memory Controller supports for single DDR-SDRAM Bank
- Static Memory Controller
  - Multiplexed Address
  - SRAM, ROM and NOR Flash
  - Programmable Wait Control

- Burst Read/ Write Support
- NAND Flash : NAND Booting and Hardware ECC Generation Support (both SLC/MLC)

1.2.5. DMA (Direct Memory Access)

- 8 Channel DMA
- Memory to Memory Transfer
- Memory to I/O Transfer
- I/O to Memory Transfer

1.2.6. Interrupt Controller

- Built-in Interrupt Controller
- Interrupt Controller Manages 64 Interrupt Sources
- Programmable Priority Control

1.2.7. Timer

- Five 32bit Built-in Timer/Counter
- WatchDog Function Supported

1.2.8. RTC (Real Time Clock)

- 32bit Counter
- Alarm Function : Alarm Interrupt or Wake Up from Power Down Mode
- Independent power pin (VDD_RTC)
- Support 1Hz Time interrupt for Power Down Mode

1.2.9. Audio

- I^2S
  - 16 bit (play and record),
  - 18 bits (play only)
  - Master and Slave Mode
  - Master Mode : Up to 192 kHz (128, 192, 256, 384fs)
  - Slave Mode : Up to 192 kHz (128, 192, 256, 384fs)
  - I^2S, Left-Justified, Right-Justified Data Mode

1.2.10. SD/ MMC

- Secure Digital memory (SD mem Version 2.00)
- Secure Digital I/O (SDIO version 1.10)
- Multimedia Cards (MMC version 4.2)
- Support clock speed up to 52MHz
- Support PIO and DMA mode data transfer
- Support 1/4-bit data bus

1.2.11. UART

- UART0 ~ UART3 with DMA-Based or Interrupt-Based Operation.
- UART1 with Full modem function.
- Ability to add or delete standard asynchronous communications bit (Start, Stop and Parity) in the serial data.
- Independently controls transmission, reception, line status and data set interrupts.
- Programmable Baud Rate

- Modem control pins that allow flow control through software.
- Fully programmable serial interface :
  - 5, 6, 7, 8-bit characters
  - Even, Odd and no parity detection
  - 1 or 2 Stop bit generation
  - Baud rate generation up to around 3.1Mbps
- 16-byte transmit FIFO
- 16-byte receive FIFO
- Complete status reporting capability
- Ability to generate and detect line breaks
- Internal diagnostic capabilities that include
  - Loopback controls for communications link fault isolation
- Separates DMA requests for transmit and receive data services

1.2.12. USB Host/ Device

- USB 1.1 Host
  - Compliant to USB 1.1 specification
  - 3 downstream ports.
- USB 2.0 Device
  - Compliant to USB2.0 specification.
  - Support FS/HS dual mode operation.
  - Conforms to UTMI (USB Transceiver Macrocell Interface)
  - Easy FIFO size configuration.
  - DMA interface capability.

1.2.13. SSP/ SPI (Serial Protocol / Serial Peripheral Interface)

- SSP Protocol compatible, SPI Protocol
- 16-bits x 16 FIFO
- Master& Slave mode
- Polling, Interrupt, DMA transfer mode
- Supports Standard four SPI Format
  - Format A, normal
  - Format A, inverse
  - Format B, normal
  - Format B, inverse
- 5-bit pre-scale counter
- 3 Channel SSP/SPI

1.2.14. I^2C (Inter-Integrate Circuit)

- 2 channel I^2C-bus
- 100Kbps ~ 1Mbps Speed (due to clock Pre-Scaler)
- Interrupt mode (Byte Transfer)
- Support Master & Slave mode

1.2.15. PWM (Pulse Width Modulation)

- 3 Channel Pulse Width Modulator channels
- 7-bit Clock divider & 10-bit Period counter
- 10-bit Duty counter

1.2.16. ADC (Analog to Digital Converter)

- Channels : 8 channels
- Resolution : 10 bit
- Maximum conversion rate : 500KSPS (samples per sec)
- Main clock : 2.5MHz (max.)
- Power supply : 3.3V ±0.3V, 1.3V ±0.1V(Digital I/O Interface)
- Input range : 0.0V ~ 3.3V ($3.3V_{P-P}$)
- Differential linearity Error : ±1.0 LSB
- Integral linearity Error : ±2.0 LSB
- Signal to Noise & Distortion Ratio : 54dB (Typ.)

1.2.17. MLC

- Two RGB Layers and One Video Layer
- RGB layers can be used as 3D layers.
- Dual Register-Set Architecture
- Various Pixel Formats
- Video Layer Priority
- Various Blending Effects between Layers
  - Per-layer or Per-pixel Alpha blending, Transparency, Inverse color
- Hardware Clipping
- Vertical flip
- Free Layer Position and Size in Pixel Unit
- Scale-up/Down (Video Layer Only)
  - Bi-linear interpolation or Nearest neighbor sampling scale-up/down
- Color control (Video layer only)
  - Brightness, Contrast, Hue, Saturation

1.2.18. DPC (Display Controller)

- Supports RGB, Multiplexed RGB (MRGB), ITU-R BT.601 and ITU-R BT.656
- Programmable HSYNC, VSYNC and DE (Data Enable)
- Programmable polarity for Sync signals
- Programmable delay for data, Sync signals and clock phase
- Supports dual display
- Supports NTSC/PAL TV output (CVBS only)
- Supports RGB dithering
- 10-bit Built-in Video DAC : Analog Composite Support
- Support Format : NTSC-J/N, PAL-B/D/G/H/I/M/N/Combination-N
- Support STN-LCD for Primary
- TV-out Up Scaler for Dual Display(LCD and TV)

1.2.19. 3D Graphic Accelerator

- Programmable floating point vector processing engine for geometric transform.
  - Variable mathematical operation.
  - 512-depth instruction memory
  - 252 Vector Input/Constant Registers
  - 16 Vector General Purpose Registers
- 2x2 Sub-Pixel Accuracy
- Features of Texturing
  - Perspective Correction
  - Multi-Texturing

- Bi-Linear Filtering
- MIPMAP

- Features of Pixel Operation
  - Per-Pixel Fogging
  - Hardware Dithering

1.2.20. CSC (Color Space Converter)

- Color Space Converter (CSC) module converts Y/Cb/Cr pixel format to R/G/B format for using as texture in 3D Core.

1.2.21. IDCT (Inverse Discrete Cosine Transform)

- IDCT supported on an 8x8 bock of samples
- Suitable for mpeg2, mpeg4, jpeg
- IDCT input precision 11 bits, output precision 9 bits/11bits
- IEEE 1180 IDCT fully compatible.
- more precisions than IEEE 1180 standard is available

1.2.22. Operating Voltage Range

- Core : TBD
- Memory : 2.5V (DDRSDRAM)
- I/O : 3.3V

1.2.23. Operating Frequency

- 533MHz /133MHz/133MHz (CPU/Core/Memory)

1.2.24. Operating Temperature

- Commercial Temperature (0℃ ~ 70℃) : POLLUX

1.2.25. Package

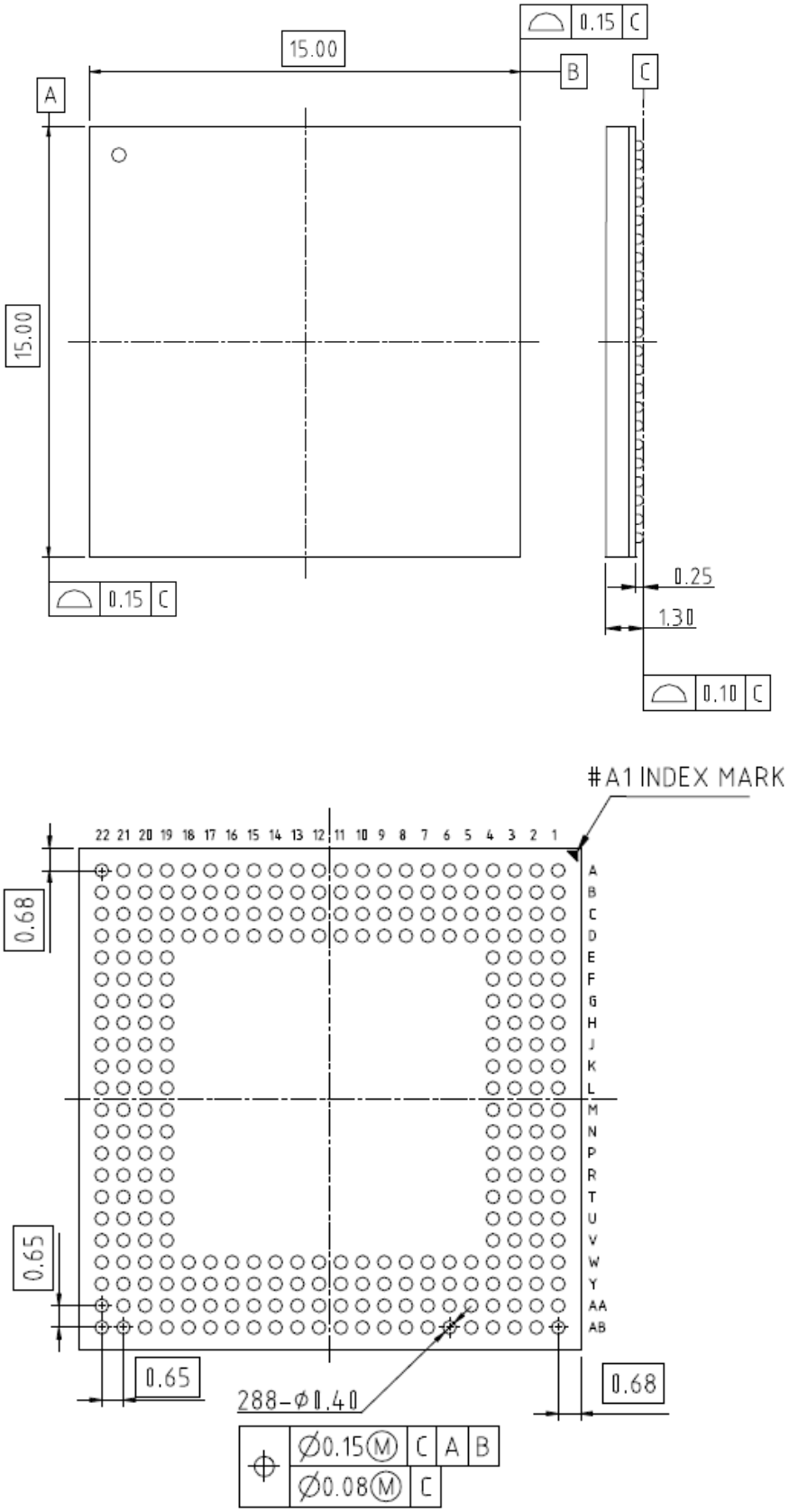
- 288-FBGA

CHAPTER 2.

I/O PIN DESCRIPTION

2. I/O PIN DESCRIPTION

2.1. Mechanical Dimensions



2.2. Marking Information

TBD

2.3. POLLUX Package FBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VDD10A_PLL0	VIDEO	VDD33A_DAC	USBXI	USBXO	VSS33A_USB2C	USBDP	USBDM	VSS33A_USB2A	ADCIN6	VDD33A_ADC	VSS33A_ADC	YA4	YA6	YA8	YA11	YDQM1	YCK	YCKE	YD7	YD5	YD4	A
B	VSS10A_PLL0	VDD10A_PLL1	VSS33A_DAC	VSSA33C_USB2	VDDA33C_USB2	VSS33A_USB2B	VDD33A_USB2B	VDD33A_USB2A	ADCIN4	ADCIN5	ADCIN7	ADCREF	YA5	YA7	YA9	YA12	YnCK	YDQM0	YDQS0	YD6	YD3	YD2	B
C	XTI	VSS10A_PLL1	VREF	IREF	USBTESTA	UP	UM	ADCIN2	ADCIN3	VDD33D_ADC	YD15	YD13	YD12	YD11	YD10	YD8	YnWE	YnCAS	YnRAS	YnCS0	YD1	YD0	C
D	XTO	GPIOALIVE1	VCOMP	VSS33AR_DAC	USBREXT	USBVBUS	ADCIN0	ADCIN1	VSS	VDDI10	YD14	YD9	YDQS1	Yref	VSS25	VDD25	VSS25	VDD25	VSS25	YBA0	YA10	YA0	D
E	GPIOALIVE3	GPIOALIVE2	GPIOALIVE0	VDD33AR_DAC															VDD25	YBA1	YA1	YA2	E
F	GPIOALIVE6	GPIOALIVE5	GPIOALIVE4	VDD33D_DAC															VDD25	SDDAT13	SDDAT12	YA3	F
G	XTIRTC	VDD_RTC	PORSEL	VDDI10_ALV															SDDAT11	SDDAT10	SDDAT03	SDDAT02	G
H	XTORTC	VDDPWRON	nBATF	VDD33_ALV															VSS	SDCMD1	SDDAT01	SDDAT00	H
J	TDO	TCK	nVDDPWRTOGGLE	VSS															VDDI10	SDCLK1	SDCMD0	SDCLK0	J
K	TMS	TDI	nTRST	VDDI10															VSS	SDA1	SCL1	SDA0	K
L	RX0	nPORST	JTAGMODE	VSS															VDD33_IO	SSPFRM0	SSPRXD0	SCL0	L
M	TX0	nEXTRST	TEST_EN	VDD33_IO															SSPFRM1	SSPCLK1	SSPTXD0	SSPCLK0	M
N	TX1	nCTS1	nRTS1	VSS															SSPRXD1	SSPTXD1	PVSYNC(YD)	PVCLK	N
P	RX1	nRIO1	nDCD1	VDDI10															VSS	PVD12	PDE(CL2)	PHSYNC(CL1)	P
R	TX2	RX2	TX3	nDSR1															VDD33_IO	PVD13	PVD1	PVD0	R
T	PWMOUT0	PWMOUT1	RX3	nDTR1															PVD14	PVD15	PVD3	PVD2	T
U	I2SDATO	I2SSYNC	PWMOUT2	VDD33_IO															PVD16	PVD17	PVD5	PVD4	U
V	I2SMCLK	I2SBCLK	I2SDATI	VSS															PVD19	PVD18	PVD7	PVD6	V
W	SA23	SA24	SA25	NC	VSS	VDDI10	VSS	nSCS4	VDD33_IO	VSS	VDDI10	VSS	VDD33_IO	VSS	RnB	VSS	VDD33_IO	VDDI10	VSS	PVD20	PVD9	PVD8	W
Y	SA21	SA22	nSCS9	NC	RDnWR	nSCS6	nSCS5	nSCS3	nSCS2	nSCS1	nSCS0	nSOE	nSWE	nNCS1	nNFOE	nNCS0	NFCLEi	NFALE	nNFWE	PVD23	PVD11	PVD10	Y
AA	SA20	nSCS8	LATADDR	nSWAIT	SA17	SA15	SA13	SA11	SA9	SA7	SA5	SA3	SA1	SD15	SD13	SD11	SD9	SD7	SD5	SD3	PVD22	PVD21	AA
AB	SA19	nSCS7	nSDQM1	SA18	SA16	SA14	SA12	SA10	SA8	SA6	SA4	SA2	SA0	SD14	SD12	SD10	SD8	SD6	SD4	SD2	SD1	SD0	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

2.4. Function Description

Pin Name	GPIO No	GPIO Function	Type	Description
Memory Controller (MCU-A)				
YD[15:0]	-	-	I/O	MCU-A Bank DDR-SDRAM Data bus. AD[15:0] is used for 16-bit data mode.
YA[12:0]	-	-	O	MCU-A Bank DDR-SDRAM Address bus.
YBA[1:0]	-	-	O	MCU-A Bank DDR-SDRAM Bank address.
YCK	-	-	O	MCU-A Bank DDR-SDRAM clock.
YnCK	-	-	O	MCU-A Bank DDR-SDRAM inverting clock.
YCKE	-	-	O	MCU-A Bank DDR-SDRAM clock enable.
YnCS0	-	-	O	MCU-A Bank DDR-SDRAM Chip Select 0. This signal should be connected to the chip select pin for DDR-SDRAM.
YnRAS	-	-	O	MCU-A Bank DDR-SDRAM RAS. This signal should be connected to the row address strobe pin for all banks of DDR-SDRAM.
YnCAS	-	-	O	MCU-A Bank DDR-SDRAM CAS. This signal should be connected to the column address strobe pin for all banks of DDR-SDRAM.
YnWE	-	-	O	MCU-A Bank DDR-SDRAM write enable. This signal should be connected to the write enables for DDR-SDRAM.
YDQS0	-	-	I/O	MCU-A Bank DDR-SDRAM Data Strobe0.
YDQS1	-	-	I/O	MCU-A Bank DDR-SDRAM Data Strobe1.
YDQM0	-	-	O	MCU-A Bank DDR-SDRAM DQM for data bytes 0. These signals should be connected to the data output mask enable for DDR-SDRAM.
YDQM1	-	-	O	MCU-A Bank DDR-SDRAM DQM for data bytes 1. These signals should be connected to the data output mask enable for DDR-SDRAM.
Yref			I	DDR PAD Reference Voltage (1.25v)
Static Memory				
SD[15:0]	-	-	I/O	Static Memory/NAND Data bus.
SA[0]/nSDQM0	-	-	O	Static Memory Address bus, This signal should be connected to the low byte enable for 16bit SRAM.
SA[1]	-	-	O	Static Memory Address bus.
SA[2](SALAT[19])	-	-	O	Static Memory Address bus.
SA[3](SALAT[20])	-	-	O	Static Memory Address bus.
SA[4](SALAT[21])	-	-	O	Static Memory Address bus.
SA[5](SALAT[22])	-	-	O	Static Memory Address bus.
SA[6](SALAT[23])	-	-	O	Static Memory Address bus.
SA[7](SALAT[24])	-	-	O	Static Memory Address bus.
SA[8](SALAT[25])	-	-	O	Static Memory Address bus.
SA[18:9]	-	-	O	Static Memory Address bus.
SA[25:19]	GPIOC[14:8]	ALT1	O	Static Memory Address bus.
nSDQM[1]	-	-	O	Static Memory High Byte Enable.
LATADDR	-	-	O	Static Memory Latch Address Enable.
RDnWR	-	-	O	Buffer Direction Control. Read/Write for static interface. Intended for use as a steering signal for buffering logic.
nSCS [0]_ nSCS [1]	-	-	O	Static Memory Chip Select.
nSCS [1]_ nSCS [0]	-	-	O	Static Memory Chip Select.

Pin Name	GPIO No	GPIO Function	Type	Description
nSCS [2]	GPIOC[15]-	ALT1	O	Static Memory Chip Select.
nSCS [3]	GPIOC[16]	ALT1	O	Static Memory Chip Select.
nSCS [4]	GPIOC[17]	ALT1	O	Static Memory Chip Select.
nSCS [5]	GPIOC[18]	ALT1	O	Static Memory Chip Select.
nSCS [6]	GPIOC[19]	ALT1	O	Static Memory Chip Select.
nSCS [7]	GPIOC[0]	ALT1	O	Static Memory Chip Select.
nSCS[8]	GPIOC[1]	ALT1	O	Static Memory Chip Select.
nSCS[9]	GPIOC[2]	ALT1	O	Static Memory Chip Select.
nSWAIT	-	-	I	Wait Control for Static Memory. This signal is an input and is driven low by the Static Memory to extend the length of the transfers to/from applications processor.
nSOE	-	-	O	Static Memory Read Enable.
nSWE	-	-	O	Static Memory Write Enable.
nNCS[0]_ nNCS [1]	-	-	O	NAND Chip Select0. This is chip select to NAND Flash memory.
nNCS[1]_ nNCS [0]	-	-	O	NAND Chip Select1. This is chip select to NAND Flash memory.
NFCLE	-	-	O	NAND CLE
NFALE	-	-	O	NAND ALE
RnB	-	-	I	NAND Ready & Busy. This is Ready/Busy signal of NAND Flash memory.
nNFOE	-	-	O	NAND Read Enable.
nNFWE	-	-	O	NAND Write Enable.
Dispay Controller				
PVD[7:0]	GPIOA[7:0]	ALT1	O	Video output data (RGB, Multiplexed-RGB, YCbCr)
PVD[23:8]	GPIOB[31:16]	ALT1	O	Video output data (RGB, Multiplexed-RGB, YCbCr)
PDE(CL2)	-	-	O	Data Enable'CSYNC.
PHSYNC(CL1)	-	-	O	Horizontal Sync
PVSYNC(YD)	-	-	O	Vertical Sync
PVCLK(VM)	-	-	O	Pixel Clock output
NTSC/PAL				
VIDEO			O	Analog TV out.
VREF			I	Video DAC Reference
IREF			I	Video DAC Reference Current
VCOMP			I	Video Compensation Capacitor
UART				
RX0	-	-	I	UART0 Receive Pin./UART Boot Pin
TX0	GPIOA[8]	ALT1	O	UART0 Transmit Pin.
nRTS1	GPIOA[10]	ALT1	O	UART1 Ready-To-Send
nCTS1	GPIOA[9]	ALT1	I	UART1 Clear-To-Send
nDTR1	GPIOA[14]	ALT1	O	UART1 Data-Terminal-Ready
nDSR1	GPIOA[13]	ALT1	I	UART1 Data-Set-Ready Pin0.
nDCD1	GPIOA[12]	ALT1	I	UART1 Data-Carrier-Detect
nRIO1	GPIOA[11]	ALT1	I	UART1 Ring Indicator

Pin Name	GPIO No	GPIO Function	Type	Description
RX1	GPIOA[16]	ALT1	I	UART1 Receive Pin.
TX1	GPIOA[15]	ALT1	O	UART1 Transmit Pin.
RX2	GPIOA[18]	ALT1	I	UART2 Receive Pin.
TX2	GPIOA[17]	ALT1	O	UART2 Transmit Pin.
RX3	GPIOA[20]	ALT1	I	UART3 Receive Pin
TX3	GPIOA[19]	ALT1	O	UART3 Transmit Pin.
MMC/SD Controller				
SDCLK0	GPIOB[0]	ALT1	IO	SD Clock 1 Channel
SDCMD0	GPIOB[1]	ALT1	I/O	SD Command 1 Channel
SDDATA0[3:0]	GPIOB[5:2]	ALT1	I/O	SD Data 1 Channel
SDCLK1	GPIOB[6]	ALT1	IO	SD Clock 2 Channel
SDCMD1	GPIOB[7]	ALT1	I/O	SD Command 2 Channel
SDDATA1[3:0]	GPIOB[11:8]	ALT1	I/O	SD Data 2 Channel
I^2S Controller				
I2SDATO	GPIOA[21]	ALT1	O	Audio Port Data Out (SDO)
I2SBCLK	GPIOA[22]	ALT1	I/O	Audio Port Bit Clock
I2SDATI	GPIOA[23]	ALT1	I	Audio Port Data In (SDI)
I2SSYNC	GPIOA[24]	ALT1	I/O	Audio Port Sync Signal (LRCK)
I2SMCLK	GPIOA[25]	ALT1	O	Audio Port MCLK (12 MHz Clock)
I^2C Controller				
SDA0	GPIOA[26]	ALT1	I/O	I2C SDA0
SCL0	GPIOA[27]	ALT1	I/O	I2C SCL0
SDA1	GPIOA[28]	ALT1	I/O	I2C SDA1
SCL1	GPIOA[29]	ALT1	I/O	I2C SCL1
SSP / SPI Controller				
SSPRXD0	GPIOB[14]	ALT1	I	Synchronous Serial Port RX (SPI MISO)
SSPTXD0	GPIOB[15]	ALT1	O	Synchronous Serial Port TX (SPI MOSI)
SSPCLK0	GPIOB[13]	ALT1	I/O	Synchronous Serial Port clock (SPI SCLK)
SSPFRM0	GPIOB[12]	ALT1	I/O	Synchronous Serial Port Frame0 signal
SSPRXD1	GPIOC[5]	ALT1	I	Synchronous Serial Port RX 1l
SSPTXD1	GPIOC[6]	ALT1	O	Synchronous Serial Port TX 1
SSPCLK1	GPIOC[4]	ALT1	I/O	Synchronous Serial Port clock 1
SSPFRM1	GPIOC[3]	ALT1	I/O	Synchronous Serial Port Frame1 signal
SSPRXD2	GPIOB[1]	ALT2	I	Synchronous Serial Port RX 2
SSPTXD2	GPIOB[2]	ALT2	O	Synchronous Serial Port TX 2
SSPCLK2	GPIOB[0]	ALT2	I/O	Synchronous Serial Port clock 2
SSPFRM2	GPIOB[5]	ALT2	I/O	Synchronous Serial Port Frame 2 signal
PWM Controller				
PWM0	GPIOA[30]	ALT1	O	Pulse Width Modulation Output
PWM1	GPIOA[31]	ALT1	O	Pulse Width Modulation Output

Pin Name	GPIO No	GPIO Function	Type	Description
PWM2	GPIOC[7]	ALT1	O	Pulse Width Modulation Output
USB				
USBDP	-	-	I/O	USB Host Only : Ch0
USBDM	-	-	I/O	USB Host Only : Ch0
UP	-	-	I/O	USB 2.0 Device Plus.
UM	-	-	I/O	USB 2.0 Device Minus.
USBREXT	-	-	O	Connection to the external 3.4k-ohm (+/- 1%) resistor. The 3.4K-ohm (+/- 1%) resistor must be referenced to the ground and placed as close as possible to the chip.
USBTESTA	-	-	O	Analog Test Pin. 10K-ohm (+/- 1%) resistor must be referenced to the GND.
USBVBUS	-	-	I	VBUS Detect. This VBUS indicator signal indicates that the VBUS signal on the USB cable is active.
USBXO	-	-	O	12MHz Crystal output.
USBXI	-	-	I	12MHz Crystal input.
ADC Controller				
ADCIN[7:0]	-	-	I	ADC Analog Input
ADCREF	-	-	I	ADC Regerence Voltage.
Miscellaneous				
nPORST	-	-	I	Global Reset In. Active low input. nRESET is a level-sensitive input which is used to start the processor from a known address. A LOW level will cause the current instruction to terminate abnormally and all on-chip states to be reset. When nRESET is driven HIGH, the processor will re-start from address 0.
nEXTRST	-	-	O	Global Reset Output.
PORSEL	-	-	I	Decide to use internal POR (Power On Reset) 0 : Use Internal POR. 1 : Not use internal POR.
TEST_EN	-	-	I	Test Mode Enable.
vddpwron	-	-	O	Momentary Power Control (VDD Power On)
vddpwrtoggle	-	-	I	Momentary Power Control (Toggle Switch)
jtagmode	-	-	I	Serial Data Input for JTAG Enable
PLL				
XTI	-	-	I	27MHz Oscillator Input
XTO	-	-	O	27MHz Oscillator Output
RTC				
XTIRTC	-	-	I	32.768KHz RTC Crystal input.
XTORTC	-	-	O	32.768KHz RTC Crystal output.
VDD_RTC	-	-	I	RTC Supply
Alive GPIO				
GPIOALIVE[6:0]	-	-	O	Active GPIO when Powered Off
Power Manager				
nBATF	-	-	I	Battery Fault
JTAG				
nTRST	-	-	I	Reset input for the JTAG Logic.
TDO	-	-	O	Serial output for test instructions and data for JTAG.
TDI	-	-	I	Serial Data input for JTAG.(testmode2)

Pin Name	GPIO No	GPIO Function	Type	Description
TMS	-	-	I	TMS controls the sequence of the TAP controller's state.(testmode1)
TCK			I	Clock Input for JTAG Logic. (testmode0)
Power and Ground : TBD				
VSS10A_PLL0	-	-	-	Analog GND for PLL TBD Power.
VDD10A_PLL0	-	-	-	Analog VCC for PLL TBD Power.
VSS10A_PLL1	-	-	-	Analog GND for PLL TBD Power.
VDD10A_PLL1	-	-	-	Analog VCC for PLL TBD Power.
VSS33A_USB2A	-	-	-	Analog GND for USB 3.3V Power.
VSS33A_USB2B	-	-	-	Analog GND for USB 3.3V Power.
VSS33A_USB2C	-	-	-	Analog GND for USB 3.3V Power.
VDD33A_USB2A	-	-	-	Analog VCC for USB 3.3V Power.
VDD33A_USB2B	-	-	-	Analog VCC for USB 3.3V Power.
VSSA33C_USB2	-	-	-	Digital GND for USB Clock 3.3V Power.
VDDA33C_USB2	-	-	-	Digital VCC for USB Clock 3.3V Power.
VSS33A_ADC	-	-	-	Analog GND for ADC 3.3V Power.
VDD33A_ADC	-	-	-	Analog VCC for ADC 3.3V Power.
VDD33D_ADC	-	-	-	Digital VCC for ADC 3.3V Power.
VSS33A_DAC	-	-	-	Analog GND for DAC 3.3V Power.
VSS33AR_DAC	-	-	-	Analog GND for DAC 3.3V Power.
VDD33A_DAC	-	-	-	Analog VCC for DAC 3.3V Power.
VDD33D_DAC	-	-	-	Digital VCC for DAC 3.3V Power.
VSS25	-	-	-	GND for DDR-SDRAM 2.5V Power.
VDD25	-	-	-	VCC for DDR-SDRAM 2.5V Power.
VDD_RTC	-	-	-	VCC for RTC 2.5V ~ 3.6V Power.
VDDI10	-	-	-	VCC for Internal TBD Logic Power.
AREF	-	-		1.25V Reference VCC for MCU-A bank.
IREF	-	-	-	External resistor connection (2.6kΩ against Ground) for generating reference current.
VREF	-	-	-	TBD Reference VCC for Internal Video DAC.
VCOMP	-	-	-	External capacitor connection to 3.3V Power.
ADCREF	-	-	-	3.3V Reference VCC for ADC.
VDD33	-	-	-	VCC for 3.3V I/O Power.
VSS	-	-	-	GND.

Table 2-1. POLLUX Pin Function Description

2.5. GPIO Pin Functions

GPIO Pins	Alternate Function 1	Alternate Function 2
GPIOA[31 : 0]		
GPIOA[31]	PWMOUT[1]	-
GPIOA[30]	PWMOUT[0]	
GPIOA[29]	SDA[1]	
GPIOA[28]	SCL[1]	
GPIOA[27]	SDA[0]	
GPIOA[26]	SCL[0]	
GPIOA[25]	I2SMCLK	
GPIOA[24]	I2SSYNC	
GPIOA[23]	I2SDATI	
GPIOA[22]	I2SBCLK	
GPIOA[21]	I2SDATO	
GPIOA[20]	RX[3]	
GPIOA[19]	TX[3]	
GPIOA[18]	RX[2]	
GPIOA[17]	TX[2]	
GPIOA[16]	RX[1]	
GPIOA[15]	TX[1]	
GPIOA[14]	nDTR[1]	
GPIOA[13]	nDSR[1]	
GPIOA[12]	nDCD[1]	
GPIOA[11]	nRIO[1]	
GPIOA[10]	nRTS[1]	
GPIOA[9]	nCTS[1]	
GPIOA[8]	TX[0]	
GPIOA[7]	PVD[7]	
GPIOA[6]	PVD[6]	
GPIOA[5]	PVD[5]	
GPIOA[4]	PVD[4]	
GPIOA[3]	PVD[3]	
GPIOA[2]	PVD[2]	
GPIOA[1]	PVD[1]	
GPIOA[0]	PVD[0]	
GPIOB[31 : 0]		
GPIOB[31]	PVD[23]	-
GPIOB[30]	PVD[22]	
GPIOB[29]	PVD[21]	
GPIOB[28]	PVD[20]	
GPIOB[27]	PVD[19]	

GPIO Pins	Alternate Function 1	Alternate Function 2
GPIOB[26]	PVD[18]	
GPIOB[25]	PVD[17]	
GPIOB[24]	PVD[16]	
GPIOB[23]	PVD[15]	
GPIOB[22]	PVD[14]	
GPIOB[21]	PVD[13]	
GPIOB[20]	PVD[12]	
GPIOB[19]	PVD[11]	
GPIOB[18]	PVD[10]	
GPIOB[17]	PVD[9]	
GPIOB[16]	PVD[8]	
GPIOB[15]	SSPTXD[0]	
GPIOB[14]	SSPRXD[0]	
GPIOB[13]	SSPCLK[0]	
GPIOB[12]	SSPFRM[0]	
GPIOB[11]	SDDAT1[3]	
GPIOB[10]	SDDAT1[2]	
GPIOB[9]	SDDAT1[1]	
GPIOB[8]	SDDAT1[0]	
GPIOB[7]	SDCMD1	
GPIOB[6]	SDCLK1	
GPIOB[5]	SDDAT0[3]	SSPFRM[2]
GPIOB[4]	SDDAT0[2]	
GPIOB[3]	SDDAT0[1]	
GPIOB[2]	SDDAT0[0]	SSPTXD[2]
GPIOB[1]	SDCMD0	SSPRXD[2]
GPIOB[0]	SDCLK0	SSPCLK[2]
GPIOC[22 : 0]		
GPIOC[19]	nSCS[6]	
GPIOC[18]	nSCS[5]	
GPIOC[17]	nSCS[4]	
GPIOC[16]	nSCS[3]	
GPIOC[15]	nSCS[2]	
GPIOC[14]	SA[25]	
GPIOC[13]	SA[24]	
GPIOC[12]	SA[23]	
GPIOC[11]	SA[22]	
GPIOC[10]	SA[21]	
GPIOC[9]	SA[20]	
GPIOC[8]	SA[19]	

GPIO Pins	Alternate Function 1	Alternate Function 2
GPIOC[7]	PWMOUT[2]	
GPIOC[6]	SSPTXD[1]	
GPIOC[5]	SSPRXD[1]	
GPIOC[4]	SSPCLK[1]	
GPIOC[3]	SSPFRM[1]	
GPIOC[2]	nSCS[9]	AVCLK
GPIOC[1]	nSCS[8]	
GPIOC[0]	nSCS[7]	

Table 2-2. GPIO Pin Functions

2.6. POLLUX I/O Pin Listing

The Power Balls will be added.

Ball	Name	Type	Func.After Reset	Primary Function	Alternate Function 1	Alternate Function 2
	GPIOALIVE[0]		GPIOALIVE[0]	GPIOALIVE[0]	-	-
	GPIOALIVE [1]		GPIOALIVE [1]	GPIOALIVE [1]	-	-
	GPIOALIVE [2]		GPIOALIVE [2]	GPIOALIVE [2]	-	-
	GPIOALIVE [3]		GPIOALIVE [3]	GPIOALIVE [3]	-	-
	GPIOALIVE [4]		GPIOALIVE [4]	GPIOALIVE [4]		
	GPIOALIVE [5]		GPIOALIVE [5]	GPIOALIVE [5]		
	GPIOALIVE [6]		GPIOALIVE [6]	GPIOALIVE [6]		
	NPORST		NPORST	NPORST	-	-
	NEXTRST		NEXTRST	NEXTRST	-	-
	XTIRTC		XTIRTC	XTIRTC	-	-
	XTORTC		XTORTC	XTORTC	-	-
	VDD_RTC		RTC_VDD	RTC_VDD	-	-
	nBATF		nBATF	nBATF	-	-
	JTAGMODE		JTAGMODE	JTAGMODE	-	-
	VDDPWRON		VDDPWRON	VDDPWRON	-	-
	VDDPWRTOGGLE		VDDPWRTOGGLE	VDDPWRTOGGLE	-	-
	TEST_EN		TEST_EN	TEST_EN	-	-
	GPIOA[0]/PVD[0]		GPIOA[0]	GPIOA[0]	PVD[0]	-
	GPIOA[1]/PVD[1]		GPIOA[1]	GPIOA[1]	PVD[1]	-
	GPIOA[2]/PVD[2]		GPIOA[2]	GPIOA[2]	PVD[2]	-
	GPIOA[3]/PVD[3]		GPIOA[3]	GPIOA[3]	PVD[3]	-
	GPIOA[4]/PVD[4]		GPIOA[4]	GPIOA[4]	PVD[4]	-
	GPIOA[5]/PVD[5]		GPIOA[5]	GPIOA[5]	PVD[5]	-
	GPIOA[6]/PVD[6]		GPIOA[6]	GPIOA[6]	PVD[6]	-
	GPIOA[7]/PVD[7]		GPIOA[7]	GPIOA[7]	PVD[7]	-
	PVCLK(VM)		PVCLK(VM)	PVCLK(VM)	-	-
	VIDEO		VIDEO	VIDEO	-	-
	VREF		VREF	VREF	-	-
	IREF		IREF	IREF	-	-
	VOUTCOMP		VOUTCOMP	VOUTCOMP	-	-
	PDE(CL2)		PDE(CL2)	PDE(CL2)	-	-
	PHSYNC(CL1)		PHSYNC(CL1)	PHSYNC(CL1)	-	-
	PVSYNC(YD)		PVSYNC(YD)	PVSYNC(YD)	-	-
	RX[0]		RX[0]	RX[0]		
	GPIOA[8]/TX[0]		GPIOA[8]	GPIOA[8]		
	GPIOA[9]/nCTS[1]		GPIOA[9]	GPIOA[9]	nCTS[1]	
	GPIOA[10]/nRTS[1]		GPIOA[10]	GPIOA[10]	nRTS[1]	
	GPIOA[11]nRIO[1]		GPIOA[11]	GPIOA[11]	nRIO[1]	

Ball	Name	Type	Func.After Reset	Primary Function	Alternate Function 1	Alternate Function 2
	GPIOA[12]/nDCD[1]		GPIOA[12]	GPIOA[12]	nDCD[1]	
	GPIOA[13]/nDSR[1]		GPIOA[13]	GPIOA[13]	nDSR[1]	
	GPIOA[14]/nDTR[1]		GPIOA[14]	GPIOA[14]	nDTR[1]	
	GPIOA[15]/TX[1]		GPIOA[15]	GPIOA[15]	TX[1]	
	GPIOA[16]/RX[1]		GPIOA[16]	GPIOA[16]	RX[1]	
	GPIOA[17]/TX[2]		GPIOA[17]	GPIOA[17]	TX[2]	
	GPIOA[18]/RX[2]		GPIOA[18]	GPIOA[18]	RX[2]	
	GPIOA[19]/TX[3]		GPIOA[19]	GPIOA[19]	TX[3]	
	GPIOA[20]/RX[3]		GPIOA[20]	GPIOA[20]	RX[3]	
	SD[0]		SD[0]	SD[0]		
	SD[1]		SD[1]	SD[1]		
	SD[2]		SD[2]	SD[2]		
	SD[3]		SD[3]	SD[3]		
	SD[4]		SD[4]	SD[4]		
	SD[5]		SD[5]	SD[5]		
	SD[6]		SD[6]	SD[6]		
	SD[7]		SD[7]	SD[7]		
	SD[8]		SD[8]	SD[8]		
	SD[9]		SD[9]	SD[9]		
	SD[10]		SD[10]	SD[10]		
	SD[11]		SD[11]	SD[11]		
	SD[12]		SD[12]	SD[12]		
	SD[13]		SD[13]	SD[13]		
	SD[14]		SD[14]	SD[14]		
	SD[15]		SD[15]	SD[15]		
	SA[0]/nSDQM0		SA[0]	SA[0]		
	SA[1]		SA[1]	SA[1]		
	SA[2](SALAT[19])		SA[2]	SA[2]		
	SA[3](SALAT[20])		SA[3]	SA[3]		
	SA[4](SALAT[21])		SA[4]	SA[4]		
	SA[5](SALAT[22])		SA[5]	SA[5]		
	SA[6](SALAT[23])		SA[6]	SA[6]		
	SA[7](SALAT[24])		SA[7]	SA[7]		
	SA[8](SALAT[25])		SA[8]	SA[8]		
	SA[9]		SA[9]	SA[9]		
	SA[10]		SA[10]	SA[10]		
	SA[11]		SA[11]	SA[11]		
	SA[12]		SA[12]	SA[12]		
	SA[13]		SA[13]	SA[13]		
	SA[14]		SA[14]	SA[14]		

Ball	Name	Type	Func.After Reset	Primary Function	Alternate Function 1	Alternate Function 2
	SA[15]		SA[15]	SA[15]		
	SA[16]		SA[16]	SA[16]		
	SA[17]		SA[17]	SA[17]		
	SA[18]		SA[18]	SA[18]		
	LATADDR		LATADDR	LATADDR		
	nSWAIT		nSWAIT	nSWAIT		
	nSOE		nSOE	nSOE		
	nSWE		nSWE	nSWE		
	nNFOE		nNFOE	nNFOE		
	nNFWE		nNFWE	nNFWE		
	NFCLE		NFCLE	NFCLE		
	NFALE		NFALE	NFALE		
	RnB		RnB	RnB		
	RDnWR		RDnWR	RDnWR		
	nSDQM1		nSDQM1	nSDQM1		
	nNCS[0]_nNCS[1]		nNCS[0]	nNCS[0]		
	nNCS[1]_nNCS[0]		nNCS[1]	nNCS[1]		
	nSCS[0]_nSCS[1]		nSCS[0]	nSCS[0]		
	nSCS[1]_nSCS[0]		nSCS[1]	nSCS[1]		
	GPIOC[18]/nSCS[5]		GPIOC[18]	GPIOC[18]	nSCS[5]	
	GPIOC[19]/nSCS[6]		GPIOC[19]	GPIOC[19]	nSCS[6]	
	GPIOA[21]/ I2SDATO		GPIOA[21]	GPIOA[21]	I2SDATO	
	GPIOA[22]/I2SBCLK		GPIOA[22]	GPIOA[22]	I2SBCLK	
	GPIOA[23]/ I2SDATI		GPIOA[23]	GPIOA[23]	I2SDATI	
	GPIOA[24]/I2SSYNC		GPIOA[24]	GPIOA[24]	I2SSYNC	
	GPIOA[25]/I2SMCLK		GPIOA[25]	GPIOA[25]	I2SMCLK	
	GPIOA[26]/SCL[0]		GPIOA[26]	GPIOA[26]	SCL[0]	
	GPIOA[27]/SDA[0]		GPIOA[27]	GPIOA[27]	SDA[0]	
	GPIOA[28]/SCL[1]		GPIOA[28]	GPIOA[28]	SCL[1]	
	GPIOA[29]/SDA[1]		GPIOA[29]	GPIOA[29]	SDA[1]	
	GPIOA[30]/PWMOUT[0]		GPIOA[30]	GPIOA[30]	PWMOUT[0]	
	GPIOA[31]/PWMOUT[1]		GPIOA[31]	GPIOA[31]	PWMOUT[1]	
	GPIOB[0]/GPIOB[0]		GPIOB[0]	GPIOB[0]	SDCLK0	SSPCLK2
	GPIOB[1]/SDCMD0		GPIOB[1]	GPIOB[1]	SDCMD0	SSPRXD2
	GPIOB[2]/SDDAT0[0]		GPIOB[2]	GPIOB[2]	SDDAT0[0]	SSPTXD2
	GPIOB[3]/SDDAT0[1]		GPIOB[3]	GPIOB[3]	SDDAT0[1]	
	GPIOB[4]/SDDAT0[2]/		GPIOB[4]	GPIOB[4]	SDDAT0[2]	
	GPIOB[5]/SDDAT0[3]		GPIOB[5]	GPIOB[5]	SDDAT0[3]	SSPRRM2
	GPIOB[6]/SDCLK1		GPIOB[6]	GPIOB[6]	SDCLK1	
	GPIOB[7]/SDCMD1		GPIOB[7]	GPIOB[7]	SDCMD1	

Ball	Name	Type	Func.After Reset	Primary Function	Alternate Function 1	Alternate Function 2
	GPIOB[8]/SDDAT1[0]		GPIOB[8]	GPIOB[8]	SDDAT1[0]	
	GPIOB[9]/SDDAT1[1]		GPIOB[9]	GPIOB[9]	SDDAT1[1]	
	GPIOB[10]/SDDAT1[2]		GPIOB[10]	GPIOB[10]	SDDAT1[2]	
	GPIOB[11]/SDDAT1[3]		GPIOB[11]	GPIOB[11]	SDDAT1[3]	
	YA[0]		YA[0]	YA[0]		
	YA[1]		YA[1]	YA[1]		
	YA[2]		YA[2]	YA[2]		
	YA[3]		YA[3]	YA[3]		
	YA[4]		YA[4]	YA[4]		
	YA[5]		YA[5]	YA[5]		
	YA[6]		YA[6]	YA[6]		
	YA[7]		YA[7]	YA[7]		
	YA[8]		YA[8]	YA[8]		
	YA[9]		YA[9]	YA[9]		
	YA[10]		YA[10]	YA[10]		
	YA[11]		YA[11]	YA[11]		
	YA[12]		YA[12]	YA[12]		
	YBA0		YBA0	YBA0		
	YBA1		YBA1	YBA1		
	YD[0]		YD[0]	YD[0]		
	YD[1]		YD[1]	YD[1]		
	YD[2]		YD[2]	YD[2]		
	YD[3]		YD[3]	YD[3]		
	YD[4]		YD[4]	YD[4]		
	YD[5]		YD[5]	YD[5]		
	YD[6]		YD[6]	YD[6]		
	YD[7]		YD[7]	YD[7]		
	YD[8]		YD[8]	YD[8]		
	YD[9]		YD[9]	YD[9]		
	YD[10]		YD[10]	YD[10]		
	YD[11]		YD[11]	YD[11]		
	YD[12]		YD[12]	YD[12]		
	YD[13]		YD[13]	YD[13]		
	YD[14]		YD[14]	YD[14]		
	YD[15]		YD[15]	YD[15]		
	YnCS0		YnCS0	YnCS0		
	YDQS0		YDQS0	YDQS0		
	YDQS1		YDQS1	YDQS1		
	YDQM0		YDQM0	YDQM0		
	YDQM1		YDQM1	YDQM1		

Ball	Name	Type	Func.After Reset	Primary Function	Alternate Function 1	Alternate Function 2
	YCK		YCK	YCK		
	YnCK		YnCK	YnCK		
	YCKE		YCKE	YCKE		
	YnWE		YnWE	YnWE		
	YnRAS		YnRAS	YnRAS		
	YnCAS		YnCAS	YnCAS		
	Yref		Yref	Yref		
	GPIOB[12]/SSPFRM[0]		GPIOB[12]	GPIOB[12]	SSPFRM[0]	
	GPIOB[13]/SSPCLK[0]		GPIOB[13]	GPIOB[13]	SSPCLK[0]	
	GPIOB[14]/SSPRXD[0]		GPIOB[14]	GPIOB[14]	SSPRXD[0]	
	GPIOB[15]/SSPTXD[0]		GPIOB[15]	GPIOB[15]	SSPTXD[0]	
	ADCIN[0]		ADCIN[0]	ADCIN[0]		
	ADCIN[1]		ADCIN[1]	ADCIN[1]		
	ADCIN[2]		ADCIN[2]	ADCIN[2]		
	ADCIN[3]		ADCIN[3]	ADCIN[3]		
	ADCIN[4]		ADCIN[4]	ADCIN[4]		
	ADCIN[5]		ADCIN[5]	ADCIN[5]		
	ADCIN[6]		ADCIN[6]	ADCIN[6]		
	ADCIN[7]		ADCIN[7]	ADCIN[7]		
	ADCREF		ADCREF	ADCREF		
	USBDP		USBDP	USBDP		
	USBDM		USBDM	USBDM		
	UP		UP	UP		
	UM		UM	UM		
	USBREXT		USBREXT	USBREXT		
	USBXO		USBXO	USBXO		
	USBXI		USBXI	USBXI		
	USBTESTA		USBTESTA	USBTESTA		
	XTI		XTI	XTI		
	XTO		XTO	XTO		
	TCK		TCK	TCK		
	nTRST		nTRST	nTRST		
	TDO		TDO	TDO		
	TMS		TMS	TMS		
	TDI		TDI	TDI		
	GPIOB[16]/PVD[8]		GPIOB[16]	GPIOB[16]	PVD[8]	
	GPIOB[17]/PVD[9]		GPIOB[17]	GPIOB[17]	PVD[9]	
	GPIOB[18]/PVD[10]		GPIOB[18]	GPIOB[18]	PVD[10]	
	GPIOB[19]/PVD[11]		GPIOB[19]	GPIOB[19]	PVD[11]	
	GPIOB[20]/PVD[12]		GPIOB[20]	GPIOB[20]	PVD[12]	

Ball	Name	Type	Func.After Reset	Primary Function	Alternate Function 1	Alternate Function 2
	GPIOB[21]/PVD[13]		GPIOB[21]	GPIOB[21]	PVD[13]	
	GPIOB[22]/PVD[14]		GPIOB[22]	GPIOB[22]	PVD[14]	
	GPIOB[23]/PVD[15]		GPIOB[23]	GPIOB[23]	PVD[15]	
	GPIOB[24]/PVD[16]		GPIOB[24]	GPIOB[24]	PVD[16]	
	GPIOB[25]/PVD[17]		GPIOB[25]	GPIOB[25]	PVD[17]	
	GPIOB[26]/PVD[18]		GPIOB[26]	GPIOB[26]	PVD[18]	
	GPIOB[27]/PVD[19]		GPIOB[27]	GPIOB[27]	PVD[19]	
	GPIOB[28]/PVD[20]		GPIOB[28]	GPIOB[28]	PVD[20]	
	GPIOB[29]/PVD[21]		GPIOB[29]	GPIOB[29]	PVD[21]	
	GPIOB[30]/PVD[22]		GPIOB[30]	GPIOB[30]	PVD[22]	
	GPIOB[31]/PVD[23]		GPIOB[31]	GPIOB[31]	PVD[23]	
	GPIOC[0]/nSCS[7]		GPIOC[0]	GPIOC[0]	nSCS[7]	
	GPIOC[1]/nSCS[8]		GPIOC[1]	GPIOC[1]	nSCS[8]	
	GPIOC[2]/nSCS[9]		GPIOC[2]	GPIOC[2]	nSCS[9]	AVCLK
	GPIOC[3]/SSPFRM[1]		GPIOC[3]	GPIOC[3]	SSPFRM[1]	
	GPIOC[4]/SSPCLK[1]		GPIOC[4]	GPIOC[4]	SSPCLK[1]	
	GPIOC[5]/SSPRXD[1]		GPIOC[5]	GPIOC[5]	SSPRXD[1]	
	GPIOC[6]/SSPTXD[1]		GPIOC[6]	GPIOC[6]	SSPTXD[1]	
	GPIOC[7]/PWMOUT[2]		GPIOC[7]	GPIOC[7]	PWMOUT[2]	
	GPIOC[8]/SA[19]		GPIOC[8]	GPIOC[8]	SA[19]	
	GPIOC[9]/SA[20]		GPIOC[9]	GPIOC[9]	SA[20]	
	GPIOC[10]/SA[21]		GPIOC[10]	GPIOC[21]	SA[21]	
	GPIOC[11]/SA[21]		GPIOC[11]	GPIOC[11]	SA[22]	
	GPIOC[12]/SA[21]		GPIOC[12]	GPIOC[12]	SA[23]	
	GPIOC[13]/SA[21]		GPIOC[13]	GPIOC[13]	SA[24]	
	GPIOC[14]/SA[21]		GPIOC[14]	GPIOC[14]	SA[25]	
	GPIOC[15]/nSCS[2]		GPIOC[15]	GPIOC[15]	nSCS[2]	
	GPIOC[16]/nSCS[3]		GPIOC[16]	GPIOC[16]	nSCS[3]	
	GPIOC[17]/nSCS[4]		GPIOC[17]	GPIOC[17]	nSCS[4]	

2.7. System Configuration

Pin Name	Ball	Function Name	Description
GPIOA[2]/PVD[2]		CfgSDRBUSBW0	MCU-A bank data bus width 00 : None 01 : None 10 : 16bit 11 : None
GPIOA[3]/PVD[3]		CfgSDRBUSBW1	
GPIOA[4]/PVD[4]		CfgSDRBW0	SDRAM IC data bus width 00 : None 01 : 8bit 10 : 16bit 11 : None
GPIOA[5]/PVD[5]		CfgSDRBW1	
GPIOA[6]/PVD[6]		CfgSDRCAP0	SDRAM IC Capacity 00 : 64Mbit 01 : 128Mbit 10 : 256Mbit 11 : 512Mbit
GPIOA[7]/PVD[7]		CfgSDRCAP1	
SD[0]		CfgSDRLAT0	SDRAM CAS Latency 00 : 1CL 01 : 2CL 10 : 2.5CL 11: 3CL
SD[1]		CfgSDRLAT1	
SD[3]		CfgSDRREADLAT0	SDRAM Read Latency 00 : 1CL 01 : 2CL 10 : 2.5CL 11 : 3CL
SD[4]		CfgSDRREADLAT1	
SD[5]		CfgBOOTMODE0	Boot Mode 00 : UART 01 : NAND 10 :MEM 11 : None
SD[6]		CfgBOOTMODE1	
SD[7]		CfgSELCS	Select the funcion of Chip Select PAD 0 : NCS[0]_NCS[1] = NCS[0], NNCS[0]_NNCS[1] = NNCS[0], NCS[1]_NCS[0]= NCS[1] NNCS[1]_NNCS[0]= NNCS[1] 1 : NCS[1]_NCS[0] = NCS[0], NNCS[1]_NNCS[0] = NNCS[0], NCS[0]_NCS[1]= NCS[1] NNCS[0]_NNCS[1]= NNCS[1]
SD [8]		CfgNFType0	NAND Flash Address Type 00 : 3Address(Small Block) 01 : 4Address(Small Block) 10 : 4Address(Large Block) 11 : 5Address(Large Block)
SD [9]		CfgNFType1	
SD [10]		CfgBOOTSIZE	UART Boot Size 0 : 512Byte 1 : 16KByte
SD [11]		CfgSTBUSWidth	Static Bus Width 0 : 8bit 1 : 16bit
SD [12]		CfgSTLATADD	Static Latched Address 0 : None 1: Latched
SD [13]		CfgShadow	Shadow mode 0 : Shadow Disable (Static First) 1 : Shadow Enable (DRAM First)
SD [14]		CfgMSBAddr	Static MSB address 0 : GPIOC[14:8] 1 : sa[25:19]

PAD	CfgMSBAddr: 0 CfgSELCS : 0	CfgMSBAddr: 1 CfgSELCS : 0	CfgMSBAddr: 0 CfgSELCS : 1	CfgMSBAddr: 1 CfgSELCS : 1
SA[25:19]	GPIOC[14:8]	SA[25:19]	GPIOC[14:8]	SA[25:19]
nCS[0]_nCS[1] nNCS[0]_nNCS[1]	nCS[0] nNCS[0]	nCS[0] nNCS[0]	nCS[1] nNCS[1]	nCS[1] nNCS[1]
nCS[1]_nCS[0] nNCS[1]_nNCS[0]	nCS[1] nNCS[1]	nCS[1] nNCS[1]	nCS[0] nNCS[0]	nCS[0] nNCS[0]

CHAPTER 3.

ELECTRICAL CHARACTERISTIC

3. ELECTRICAL CHARACTERISTIC

TBD