SONY

Diagonal 6.475 mm (Type 1/2.78) 24.8Mega-Pixel CMOS Image Sensor with Square Pixel for Color Cameras

IMX576-AAKH5-C

General description and application

IMX576-AAKH5-C is a diagonal 6.475 mm (Type 1/2.78) 24.8 Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Sony's back-illuminated and stacked CMOS image sensor to achieve high speed image capturing by column parallel A/D converter circuits and high sensitivity and low noise image (comparing with conventional CMOS image sensor) through the backside illuminated imaging pixel structure. R, G, and B pigment primary color mosaic filter is employed. It operates with three power supply: analog 2.8 V, digital 1.05 V and 1.8 V for input/output interface and achieves low power consumption.
In addition, this product is designed for use in cellular phone and tablet pc. When using this for another application, Sony Semiconductor Solutions Corporation does not guarantee the quality and reliability of product. Therefore, don't use this for applications other than cellular phone and tablet pc. Consult your Sony Semiconductor Solutions Corporation sales representative if you have any questions.

Functions and Features

- ◆ Back-illuminated and stacked CMOS image sensor
- ◆ Quad Bayer Coding color filter arrangement
- ◆ High Frame Rate 30fps@Full resolution(QBC Re-mosaic) / 30fps@QBC-HDR / 120fps@2x2 Adjacent Pixel Binning (4:3)
- ◆ High signal to noise ratio(SNR)
- ◆ Dual sensor synchronization operation
- ◆ Built-in 2D Dynamic Defect Pixel Correction
- ◆ Lens Shading Correction (LSC)
- ◆ Built-in temperature sensor
- ◆ Output video format of RAW10/8, COMP8
- ◆ QBC Re-mosaic function
- ◆ QBC HDR function
- ◆ 2x2 Adjacent Pixel Binning function
- ◆ Two PLLs for independent clock generation for pixel control and data output interface
- ◆ CSI-2 serial data output (MIPI 2lane/4lane, Max. 2.3Gbps/lane, D-PHY spec. ver. 1.2 compliant)
- ◆ 2-wire serial communication (Supports I2C "Fast mode" and "Fast-mode Plus")
- ◆ 9.0 Kbit of OTP ROM for users

E18105C82

Device Structure

- ◆CMOS image sensor
- ◆Image size : Diagonal 6.475 mm (Type 1/2.78)
- ◆Total number of pixels : 5792 (H) × 4464 (V) approx. 25.85 M pixels
- ◆Number of effective pixels : 5792 (H) × 4352 (V) approx. 25.20 M pixels
- ◆Number of active pixels : 5760 (H) × 4312 (V) approx. 24.83 M pixels
- ◆Chip size : 5.848 mm (H) × 5.110 mm (V)
- ◆Unit cell size : 0.9 µm (H) × 0.9 µm (V)
- ◆Substrate material : Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	-0.3 to +4.2	V	refer to VSS level
Supply voltage (digital)	VDIG	-0.3 to +1.54	V	
Supply voltage (interface)	VIF	-0.3 to +2.52	V	
Input voltage (digital)	VI	-0.3 to +2.52	V	
Output voltage (digital)	VO	-0.3 to +2.52	V	
Guaranteed Operating temperature	TOPR	-20 to +70	˚C	
Guaranteed storage temperature	TSTG	-30 to +80	˚C	
Guaranteed performance temperature	TSPEC	-20 to +60	˚C	

Recommended Operating Voltage

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	2.8 ± 0.1	V	refer to VSS level
Supply voltage (digital)	VDIG	1.05 ± 0.1	V	
Supply voltage (interface)	VIF	1.8 ± 0.1	V	

USE RESTRICTION NOTICE

This USE RESTRICTION NOTICE ("Notice") is for customers who are considering or currently using the image sensor products ("Products") set forth in this specifications book. Sony Semiconductor Solutions Corporation ("SSS") may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a SSS subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of SSS on such a use restriction notice when you consider using the Products.

Use Restrictions

- The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by SSS from time to time.
- You should not use the Products for critical applications which may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.
- SSS disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

Design for Safety

- SSS is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Export Control

- If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations. You should be responsible for compliance with the said laws or regulations.

No License Implied

- The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that SSS and its licensors will license any intellectual property rights in such information by any implication or otherwise. SSS will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

Governing Law

- This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

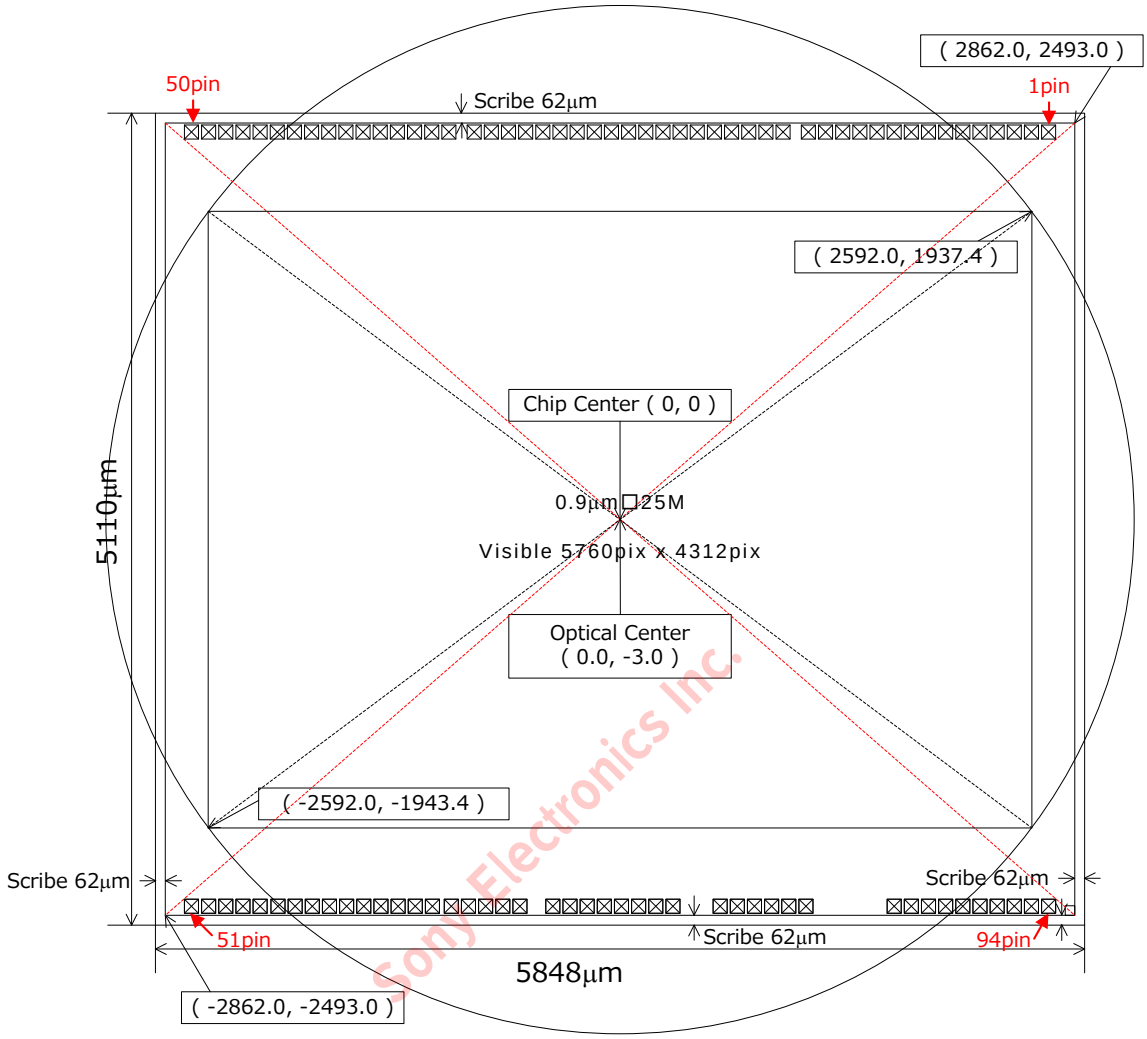
Other Applicable Terms and Conditions

- The terms and conditions in the SSS additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

General-0.0.9

Contents

1. Chip Center and Optical Center



*1 Actual size of a chip will be smaller than indicated when dicing (scribe) is taken into account.

Figure 1 Chip Center and Optical Center (x and y coordinates in µm)

2. Pin Coordinates

Table 1 Pin Coordinates

No.	Symbol	X	Y
1	VPI1	2697.30	2436.25
2	VRL1	2589.30	2436.25
3	VRLRD1	2481.30	2436.25
4	VSSHSN1	2373.30	2436.25
5	VDDHSN1	2265.30	2436.25
6	VDDHDA	2157.30	2436.25
7	VSSHAN	2049.30	2436.25
8	VDDHAN	1941.30	2436.25
9	TVMON	1833.30	2436.25
10	INCK	1725.30	2436.25
11	VDDMIO1	1617.30	2436.25
12	VSSLSC1	1509.30	2436.25
13	VDDLSC1	1401.30	2436.25
14	VSSLSC2	1293.30	2436.25
15	VDDLSC2	1185.30	2436.25
16	VDDMIF	1026.00	2436.25
17	VSSLSC3	918.00	2436.25
18	DMO3P	810.00	2436.25
19	DMO3N	702.00	2436.25
20	DMO1P	594.00	2436.25
21	DMO1N	486.00	2436.25
22	VDDLSC3	378.00	2436.25
23	VDDLIF1	270.00	2436.25
24	VSSLSC4	162.00	2436.25
25	DCKP	54.00	2436.25
26	DCKN	-54.00	2436.25
27	VSSLSC5	-162.00	2436.25
28	VDDLIF2	-270.00	2436.25
29	VDDLSC4	-378.00	2436.25
30	DMO2P	-486.00	2436.25
31	DMO2N	-594.00	2436.25
32	DMO4P	-702.00	2436.25
33	DMO4N	-810.00	2436.25
34	VSSLSC6	-918.00	2436.25
35	VSSLPL1	-1077.30	2436.25
36	VDDLPL1	-1185.30	2436.25
37	VDDLSC5	-1293.30	2436.25
38	VSSLSC7	-1401.30	2436.25
39	VDDLSC6	-1509.30	2436.25
40	VSSLSC8	-1617.30	2436.25
41	VDDLSC7	-1725.30	2436.25
42	VSSLSC9	-1833.30	2436.25
43	VDDLSC8	-1941.30	2436.25
44	VSSLPL2	-2049.30	2436.25
45	VDDLPL2	-2157.30	2436.25
46	VSSHSN2	-2265.30	2436.25
47	VDDHSN2	-2373.30	2436.25
48	VRLRD2	-2481.30	2436.25
49	VRL2	-2589.30	2436.25

No.	Symbol	X	Y
50	VPI2	-2697.30	2436.25
51	VDDLSC9	-2697.30	-2436.25
52	VSSLSC10	-2589.30	-2436.25
53	VDDLSC10	-2481.30	-2436.25
54	VSSLSC11	-2373.30	-2436.25
55	VDDMIO2	-2265.30	-2436.25
56	SDA	-2152.80	-2436.25
57	SCL	-2044.80	-2436.25
58	GYINT	-1936.80	-2436.25
59	SCSB	-1828.80	-2436.25
60	SCK	-1720.80	-2436.25
61	SDO	-1612.80	-2436.25
62	SDI	-1504.80	-2436.25
63	SLASEL	-1396.80	-2436.25
64	GPO	-1288.80	-2436.25
65	SWTCK	-1180.80	-2436.25
66	VSSHSN3	-1062.00	-2436.25
67	VDDHSN3	-954.00	-2436.25
68	VDDHCM1	-846.00	-2436.25
69	VSSLCN1	-738.00	-2436.25
70	VDDLCN1	-630.00	-2436.25
71	TESTOUT / S_SDO	-423.00	-2436.25
72	TEST1 / S_SCSB	-315.00	-2436.25
73	TEST2 / S_SCK	-207.00	-2436.25
74	TEST3 / S_SDI	-99.00	-2436.25
75	SWDIO / S_GYINT	9.00	-2436.25
76	VDDMIO3	117.00	-2436.25
77	VSSLSC12	225.00	-2436.25
78	VDDLSC11	333.00	-2436.25
79	VDDLCN2	630.00	-2436.25
80	VSSLCN2	738.00	-2436.25
81	VDDHCM2	846.00	-2436.25
82	VDDHSN4	954.00	-2436.25
83	VSSHSN4	1062.00	-2436.25
84	VDDSUB	1170.00	-2436.25
85	XVS	1725.30	-2436.25
86	TENABLE	1833.30	-2436.25
87	XCLR	1941.30	-2436.25
88	FSTROBE	2049.30	-2436.25
89	POREN	2157.30	-2436.25
90	VDDMIO4	2265.30	-2436.25
91	VSSLSC13	2373.30	-2436.25
92	VDDLSC12	2481.30	-2436.25
93	VSSLSC14	2589.30	-2436.25
94	VDDLSC13	2697.30	-2436.25

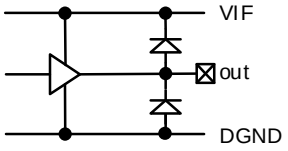
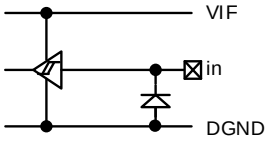
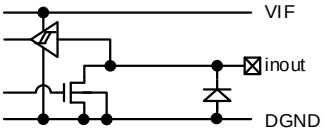
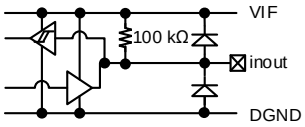
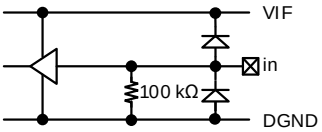
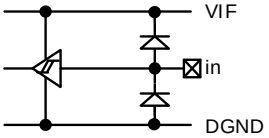
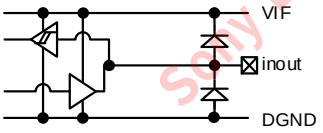
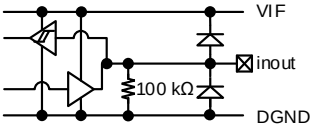
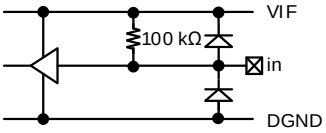
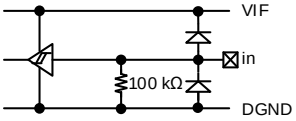
3. Pin Description

Table 2 Pin Description

No.	Symbol	I/O	A/D	Description	Remarks
1	VPI1	Power	A	analog input	Connect VPI2
2	VRL1	Minus	A	analog input	Connect VRL2
3	VRLRD1	Minus	A	analog input	Connect VRLRD2
4	VSSHSN1	GND	A	VANA GND	
5	VDDHSN1	Power	A	VANA power supply	
6	VDDHDA	Power	A	VANA power supply	
7	VSSHAN	GND	A	VANA GND	
8	VDDHAN	Power	A	VANA power supply	
9	TVMON	O	A	analog output	NC
10	INCK	I	D	digital input	Clock Input
11	VDDMIO1	Power	D	VIF power supply	
12	VSSLSC1	GND	D	VDIG GND	
13	VDDLSC1	Power	D	VDIG power supply	
14	VSSLSC2	GND	D	VDIG GND	
15	VDDLSC2	Power	D	VDIG power supply	
16	VDDMIF	Power	D	VIF power supply	
17	VSSLSC3	GND	D	VDIG GND	
18	DMO3P	O	D	Digital output	MIPI output (DATA+)
19	DMO3N	O	D	Digital output	MIPI output (DATA–)
20	DMO1P	O	D	Digital output	MIPI output (DATA+)
21	DMO1N	O	D	Digital output	MIPI output (DATA–)
22	VDDLSC3	Power	D	VDIG power supply	
23	VDDLIF1	Power	D	VDIG Power supply	
24	VSSLSC4	GND	D	VDIG GND	
25	DCKP	O	D	Digital output	MIPI output (CLK+)
26	DCKN	O	D	Digital output	MIPI output (CLK-)
27	VSSLSC5	GND	D	VDIG GND	
28	VDDLIF2	Power	D	VDIG Power supply	
29	VDDLSC4	Power	D	VDIG power supply	
30	DMO2P	O	D	Digital output	MIPI output (DATA+)
31	DMO2N	O	D	Digital output	MIPI output (DATA–)
32	DMO4P	O	D	Digital output	MIPI output (DATA+)
33	DMO4N	O	D	Digital output	MIPI output (DATA–)
34	VSSLSC6	GND	D	VDIG GND	
35	VSSLPL1	GND	D	VDIG GND	
36	VDDLPL1	Power	D	VDIG Power supply	
37	VDDLSC5	Power	D	VDIG power supply	
38	VSSLSC7	GND	D	VDIG GND	
39	VDDLSC6	Power	D	VDIG power supply	
40	VSSLSC8	GND	D	VDIG GND	
41	VDDLSC7	Power	D	VDIG power supply	
42	VSSLSC9	GND	D	VDIG GND	
43	VDDLSC8	Power	D	VDIG power supply	
44	VSSLPL2	GND	D	VDIG GND	
45	VDDLPL2	Power	D	VDIG Power supply	
46	VSSHSN2	GND	A	VANA GND	
47	VDDHSN2	Power	A	VANA power supply	
48	VRLRD2	Minus	A	analog input	Connect VRLRD1

No.	Symbol	I/O	A/D	Description	Remarks
49	VRL2	Minus	A	analog input	Connect VRL1
50	VPI2	Power	A	analog input	Connect VPI1
51	VDDLSC9	Power	D	VDIG power supply	
52	VSSLSC10	GND	D	VDIG GND	
53	VDDLSC10	Power	D	VDIG power supply	
54	VSSLSC11	GND	D	VDIG GND	
55	VDDMIO2	Power	D	VIF power supply	
56	SDA	I/O	D	digital I/O	I^2C serial communication
57	SCL	I/O	D	digital I/O	I^2C serial communication
58	GYINT	I	D	digital input	Gyro interrupt (or pull-down external)
59	SCSB	I/O	D	digital I/O	Gyro chip select (or NC)
60	SCK	I/O	D	digital I/O	Gyro control clock (or NC)
61	SDO	I/O	D	digital I/O	Gyro data output (or NC)
62	SDI	I/O	D	digital I/O	Gyro data input (or pull-down external)
63	SLASEL	I	D	digital input	I^2C slave address select Pull down (pull-down internal)
64	GPO	O	D	digital output	
65	SWTCK	I/O	D	digital I/O	NC (pull-down internal)
66	VSSHSN3	GND	A	VANA GND	
67	VDDHSN3	Power	A	VANA power supply	
68	VDDHCM1	Power	A	VANA power supply	
69	VSSLCN1	GND	D	VDIG GND	
70	VDDLCN1	Power	D	VDIG power supply	
71	TESTOUT / S_SDO	O	D	digital output	Gyro data output
72	TEST1 / S_SCSB	I	D	digital input	SPI Communication for OIS control (or pull-down external)
73	TEST2 / S_SCK	I	D	digital input	SPI Communication for OIS control (or pull-down external)
74	TEST3 / S_SDI	I/O	D	digital I/O	SPI Communication for OIS control (or pull-down external)
75	SWDIO / S_GYINT	I/O	D	digital I/O	Gyro interrupt output signal (pull-up internal)
76	VDDMIO3	Power	D	VIF power supply	
77	VSSLSC12	GND	D	VDIG GND	
78	VDDLSC11	Power	D	VDIG power supply	
79	VDDLCN2	Power	D	VDIG power supply	
80	VSSLCN2	GND	D	VDIG GND	
81	VDDHCM2	Power	A	VANA power supply	
82	VDDHSN4	Power	A	VANA power supply	
83	VSSHSN4	GND	A	VANA GND	
84	VDDSUB	Power	A	VANA power supply	
85	XVS	I/O	D	digital I/O	for dual sync (pull-up internal)
86	TENABLE	I	D	digital input	NC (pull-down internal)
87	XCLR	I	D	digital input	Chip clear (pull-down internal)
88	FSTROBE	O	D	digital output	Flash strobe
89	POREN	I	D	digital input	NC (pull-up internal)
90	VDDMIO4	Power	D	VIF power supply	
91	VSSLSC13	GND	D	VDIG GND	
92	VDDLSC12	Power	D	VDIG power supply	
93	VSSLSC14	GND	D	VDIG GND	
94	VDDLSC13	Power	D	VDIG power supply	

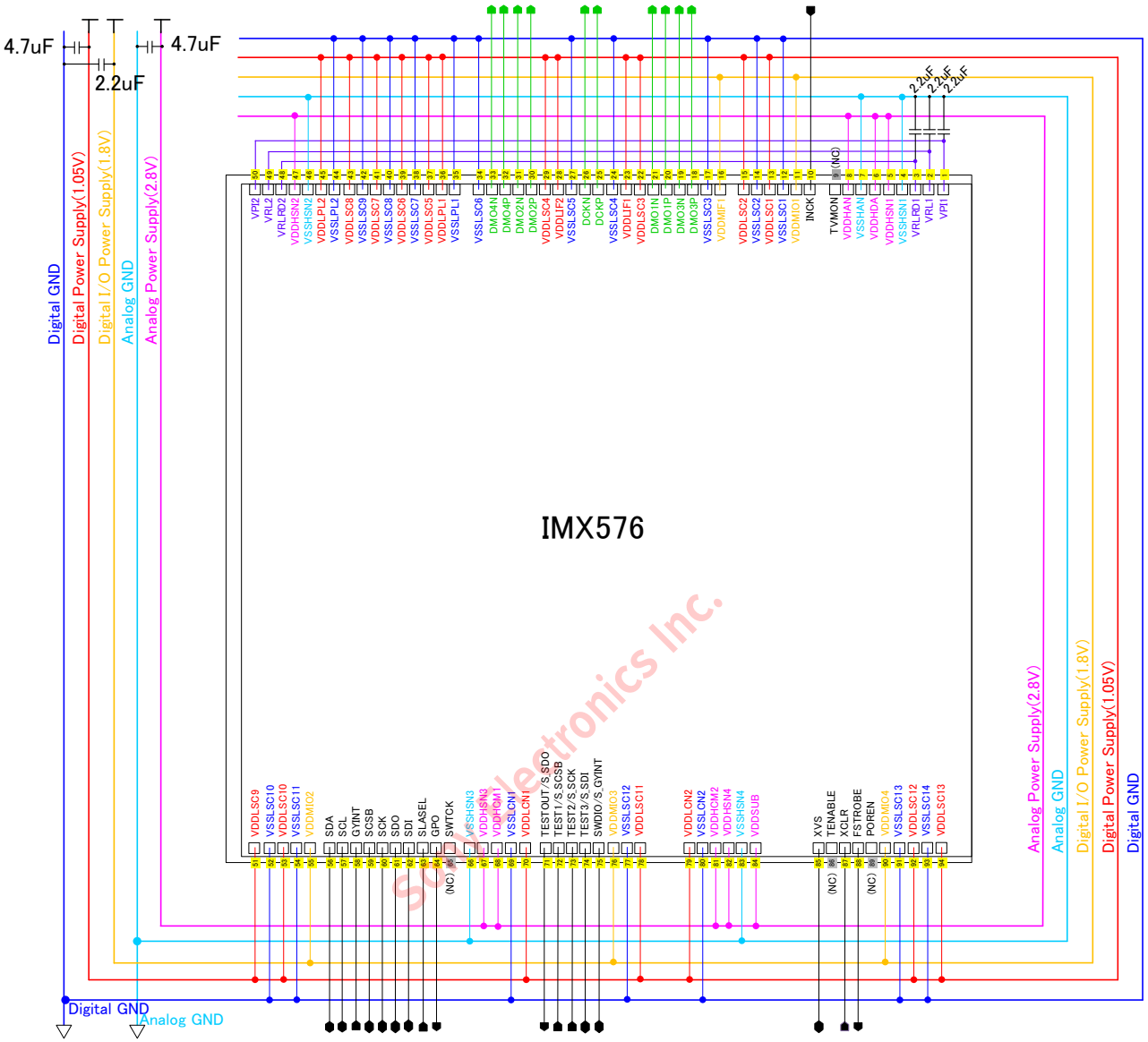
4. Input / Output Equivalent Circuit

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
FSTROBE GPO TESTOUT / S_SDO		INCK	
SCL SDA		XVS SWDIO / S_GYINT	
SLASEL XCLR		GYINT TEST1/S_SCSB TEST2/S_SCK	
SDI SCSB SCK SDO TEST3/S_SD I		SWTCK	
POREN		TENABLE	

VIF : 1.8 V power supply
DGND : VDIG GND

Figure 2 Input / Output Equivalent Circuit

5. Peripheral Circuit Diagram



Note: Back side or substrate of the sensor chip has a contact with Digital GND (VSSLSC) internally by following the above schematics. No other additional or intentional electrical contact is necessary.

Note: The capacitor values and parts count used for decoupling of power supply lines in this diagram are determined only with Sony Semiconductor Solutions Corporation's testing environment. The capacitor values and/or parts count for power line decoupling may have to be reviewed and optimized by each manufacture depending on their design.

Figure 3 Peripheral Circuit (Recommended schematics)

6. Functional Description

6-1 System Outline

IMX576-AAKH5-C is a CMOS active pixel type image sensor which adopts Sony's back-illuminated and stacked CMOS image sensor to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions. Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.
A onetime programmable memory is embedded in the chip for storing the user data. It has 9.0K-bit for user, 32 K-bit as a whole.

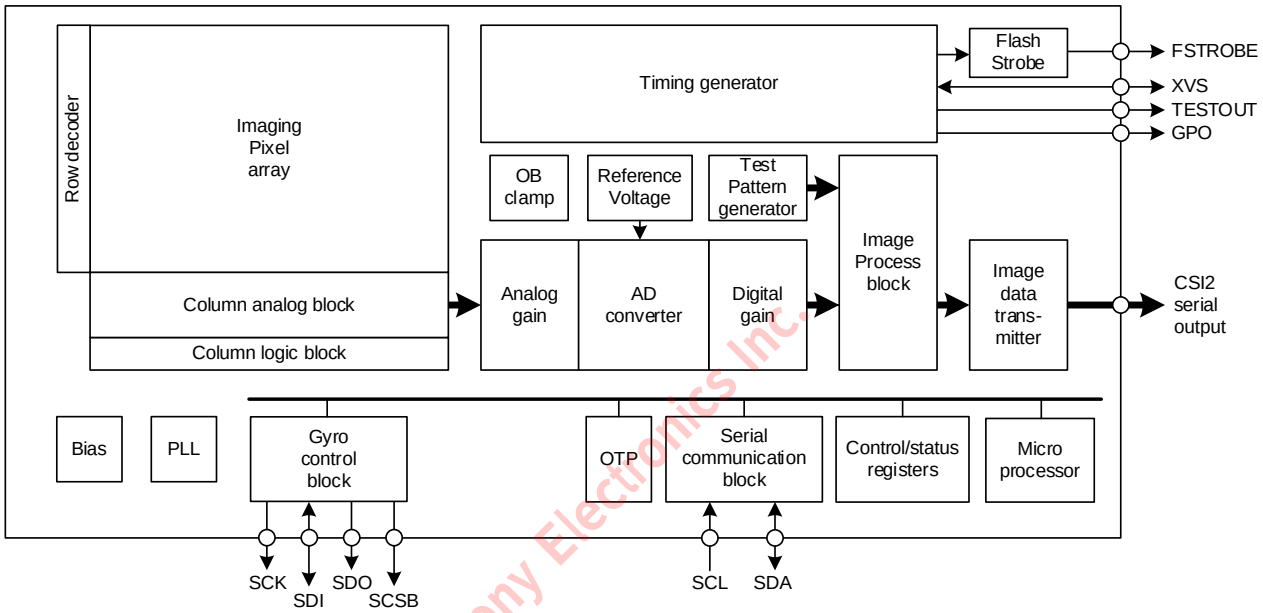


Figure 4 Overview of functional block diagram

6-2 Control register setting by the serial communication

The IMX576-AAKH5-C can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows. See Application Notes for more details of each function beyond the following description.

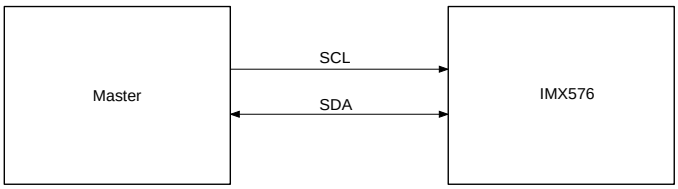


Figure 5 2-wire serial communication

6-2-1 2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I^2C fast-mode compatible interface, and the data transfer protocol is I^2C standard. IMX576-AAKH5-C supports two transfer speed mode (Fast-mode ≤400 kHz, Fast-mode Plus* ≤1 MHz).
This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX576-AAKH5-C.
*only available with INCK ≥ 14.5 MHz

Table 3 Description of 2-wire Serial Communication Pins

pin name	description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of IMX576-AAKH5-C are mapped on the 16-bit address space and the register categories shown as below. Detail register information is shown in Register Map.

Table 4 Specification of register address map for 2-wire serial communication

	address range	description
I^2C register	0x0000 - 0x0fff	Configuration register Read Only and Read/Write Dynamic register
	0x1000 - 0x1fff	Parameter limit register Read only static register
	0x2000 - 0x2fff	Reserved
	0x3000 - 0xffff	Manufacture specific register

6-2-2 Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

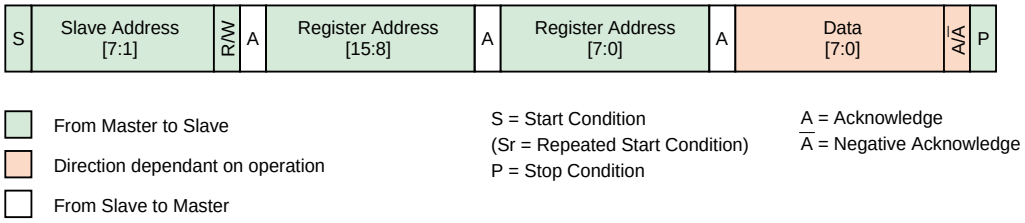
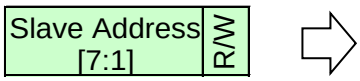


Figure 6 2-wire serial communication protocol

IMX576-AAKH5-C has a default slave address shown as below.
The slave address is selectable by pin connection of SLASEL.
When called by the selected slave address, serial communication interface is activated.
Duplication of the address on the same bus must be prevented.
For other slave address options, refer to Application Note.



Slave Address (Read or Write) * See Table 5 for R/W bit	SLASEL (pin#63)
MSB LSB 0 0 1 1 0 1 0 R/W	L or NC
MSB LSB 0 0 1 0 0 0 0 R/W	H

R/W shows the direction of communication.

Figure 7 Slave address

Table 5 R/W bit

R/W bit	direction of communication
0	Write (Master → Sensor)
1	Read (Sensor → Master)

6-3 Clock generation and PLL

IMX576-AAKH5-C equips embedded PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation condition. See Application Notes for more details of each function.

6-3-1 Clock System Diagram

IMX576-AAKH5-C is equipped with two PLLs, One outputs IVTCK for image processing, the other is IOPSYCK for MIPI output.
The IVTCK PLL can output at 1050 to 2100 MHz, and the IOPCK PLL can output at 1250 to 2300 MHz, based on a clock input with the 6 to 27 MHz range.

The IVTCK PLL could be configured with divider of up to 1/1 to 1/4 range, and multiply in the 87 to 350 range.
The IOPCK PLL could be configured with divider of up to 1/1 to 1/15 range, and multiply in the 47 to 2300 range.

Typically, IMX576-AAKH5-C can be driven from the single PLL mode to move only one side of the PLL (IOPCK PLL), but it also supports dual PLL mode to operate the both of PLLs.

In PLL single mode, IOP_PREPLLCK_DIV and IOP_PLL_MPY are ignored.

.

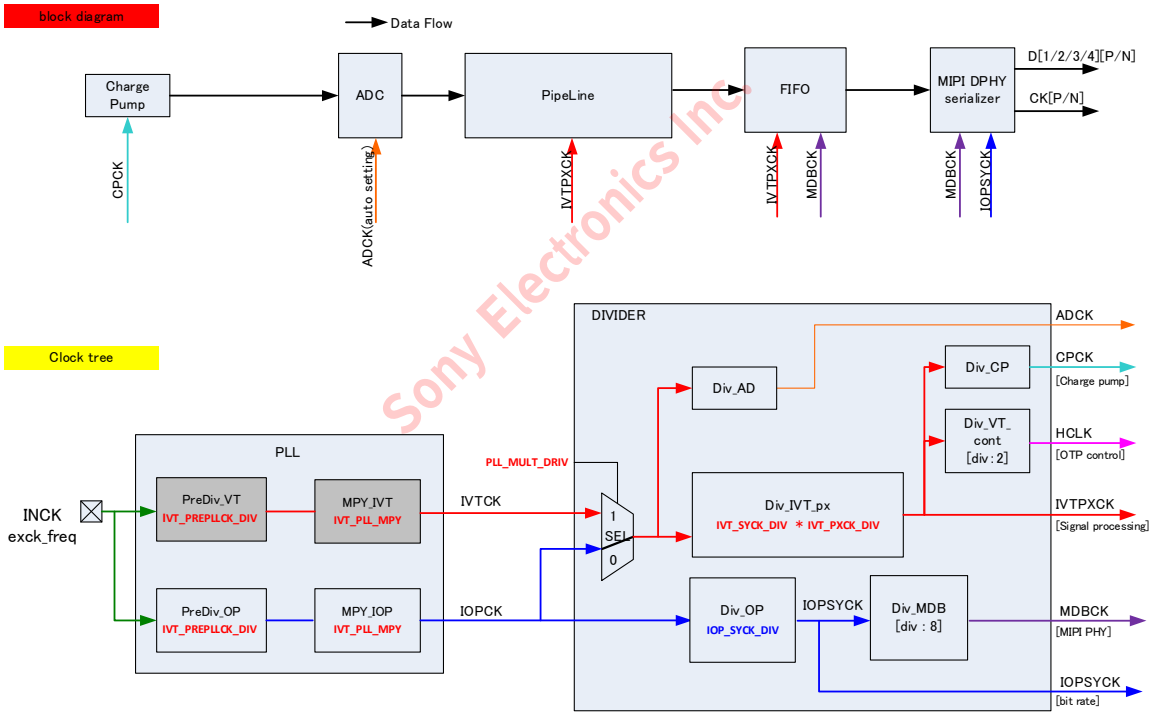


Figure 8 Clock System Diagram (PLL single mode)

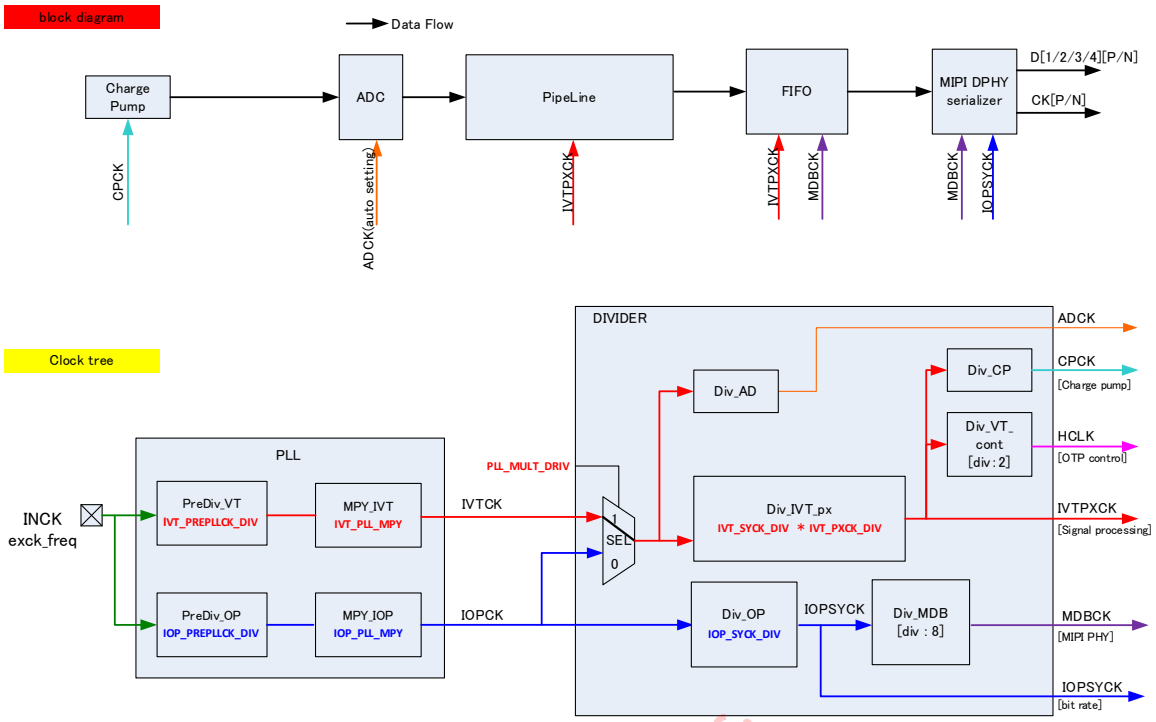


Figure 9 Clock System Diagram (PLL dual mode)

6-4 Description of operation clocks

The followings are general descriptions for each clock. See Application Note for more detail.

6-4-1 INCK

INCK is an external input clock (6 to 27MHz). See “AC characteristics” for electrical requirements to INCK.

6-4-2 IVTCK, IOPCK(PLL output)

These clocks are the root of all the operation clocks in IMX576-AAKH5-C and it designates the data rate. DCKP/DCKN; CSI2 interface clock is generated from IOPCK by dividing into 1/2 frequency since the interface is operated in double data rate format.

6-4-3 IVTPXCK Clock

The clock for internal image processing is used as the base of integration time, frame rate, and etc.

6-4-4 IOPSYCK Clock

The clock for internal image processing is designating the pixel rate and etc.

6-5 Image Readout Operation

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, IMX576-AAKH5-C outputs the image data.

See Application Notes for more details of each function.

6-5-1 Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with pin #1 located at the upper right corner.

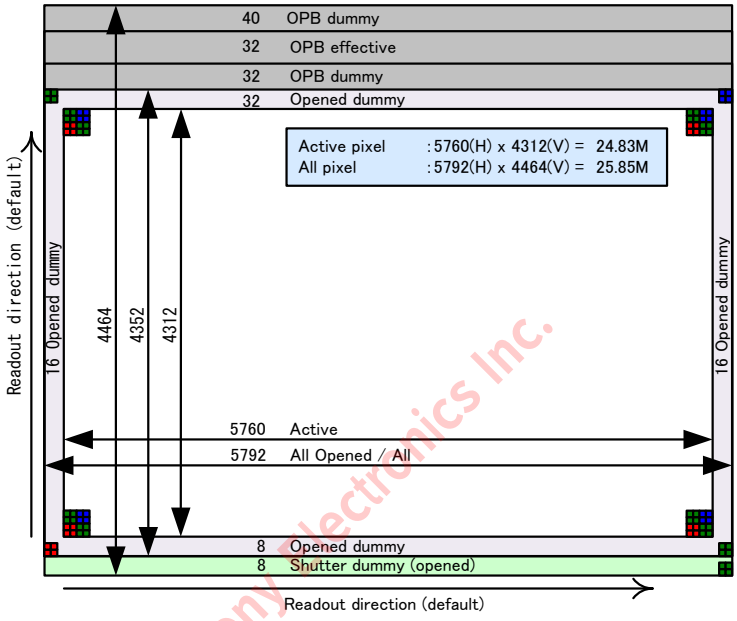


Figure 10 physical alignment of the imaging pixel array

6-5-2 Color coding and order of reading image date

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals respectively. The line with R and Gr signals and the line with Gb and B signals are output alternating one after the other.

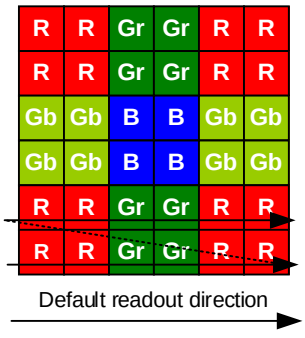


Figure 11 Color coding alignment (Quad Bayer Coding)

6-6 Output Image Format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

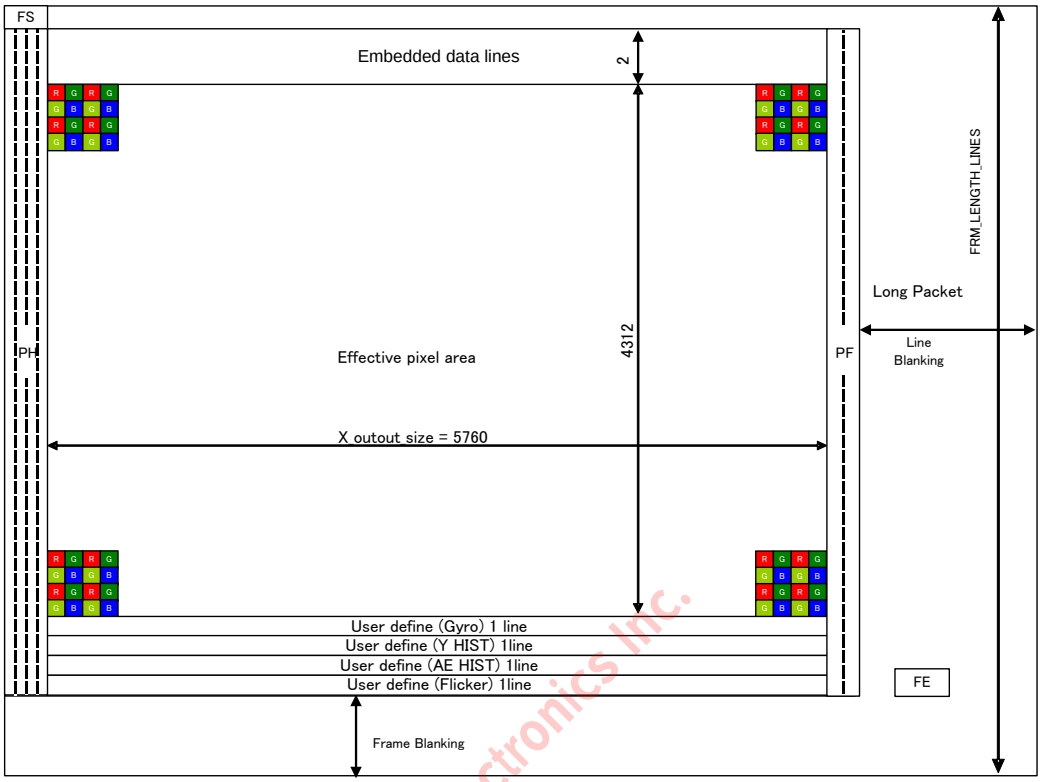


Figure 12 Full pixel output mode data structure

6-6-1 Embedded data line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame. The corresponding registers are indicated by “EDL” column of the Register Map.
An unfixed value is output when not outputting embedded data.

See Application Notes for contents and output sequence of Embedded Data Lines.

6-6-2 STATS data control

STATS data (Y HIST, AE HIST, Flicker) can be output as a packet different from normal image data during the frame blanking period.

6-6-3 Gyro data control

Gyro data is retrieved from an external Gyro IC sampling data, and output in the embedded data line.

6-6-4 Image size of mode

IMX576-AAKH5-C can capture and output full size, cropped/scaled image in combination with the normal mode. Examples are shown in the table below. Definitions of each parameter are shown in the below figure.

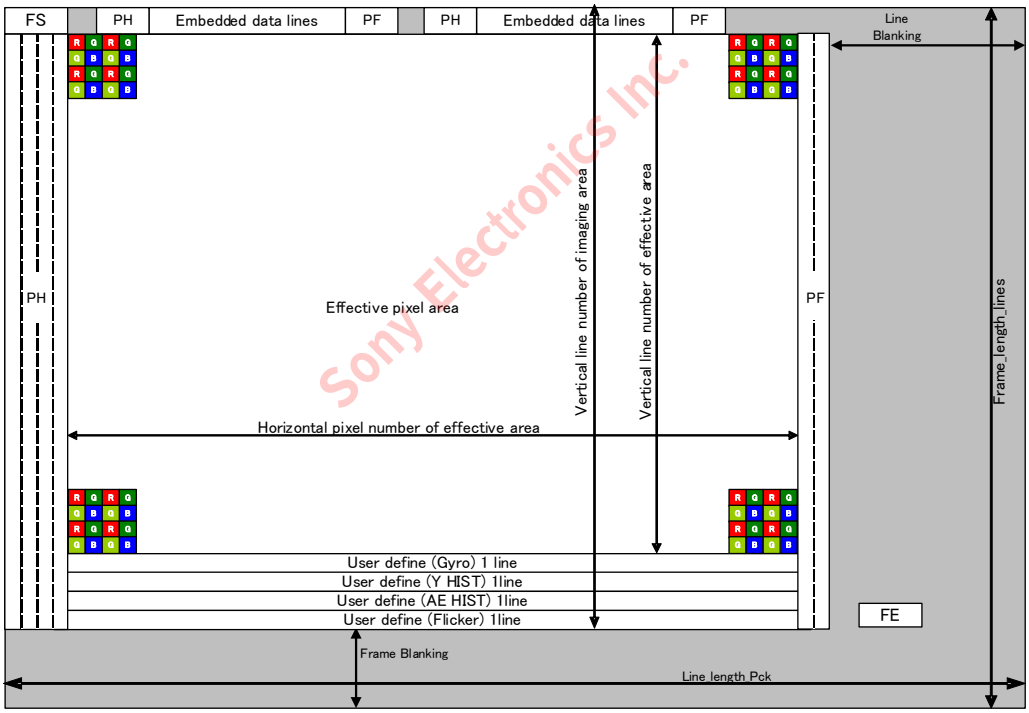


Figure 13 Image size parameter definition

Table 6 modes and image sizes

	Modes		
	Full size (QBC Re-mosaic)	QBC-HDR	2x2 Adjacent Pixel Binning
Cropping	Non(4:3)	Non(4:3)	Non(4:3)
Binning	Non	Non	H/V
Scaling	Non	Non	Non
H Pixels	5760	2880	2880
V Pixels	4312	2156	2156
Frame Rate	30fps	30fps	120fps
FOV			
Output			

6-6-5 Available operation mode

IMX576-AAKH5-C has three modes that All-pixel, QBC-HDR, and 2x2 Adjacent Pixel Binning.

6-6-6 Image area control capabilities

As control function for image's viewing area and /or image size, IMX576-AAKH5-C has capability of analog crop, digital crop, scaling and output crop. The relation of image output size and the resister is shown below.
In this sensor, Horizontal analog cropping is prohibited.

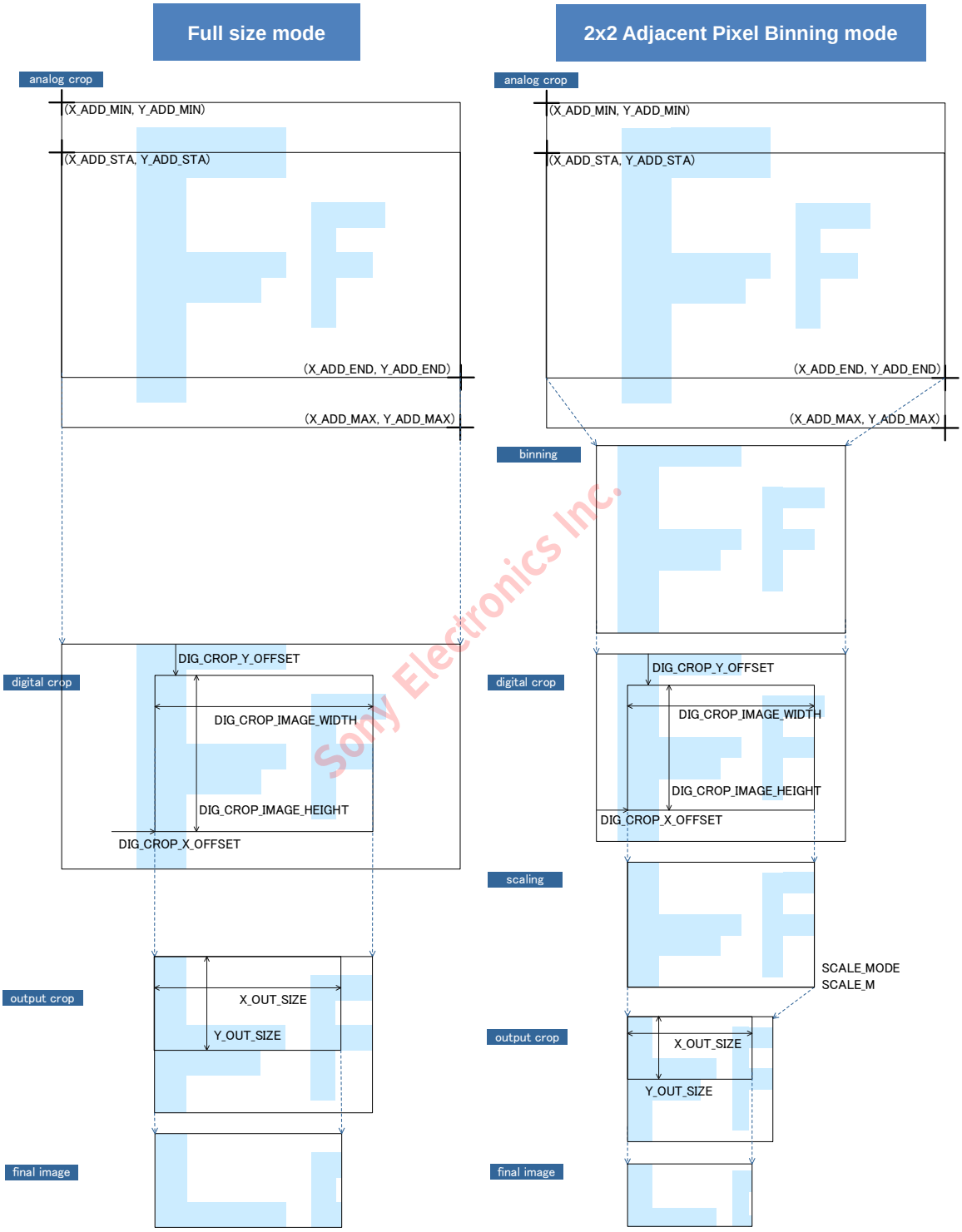


Figure 14 image area control capabilities

Readout Start Position

Default readout position of IMX576-AAKH5-C starts from the lower left when PIN1 is placed at the upper right corner. Because the lens will invert the image both vertically and horizontally, the proper image can be archived when PIN1 is placed at the upper right corner.

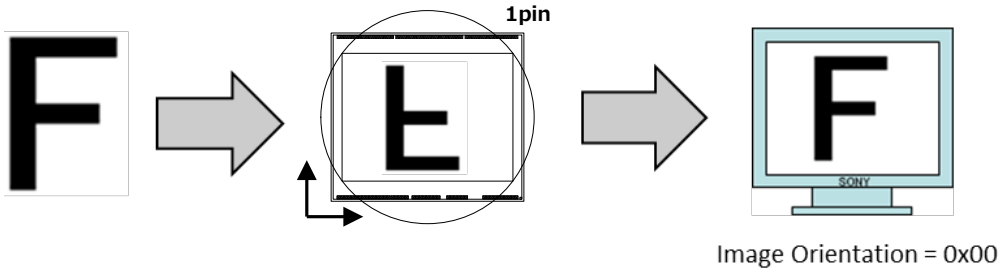


Figure 15 Readout start position

Vertical flip and horizontal mirror readout modes can be specified by the register below. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image. When changing the readout direction, the color of first readout pixel (R/Gr/Gb/B) also changes with it.

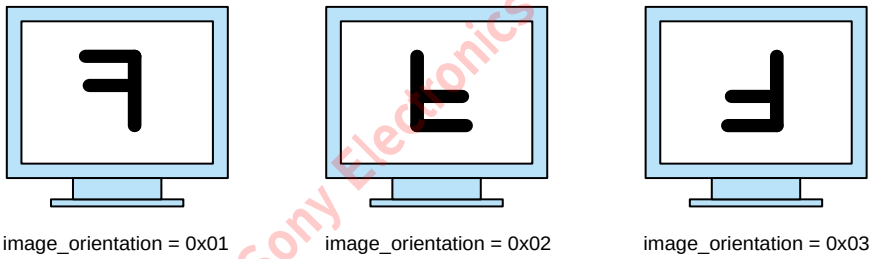


Figure 16 Read out image for each combination of flip and mirror

6-7 Gain setting

IMX576-AAKH5-C can apply analog gain on photo-electron signal and digital gain on digital signal after ADC. Range of settable range is as follows.

Table 7 Range of Gains

Function	Min	Max.	Note
Analog Gain	0 dB	24 dB	-
Digital Gain	0 dB	24 dB	Functionally Settable

6-8 Image compensation function

There are some additional functions in sensor image pipeline. Use-case may be chosen in terms of trade-off for power consumption and image quality for example.
See Application Notes for more details of each function.

6-8-1 Defect Pixel Correction

The defect correction function includes static defect correction and dynamic defect correction.
The static defect correction is to correct the defective pixels according to address data stored in OTP.
There is only area for Sony Semiconductor Solutions Corporation's factory area.
The dynamic defect correction eliminates any critical defects detected on RGB array by estimating from surrounding adjacent pixels value.

6-8-2 Lens Shading Correction (LSC)

Lens Shading Correction (LSC) is a function to compensate degraded illumination toward the edge of an image.

6-9 Miscellaneous functions

IMX576-AAKH5-C has the following additional functions to be used for various final products' features.
See Application Notes for more details of each function.

6-9-1 Thermal Meter

This function is to measure the thermal data from internal sensor then average it. Measurement results could be read via I^2C or EBD data.

6-9-2 Test pattern output

IMX576-AAKH5-C can output the following test pattern by build-in pattern generator.
Test patterns of Solid Color, 100% Color Bar, Fade to Gray Color Bar, PN9 are available.
For Solid Color mode, each value of R, Gr, Gb and B is adjustable.

6-9-3 Long Exposure Setting

IMX576-AAKH5-C can achieve a very long exposure time (up to 128 times of 1 vertical period) by simply expanding the vertical blanking time setting.

6-9-4 OTP (One Time Programmable Read Only Memory)

Total of 9.0 Kbit of OTP is available for users.
It is divided into 18 pages and 448 byte of them are usable at user's discretion while other 704 byte are assigned as the area for the particular purpose like defective pixel correction, model ID, etc., and partially write protected.
See OTP manual for details.

6-9-5 Multi sensor synchronization operation

IMX576-AAKH5-C supports synchronized shooting operation of two image sensors by implementing both slave and master mode for each sensor. To enable this feature, master/slave must be set for each sensor by software control method. XVS is dedicated signal for the synchronization.

6-9-6 Flash light control sequence

IMX576-AAKH5-C can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins (FSTROBE).

6-9-7 Monitor terminal settings

IMX576-AAKH5-C can output three internal signals (H Sync/V Sync/OIS pulse) via monitor terminals.
The monitor terminals mean the following two terminals, such as GPO and TESTOUT.

6-10 Image signal interface

6-10-1 MIPI transmitter

IMX576-AAKH5-C outputs image signal by CSI2 high speed serial interface consisted of one pair of clock line and four pairs of data line. See MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) version 1.2 and MIPI Alliance Specification for D-PHY version 1.2 for details.

Because signal is transmitted by differential pair, impedance (generally 100 Ω) between differential pair near the receiver side during HS mode is required. Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

7. How to operate IMX576-AAKH5-C

7-1 Power on Reset

IMX576-AAKH5-C does not support the built in “Power On Reset” function.
XCLR pin is set to “LOW” and the power supplies are brought up. Then XCLR pin should be set to “High” after INCK supplied.

7-2 Power on sequence

7-2-1 Power on slew rate

Maximum slew rate (mV/μs) is specified for each power supply to avoid oscillation during power on.

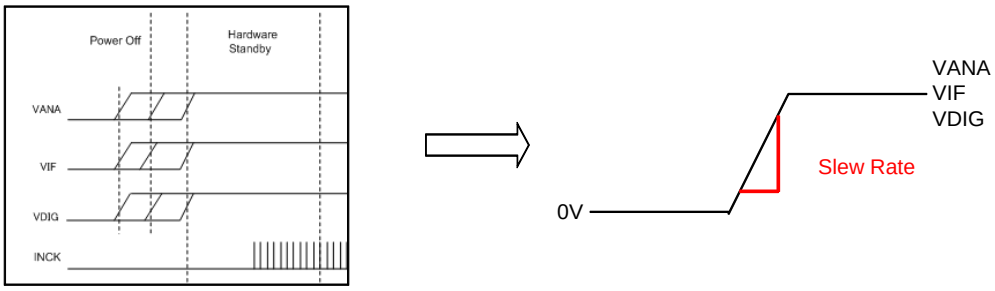


Figure 17 Power on slew rate

Table 8 Limitation on power-on slew rate

Power Supplies	Slew Rate			Comment
	Min	Max	Unit	
VANA, VIF, VDIG	-	100	mV/μs	

7-2-2 Startup sequence with 2-wire serial communication

Follow the power supply start up sequence as below.

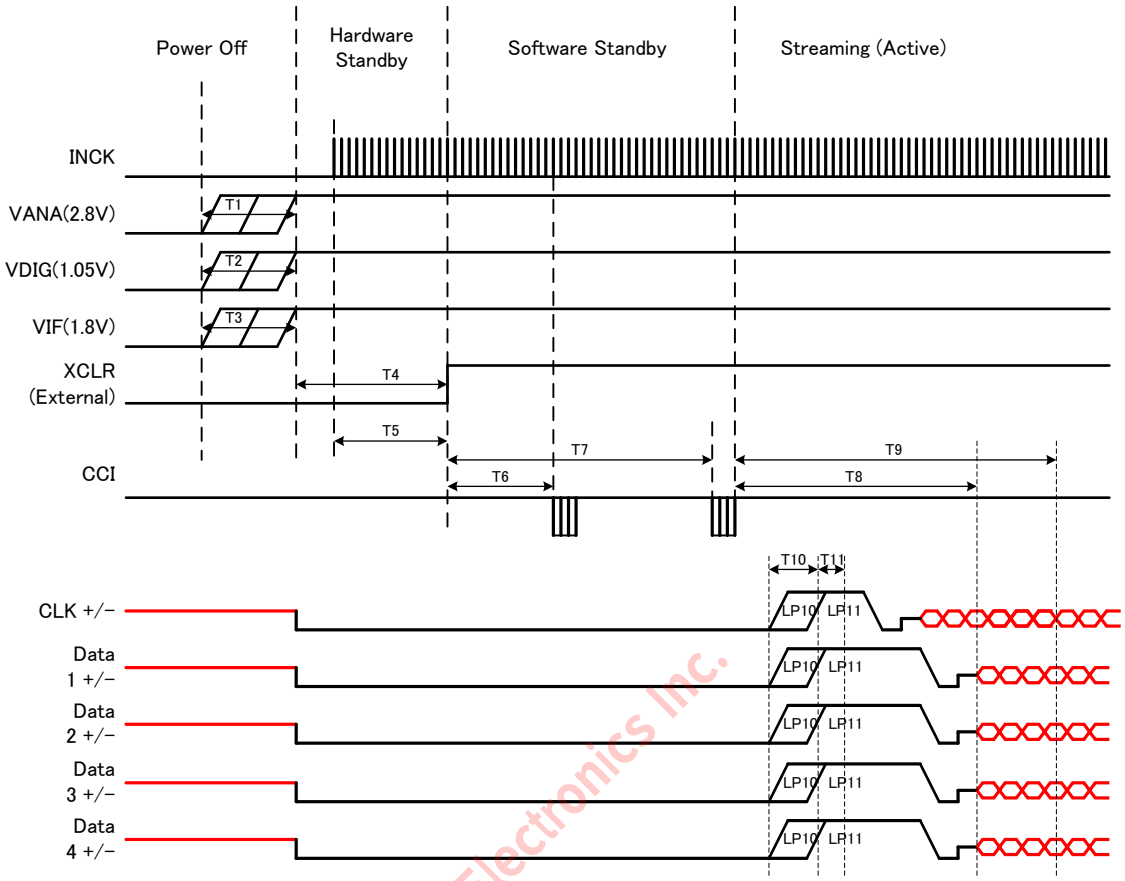


Figure 18 Startup sequence with 2-wire serial communication

* Presence of INCK during Power Off is acceptable despite of above chart.

Table 9 Startup sequence timing constraints

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA on	T1	VANA, VDIG and VIF may rise in any order.		µs	Slew rate of VANA, VDIG and VIF(0%-100%) : max 100mV/us
VDIG rising – VDIG on	T2			µs	
VIF rising – VIF on	T3			µs	
VANA, VDIG and VIF rising – XCLR rising	T4	0		µs	Later of T1, T2 and T3
INCK start - XCLR rising	T5	0		ms	
INCK start and XCLR rising till CCI Read version ID register wait time	T6	1		ms	
INCK start and XCLR rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	8		ms	
Start of first streaming from Sending Streaming Command.	T8		3.0 ms + The delay of the coarse integration time value + (Tline * 56[lines])		IVTPXCK = 210MHz INCK = 6MHz
			5.0 ms + The delay of the coarse integration time value + (Tline * 56[lines])		IVTPXCK = 60MHz INCK = 6MHz
Start of first streaming with valid frame after power-on sequence.	T9		T8 + 1Frame	Frames	
DPHY power up	T10	1	1.1	ms	
DPHY init	T11	100	110	µs	

Note : XCLR needs to be Low until all power supplies complete power-on

7-3 Power down sequence

7-3-1 Power down sequence with 2-wire serial communication

Follow the power down sequence below.

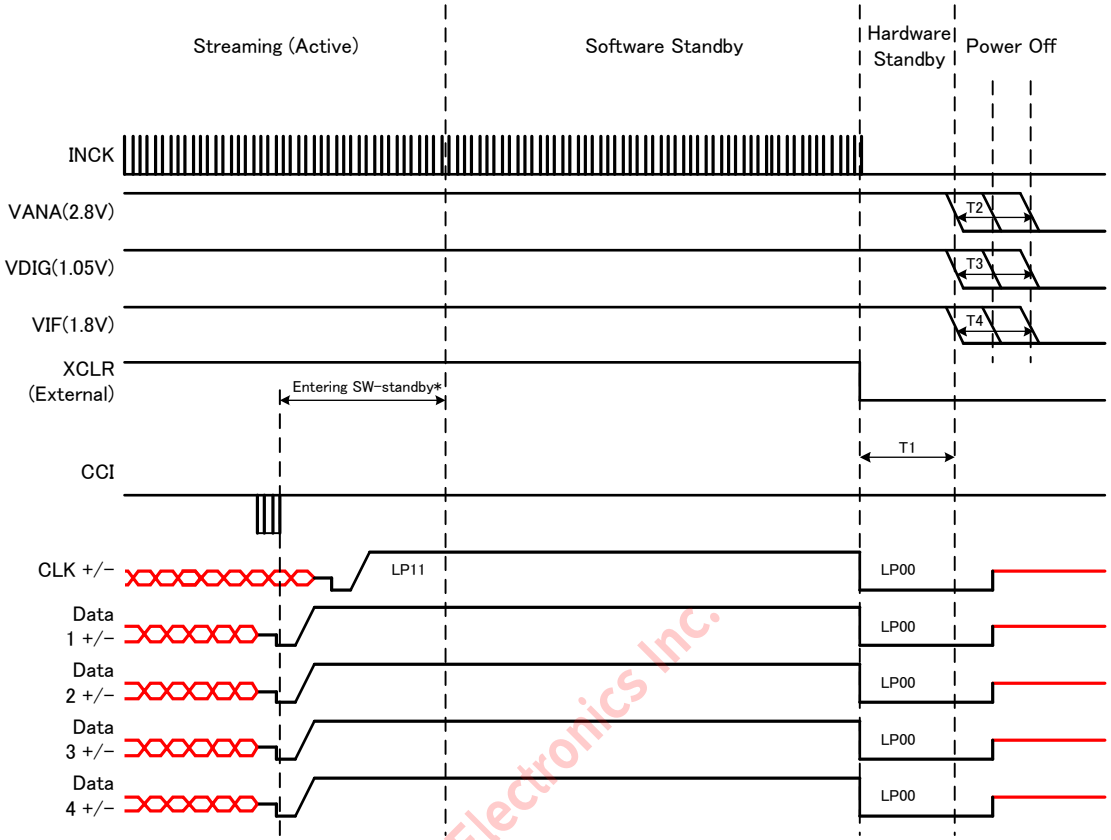


Figure 19 Power down sequence with 2-wire serial communication

Table 10 Power down sequence timing constraints

Item	Label	Min.	Max.	Unit	Comment
XCLR Neg-edge – VANA(VDIG or VIF) fall	T1	0		μs	Presence of INCK during Power Off is acceptable.
Sequence free of VANA falling and VDIG falling and VIF falling	T2,T3,T4	VANA, VDIG and VIF may fall in any order.		μs	

7-4 Register Map

See “Register Map document”.

8. Electrical Characteristics

The Electrical Characteristics of the IMX576-AAKH5-C is shown below

8-1 DC characteristics

Table 11 DC Characteristics

Item	Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDDSUB VDDHSN1,2,3,4 VDDHAN VDDHDA VDDHCM1,2	VANA	2.7	2.8	2.9	V
	VDDLCN1,2 VDDLSC1,2,3,4,5,6,7,8,9,10,11,12,13 VDDLIF1,2 VDDLPL1,2	VDIG	0.95	1.05	1.15	V
	VDDMIO1,2,3,4 VDDMIF	VIF	1.7	1.8	1.9	V
Digital input voltage	SDA, SCL	VIH	0.7VIF		2.9	V
		VIL	-0.3		0.3VIF	V
Digital input voltage	XCLR, INCK, GYINT, SDI, TEST1/S_SCSB, TEST2/S_SCK, TEST3/S_SDI, SLASEL, XVS	VIH	0.65VIF		VIF+0.3	V
		VIL	-0.3		0.35VIF	V
Digital output voltage	SDA	VOL	-		0.2VIF	V
	GPO, FSTROBE, XVS, TESTOUT, SCK, SDI, SDO, SCSB	VOH	VIF-0.2		-	V
		VOL	-		0.2	V

8-2 AC Characteristics

8-2-1 Master Clock Waveform Diagram

8-2-1-1 INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.

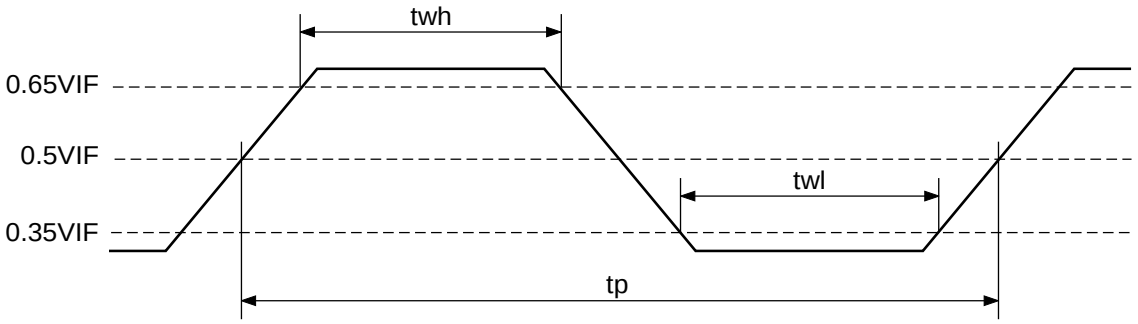


Figure 20 Master Clock Square Waveform Input Diagram

Table 12 Master Clock Square Waveform Input Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{SCK}	6		27	MHz
INCK clock period	t_p	37.0		166.7	ns
INCK low level width	t_{wl}	0.4tp		0.6tp	ns
INCK high level width	t_{wh}	0.4tp		0.6tp	ns
INCK jitter	Tjitter			600	ps

8-2-1-2 INCK Sine Waveform Input Specifications

IMX576-AAKH5-C does not support the “AC coupled connection”.

8-2-2 PLL block characteristics

Electrical characteristics of PLL block is shown below.

Table 13 PLL block characteristics (VT system)

Conditions : V_{ANA} = 2.8V, V_{DIG} = 1.05 V, Tj = 25 ˚C.

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6		27	MHz	
Input frequency range of phase comparator	6		12	MHz	
VCO frequency range	1050		2100	MHz	
Output frequency range	1050		2100	MHz	
Settling time			1000	µs	

Table 14 PLL block characteristics (OP system)

Conditions : V_{ANA} = 2.8V, V_{DIG} = 1.05 V, T_j = 25 ˚C

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6		27	MHz	
Input frequency range of phase comparator	6		12	MHz	
VCO frequency range	1250		2300	MHz	
Output frequency range	1250		2300	MHz	
Settling time			1000	μs	

8-2-3 Definition of settling time of PLL block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

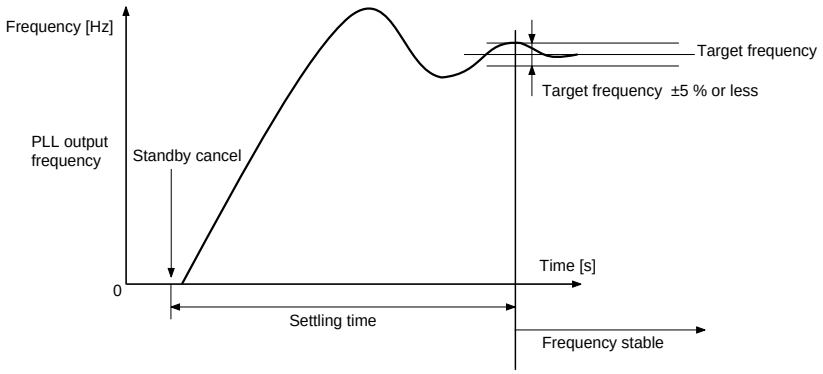


Figure 21 Definition of settling time

8-2-4 2-wire serial communication block characteristics

2-wire serial communication characteristics are shown below.

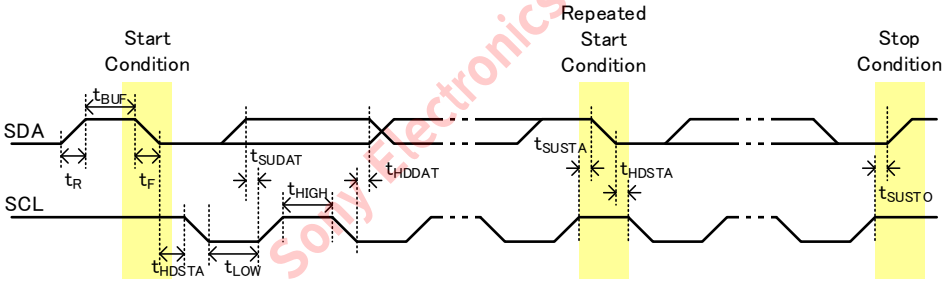


Figure 22 2-wire serial communication block specification

Table 15 2-wire serial communication block specification

Parameter	Symbol	Conditions	Min.	Max. (Fast-mode Plus)	Unit
Low level input voltage	V_{IL}		-0.5	$0.3V_{IF}$	V
High level input voltage	V_{IH}		$0.7V_{IF}$	2.9	V
Low level output voltage	V_{OL1}	V_{IF} > 2 V, Sink 3 mA	0	0.4	V
	V_{OL2}	V_{IF} < 2 V, Sink 3 mA	0	$0.2V_{IF}$	V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 V_{IF}→0.3 V_{IF}		250 (120)	ns
Input current	I_I	0.1 V_{IF}→0.9 V_{IF}	-10	10	μA
SDA I/O capacitance	$C_{I/O}$			10	pF
SCL Input capacitance	C_I			10	pF

Table 16 2-wire serial communication block AC specification

Fast-mode

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Rise time (SDA and SCL)	t_R	-	300	ns
Fall time (SDA and SCL)	t_F	-	300	ns
Hold time (start condition)	t_{HDSTA}	0.6	-	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.6	-	µs
Setup time (stop condition)	t_{SUSTO}	0.6	-	µs
Data setup time	t_{SUDAT}	100	-	ns
Data hold time	t_{HDDAT}	0	0.9	µs
Bus free time between Stop and Start condition	t_{BUF}	1.3		µs
Low period of the SCL clock	t_{LOW}	1.3		µs
High period of the SCL clock	t_{HIGH}	0.6		µs

Fast-mode Plus*

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	1000	kHz
Rise time (SDA and SCL)	t_R	-	120	ns
Fall time (SDA and SCL)	t_F	-	120	ns
Hold time (start condition)	t_{HDSTA}	0.26	-	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.26	-	µs
Setup time (stop condition)	t_{SUSTO}	0.26	-	µs
Data setup time	t_{SUDAT}	50	-	ns
Data hold time	t_{HDDAT}	0	-	µs
Bus free time between Stop and Start condition	t_{BUF}	0.5		µs
Low period of the SCL clock	t_{LOW}	0.5		µs
High period of the SCL clock	t_{HIGH}	0.26		µs

Note : Fast-mode Plus supports only available with INCK ≥ 14.5MHz; See module design reference manual for detail.

8-2-5 Current consumption and standby current

Table 17 Current consumption and standby current

(INCK = 18MHz, V_{ANA} = 2.8V, V_{DIG} = 1.05 V, V_{IF} = 1.8 V, T_j = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (analog)	I_{ANA}		62.8	65.5	mA	Normal Full @30 frame/s, MIPI = 2.1Gbps/lane, QBC Re-mosaic : ON, DPC(Static, Dynamic) : ON
Current consumption (digital)	I_{DIG}		257.8	356.0	mA	
Current consumption (IF)	I_{IF}		2.2	2.7	mA	
Standby current (analog)	I_{STBANA}			2	µA	XCLR : Low fixed INCK : stop SLASEL : NC or Low fixed XVS : NC or High fixed SWDIO : NC or High fixed GYINT : Low fixed TEST1/S_SCSB : Low fixed TEST2/S_SCK : Low fixed TEST3/S_SDI : Low fixed
Standby current (digital)	I_{STBDIG}			158	µA	
Standby current (IF)	I_{STBIF}			1	µA	

8-2-6 Gyro Control Interface

Gyro Control Interface supports Serial Peripheral Interface (SPI).
Gyro Control Interface characteristics are shown below.

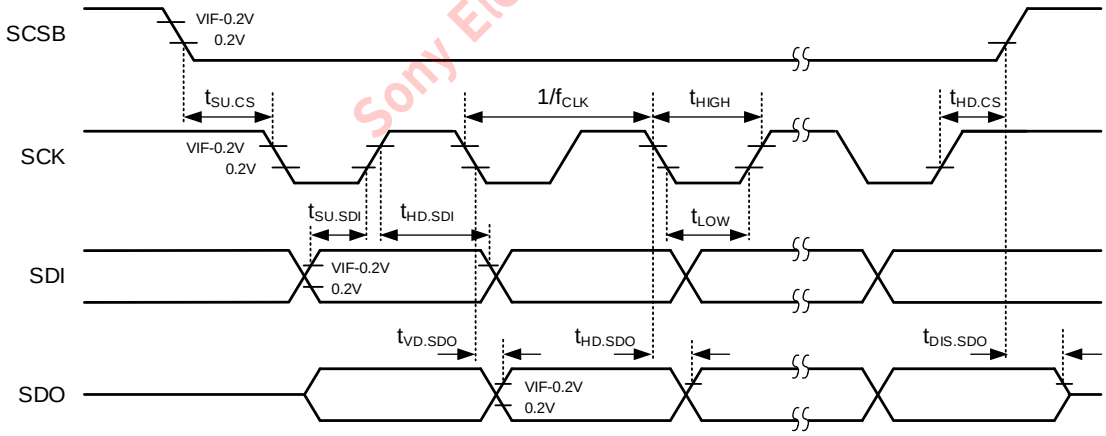


Figure 23 2-wire serial communication block specification

Table 18 2-wire serial communication block AC specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK Clock Frequency	f_{CLK}	-	-	1	MHz	
SCLK Low Period	t_{LOW}	500	-	-	ns	
SCLK High Period	t_{HIGH}	500	-	-	ns	
CS Setup Time	t_{SU_CS}	500	-	-	ns	
CS Hold Time	t_{HD_CS}	500	-	-	ns	
SDI Setup Time	t_{SU_SDI}	11	-	-	ns	
SDI Hold Time	t_{HD_SDI}	7	-	-	ns	
SDO Valid Time	t_{VD_SDO}	-	-	100	ns	
SDO Hold Time	t_{HD_SDO}	4	-	-	ns	
SDO Output Disable Time	t_{DIS_SDO}	-	-	50	ns	
CS high time between transactions	t_{BUF}	-	940	-	µs	

9. Spectral Sensitivity Characteristic

(Includes neither lens characteristics nor light source characteristics.)

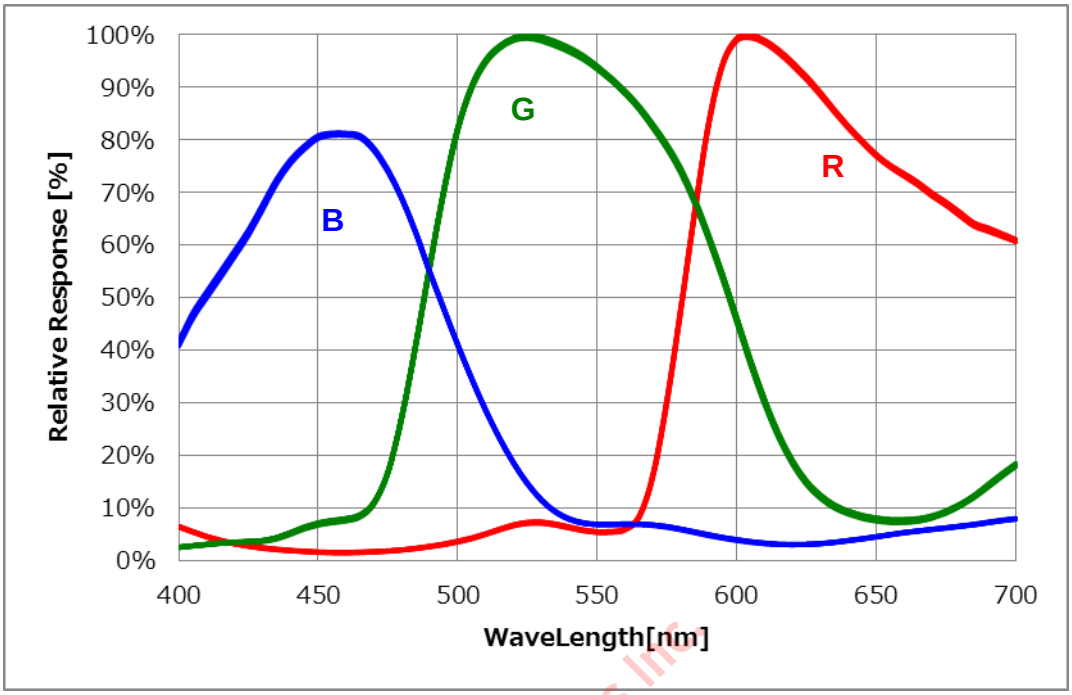


Figure 24 Spectral sensitivity characteristics

10. Image Sensor Characteristics

10-1 Image Sensor Characteristics

Table 19 Image Sensor Characteristics

(Full size@30 frame/s, V_{ANA} = 2.8V, V_{DIG} = 1.05 V, V_{IF} = 1.8 V, T_j = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Range	Measurement method	Remarks
Sensitivity	S	133			LSB	Center	1(*1)	
Sensitivity ratio	RG	0.48	0.54	0.60		Center	2(*1)	
	BG	0.33	0.39	0.45				
Saturation signal	Vsat	1023			LSB	Zone1	3(*1)	Include OB level (*2)
Video signal shading	SH			88	%	Zone2D	4(*1)	Design assurance
Dark signal	Vdt			0.5	LSB	Zone2D	5(*1)	When operation at 15 frame/s

The data described at this image sensor characteristics are the measurement standard without base gain setting, and indicates the results evaluated with OB as a reference.

Note 1) These refer to the descriptions of the Measurement Methods on “11-4 Measurement method”.

Note 2) LSB is the abbreviation of Least Significant Bit. 10 bits = 1023 digital is the maximum output code for the output unit. The gain setting (base gain setting) in which the saturation signal output matches with 1023 LSB requires 0[dB] when the OB level is 64 LSB (standard recommended value).

10-2 Zone Definition used for specifying image sensor characteristics

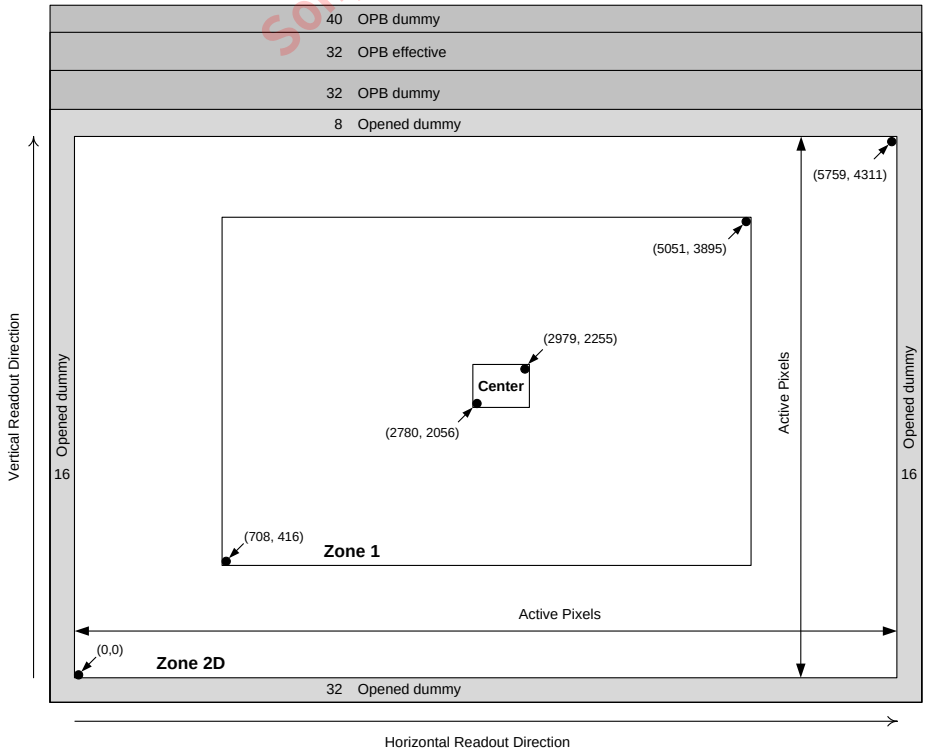


Figure 25 Zone Definition Diagram

11. Measurement Method for Image Sensor Characteristics

11-1 Measurement conditions

The device operation conditions are at the typical values of the bias and clock voltage.

Table 20 Measurement Conditions

Supply voltage	VANA 2.8V, VDIG 1.05V, VIF 1.8V
Clock	INCK 18 MHz

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr, Gb, R and B digital signal outputs of the measurement system.

11-2 Pixel position of This Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.

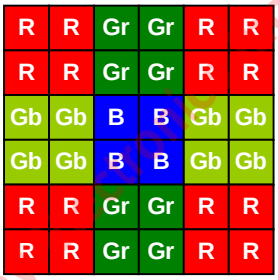


Figure 26 Coding alignment

11-3 Definition of Standard Imaging Conditions

11-3-1 Standard imaging condition I

Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

11-3-2 Standard imaging condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.

11-4 Measurement method

11-4-1 Sensitivity

Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/300 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of imaging area, and substitute the values into the following formula.

S = {((VGr + VGb) /2) × (300/120)} [LSB]

11-4-2 Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting so that the average value of the Gr and Gb signal output is 341 [LSB], measure the R signal output (VR [LSB]), the Gr and Gb signal outputs (VGr, VGb [LSB]) and the B signal output (VB [LSB]) at the imaging area Center in frame readout mode, and substitute the values into the following formulas.

VG = (VGr + VGb) /2

RG = VR/VG

RB = VB/VG

11-4-3 Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous Intensity to 20 times the intensity with the average value of the Gr, Gb signal outputs, 341 [LSB], measure the average value of the Gr, Gb, R and B signal outputs.

11-4-4 Video signal shading

Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 341 [LSB]. Then measure the maximum value (Gmax [LSB]) and minimum value (Gmin [LSB]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

SH = ((Gmax –Gmin) /Gmax) × 100 [%]

11-4-5 Dark signal

Measure the output difference between 1/15 [s] signal output (Va) and 1/15000 or less [s] signal output (Vb) at the device ambient temperature of 60 ˚C and the device in the light-obstructed state, and calculate the signal output at 1/15 [s] storage by them using the following approximate formula. Then,this is Vdt [LSB].

Vdt = (Va – Vb) × (1/15) / (1/15) – (1/15000) ≈ (Va –Vb) [LSB]

12. Spot Pixel Specification

Table 21 Spot Pixel Specifications

(Full size@30 frame/s, V_{ANA} = 2.8V, V_{DIG} = 1.05 V, V_{IF} = 1.8 V, T_j = 60 ˚C)

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone		Measurement method	Remarks
		Zone2D	Other		
Black or white pixels at high light	30 % ≤ D	122	No evaluation criteria applied	12-3-1	
White pixels in the dark	28 (LSB) ≤ D	1865	No evaluation criteria applied	12-3-2	1/30 storage Note 2)

Note) 1. D...Spot pixel level.
2. Continuous same color pixels in the horizontal or vertical direction are NG.
3. Defect pixels are measured with all optional image processing features (DPC, LSC, QBC Re-mosaic) disabled.
4. The maximum quantity pixel counts of 122 for Bright Pixels and 1865 for Dark Pixels are total of R + Gr + Gb + B individual pixels from any color channels.
5. The analog gain for both the Illuminated and Dark defect conditions is 0dB.
6. The above chart (hereinafter referred to as the “Spot Pixel Specifications”) is the standard only for sorting image sensor products in this specification book (hereinafter referred to as the “PRODUCTS”) before shipment from a manufacturing factory. Sony Semiconductor Solutions Corporation and its distributors (collectively hereinafter referred to as the “Seller”) disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the Spot Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the “Program”), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.

12-1 Notice on White Pixels Specifications

After shipment inspection of CMOS image sensors, pixels of CMOS image sensors may be distorted and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels.")
Particle radiation such as cosmic rays etc. is one of the causes of White Pixels.
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such distorted pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against White Pixels, such as adoption of automatic compensation systems for White Pixels and establishment of quality assurance standards.
White Pixels may be also caused by alpha radiation, which will be emitted in a process of decay of radioactive isotopes which inevitably exist in the air in minute amounts and may exist in materials or parts of CMOS image sensor devices (e.g. packaging materials, seal glass, wiring materials and IC chips). It is recommended that you should use materials or parts which do not include radioactive isotopes, which are sources of alpha radiation, and consider taking measures, such as adoption of vacuum packaging technologies in order to ensure that the PRODUCTS are not exposed to the air. As the density of radioactive isotopes in the air of the underground space may become thicker than that on the ground, it is highly recommended to ensure the PRODUCTS are not exposed to the air in using or storing the PRODUCTS at the underground space.

[For Your Reference]

The Annual number of White Pixels Occurrence Caused by Particle Radiation such as cosmic rays etc.

The data in the below chart shows the estimated annual number of White Pixels occurrence caused by particle radiation such as cosmic rays etc. in a single-story building in Tokyo at an altitude of 0 meters. The data shows estimated number of White Pixels based on records of past field tests calculated taking structures and electrical properties of each device into account. However, the data in the chart is for your reference purpose only, and shall not be construed as part of any CMOS image sensor product specifications which the Seller warrants.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
14.1 LSB or higher	1.5 pcs
25.1 LSB or higher	1.0 pcs
60.3 LSB or higher	0.5 pcs
125.6 LSB or higher	0.3 pcs
180.9 LSB or higher	0.3 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the annual number of White Pixels occurrence.

Material_No.06-0.0.9

12-2 Measurement Method for Spot Pixels

Measure under the standard imaging condition II.

12-3 Spot Pixel Pattern Specifications

12-3-1 Black or white pixels at high light

After adjusting the average value of the Gr/Gb signal output to 341 LSB, measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the Gr/Gb/R/B signal output Vx (x = Gr/Gb/R/B), and substitute the values into the following formula.
The 341 LSB does not include the dark level offset of 64. The average value is calculated using the signal level output of Zone 2D.

$$D_K(\text{White Pixel level}) = (V_{XK} / \overline{V_X}) \times 100\ [\%]$$

$$D_B(\text{Black Pixel level}) = (V_{XB} / \overline{V_X}) \times 100\ [\%]$$

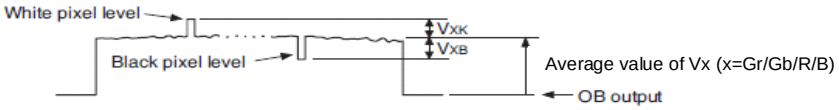


Figure 27 Measurement Method for Spot Pixels

12-3-2 White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

13. CRA Characteristics of Recommended Lens

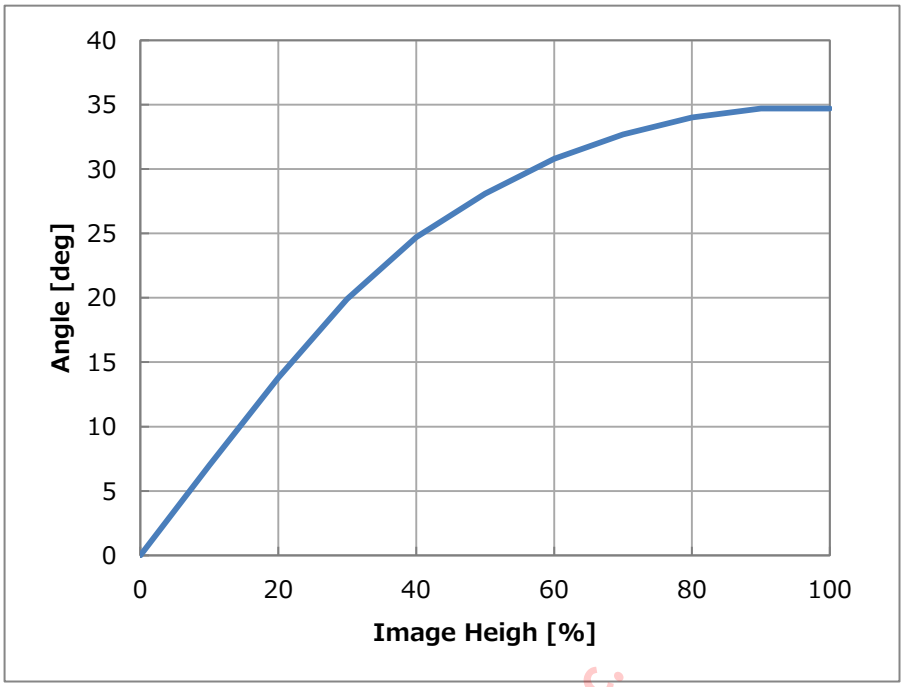


Figure 28 CRA characteristics

14. Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

(1) Perform all work in a clean environment.
(2) Do not touch the chip surface with hand and make any object contact with it.
(3) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

3. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Reliability assurance of this product should be ignored because it is a bare chip.
(5) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(6) Note that X-ray inspection may damage characteristics of the sensor.
(7) Note that the sensor may be damaged when using ultraviolet ray and infrared ray on mounting it.
(8) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

15. Notes on Handling (Additional items concerning bare chip mounting of stacked-type CMOS image sensors)

Collet contact is allowed in areas other than the pixel area, bonding pads, scribe area, and chip edge. Contact with areas other than the contact-allowed area may result in problems such as dust emission or electrostatic breakdown.

Collet contact-prohibited areas

- Pixel area: Abnormal images
- Bonding pad: Circuit electrostatic breakdown
  (Please note that this rule is not applicable for electrostatic breakdown prevention areas.)
- Scribe area: Dust emission due to chipping
- Chip edge: Dust emission due to chip breakage

Note: Ensure sufficient positional accuracy during the pickup work.
Separate the collet contact surfaces and contact-prohibited areas as much as possible.

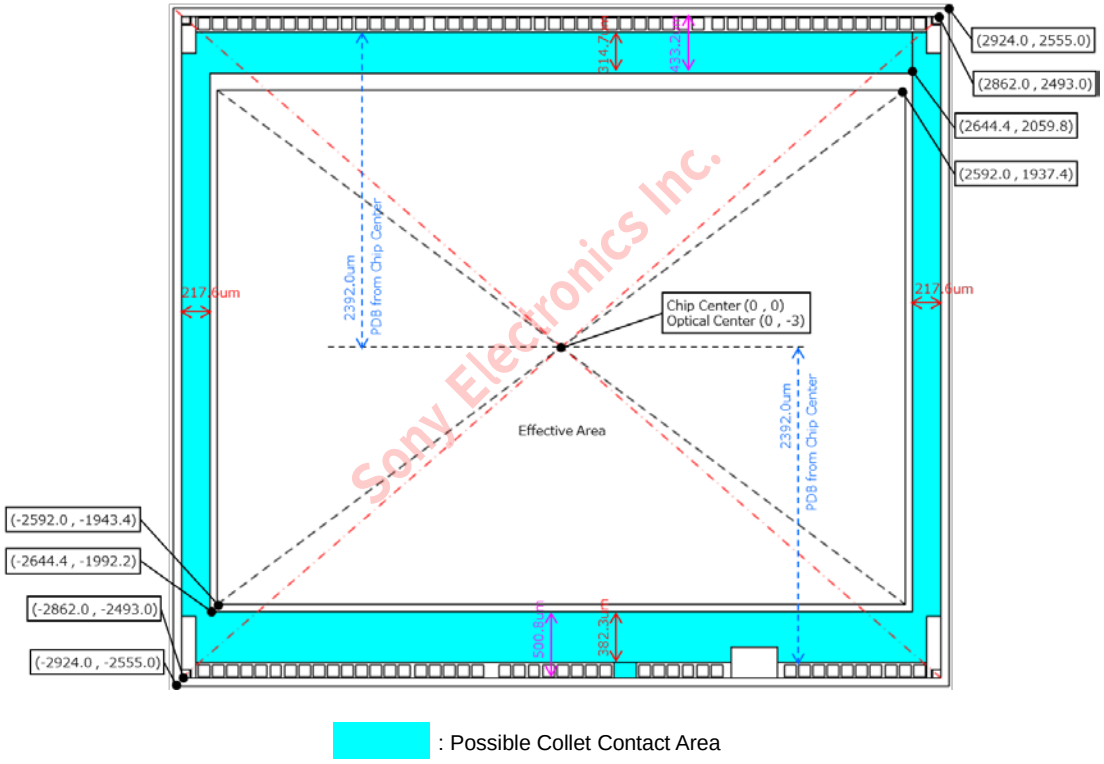


Figure 29 Prohibited Area

Ultrasonic chip cleaning is prohibited.
This may result in dust emission from cut surfaces.

Material_No.20-0.0.3

16. Open Source Software License

```
/* ----------------------------------------------------------------------
* Copyright (C) 2010-2013 ARM Limited. All rights reserved.
*
* $Date:            17. January 2013
* $Revision:        V1.4.1
*
* Project:          CMSIS DSP Library
* Title:            arm_common_tables.h
*
* Description:    This file has extern declaration for common tables like Bitreverse, reciprocal etc which are used
across different functions
*
* Target Processor: Cortex-M4/Cortex-M3
*
* Redistribution and use in source and binary forms, with or without
* modification, are permitted provided that the following conditions
* are met:
*     - Redistributions of source code must retain the above copyright
*       notice, this list of conditions and the following disclaimer.
*     - Redistributions in binary form must reproduce the above copyright
*       notice, this list of conditions and the following disclaimer in
*       the documentation and/or other materials provided with the
*       distribution.
*     - Neither the name of ARM LIMITED nor the names of its contributors
*       may be used to endorse or promote products derived from this
*       software without specific prior written permission.
*
* THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS
* "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT
* LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS
* FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE
* COPYRIGHT OWNER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT,
* INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING,
* BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES;
* LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER
* CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT
* LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN
* ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE
* POSSIBILITY OF SUCH DAMAGE.
* -------------------------------------------------------------------- */

/* ----------------------------------------------------------------------
* Copyright (C) 2010-2013 ARM Limited. All rights reserved.
*
* $Date:            17. January 2013
* $Revision:        V1.4.1
*
* Project:          CMSIS DSP Library
* Title:            arm_const_structs.h
*
* Description:    This file has constant structs that are initialized for
*                   user convenience.    For example, some can be given as
*                   arguments to the arm_cfft_f32() function.
*
* Target Processor: Cortex-M4/Cortex-M3
*
```

```
* Redistribution and use in source and binary forms, with or without
* modification, are permitted provided that the following conditions
* are met:
*   - Redistributions of source code must retain the above copyright
*     notice, this list of conditions and the following disclaimer.
*   - Redistributions in binary form must reproduce the above copyright
*     notice, this list of conditions and the following disclaimer in
*     the documentation and/or other materials provided with the
*     distribution.
*   - Neither the name of ARM LIMITED nor the names of its contributors
*     may be used to endorse or promote products derived from this
*     software without specific prior written permission.
*
* THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS
* "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT
* LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS
* FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE
* COPYRIGHT OWNER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT,
* INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING,
* BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES;
* LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER
* CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT
* LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN
* ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE
* POSSIBILITY OF SUCH DAMAGE.
* ---------------------------------------------------------------------- */

/* ----------------------------------------------------------------------
* Copyright (C) 2010-2013 ARM Limited. All rights reserved.
*
* $Date:            17. January 2013
* $Revision:        V1.4.1
*
* Project:          CMSIS DSP Library
* Title:            arm_math.h
*
* Description:    Public header file for CMSIS DSP Library
*
* Target Processor: Cortex-M4/Cortex-M3/Cortex-M0
*
* Redistribution and use in source and binary forms, with or without
* modification, are permitted provided that the following conditions
* are met:
*   - Redistributions of source code must retain the above copyright
*     notice, this list of conditions and the following disclaimer.
*   - Redistributions in binary form must reproduce the above copyright
*     notice, this list of conditions and the following disclaimer in
*     the documentation and/or other materials provided with the
*     distribution.
*   - Neither the name of ARM LIMITED nor the names of its contributors
*     may be used to endorse or promote products derived from this
*     software without specific prior written permission.
*
* THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS
* "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT
* LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS
* FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE
* COPYRIGHT OWNER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT,
* INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING,
* BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES;
* LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER
```

```
* CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT
* LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN
* ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE
* POSSIBILITY OF SUCH DAMAGE.
  * ---------------------------------------------------------------------- */


/******************************************************************************//**
  * @file        core_cm0.h
  * @brief       CMSIS Cortex-M0 Core Peripheral Access Layer Header File
  * @version     V3.20
  * @date        25. February 2013
  *
  * @note
  *
  ******************************************************************************/
/* Copyright (c) 2009 - 2013 ARM LIMITED

    All rights reserved.
    Redistribution and use in source and binary forms, with or without
    modification, are permitted provided that the following conditions are met:
    - Redistributions of source code must retain the above copyright
      notice, this list of conditions and the following disclaimer.
    - Redistributions in binary form must reproduce the above copyright
      notice, this list of conditions and the following disclaimer in the
      documentation and/or other materials provided with the distribution.
    - Neither the name of ARM nor the names of its contributors may be used
      to endorse or promote products derived from this software without
      specific prior written permission.
    *
    THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS"
    AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE
    IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE
    ARE DISCLAIMED. IN NO EVENT SHALL COPYRIGHT HOLDERS AND CONTRIBUTORS BE
    LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR
    CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF
    SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS
    INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN
    CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE)
    ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE
    POSSIBILITY OF SUCH DAMAGE.
    ---------------------------------------------------------------------------*/

/******************************************************************************//**
  * @file        core_cm0plus.h
  * @brief       CMSIS Cortex-M0+ Core Peripheral Access Layer Header File
  * @version     V3.20
  * @date        25. February 2013
  *
  * @note
  *
  ******************************************************************************/
/* Copyright (c) 2009 - 2013 ARM LIMITED

    All rights reserved.
    Redistribution and use in source and binary forms, with or without
    modification, are permitted provided that the following conditions are met:
    - Redistributions of source code must retain the above copyright
      notice, this list of conditions and the following disclaimer.
    - Redistributions in binary form must reproduce the above copyright
      notice, this list of conditions and the following disclaimer in the
```

```
   documentation and/or other materials provided with the distribution.
 - Neither the name of ARM nor the names of its contributors may be used
   to endorse or promote products derived from this software without
   specific prior written permission.
 *
 THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS"
 AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE
 IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE
 ARE DISCLAIMED. IN NO EVENT SHALL COPYRIGHT HOLDERS AND CONTRIBUTORS BE
 LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR
 CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF
 SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS
 INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN
 CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE)
 ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE
 POSSIBILITY OF SUCH DAMAGE.
 ---------------------------------------------------------------------------*/

/******************************************************************************//**
 * @file     core_cmFunc.h
 * @brief    CMSIS Cortex-M Core Function Access Header File
 * @version  V3.20
 * @date     25. February 2013
 *
 * @note
 *
 ******************************************************************************/
/* Copyright (c) 2009 - 2013 ARM LIMITED

   All rights reserved.
   Redistribution and use in source and binary forms, with or without
   modification, are permitted provided that the following conditions are met:
   - Redistributions of source code must retain the above copyright
     notice, this list of conditions and the following disclaimer.
   - Redistributions in binary form must reproduce the above copyright
     notice, this list of conditions and the following disclaimer in the
     documentation and/or other materials provided with the distribution.
   - Neither the name of ARM nor the names of its contributors may be used
     to endorse or promote products derived from this software without
     specific prior written permission.
   *
   THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS"
   AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE
   IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE
   ARE DISCLAIMED. IN NO EVENT SHALL COPYRIGHT HOLDERS AND CONTRIBUTORS BE
   LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR
   CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF
   SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS
   INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN
   CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE)
   ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE
   POSSIBILITY OF SUCH DAMAGE.
   ---------------------------------------------------------------------------*/

/******************************************************************************//**
 * @file     core_cmInstr.h
 * @brief    CMSIS Cortex-M Core Instruction Access Header File
 * @version  V3.20
 * @date     05. March 2013
 *
 * @note
```

```
 *
 ******************************************************************************/
/* Copyright (c) 2009 - 2013 ARM LIMITED

    All rights reserved.
    Redistribution and use in source and binary forms, with or without
    modification, are permitted provided that the following conditions are met:
    - Redistributions of source code must retain the above copyright
      notice, this list of conditions and the following disclaimer.
    - Redistributions in binary form must reproduce the above copyright
      notice, this list of conditions and the following disclaimer in the
      documentation and/or other materials provided with the distribution.
    - Neither the name of ARM nor the names of its contributors may be used
      to endorse or promote products derived from this software without
      specific prior written permission.
    *
    THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS"
    AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE
    IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE
    ARE DISCLAIMED. IN NO EVENT SHALL COPYRIGHT HOLDERS AND CONTRIBUTORS BE
    LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR
    CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF
    SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS
    INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN
    CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE)
    ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE
    POSSIBILITY OF SUCH DAMAGE.
    ---------------------------------------------------------------------------*/

 * @version    V3.10
 * @date       19. August, 2014
 *
 * @note
 *
 ******************************************************************************/
/* Copyright (c) 2012 ARM LIMITED

    All rights reserved.
    Redistribution and use in source and binary forms, with or without
    modification, are permitted provided that the following conditions are met:
    - Redistributions of source code must retain the above copyright
      notice, this list of conditions and the following disclaimer.
    - Redistributions in binary form must reproduce the above copyright
      notice, this list of conditions and the following disclaimer in the
      documentation and/or other materials provided with the distribution.
    - Neither the name of ARM nor the names of its contributors may be used
      to endorse or promote products derived from this software without
      specific prior written permission.
    *
    THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS"
    AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE
    IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE
    ARE DISCLAIMED. IN NO EVENT SHALL COPYRIGHT HOLDERS AND CONTRIBUTORS BE
    LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR
    CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF
    SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS
    INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN
    CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE)
    ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE
    POSSIBILITY OF SUCH DAMAGE.
    ---------------------------------------------------------------------------*/
```