

Model Number	Fab	CPU				GPU			Memory Technology			Nav	Wii Cellular
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)		
K3V2 (Hi3620)	40 nm	ARMv7	Cortex-A9 L1: 32 KB instruction + 32 KB data, L2: 1 MB	4	1.4	Vivante GC4000	240	15.3	LPDDR2	64-bit (2x32-bit Dual-channel)	8.5 (533 MHz)	—	—

K3V2E

This is a revised version of K3V2 SoC with improved support of Intel baseband. The SoC supports LPDDR2-1066, but actual products are found with LPDDR-900 instead for lower power consumption.

Model Number	Fab	CPU				GPU			Memory Technology			Nav	Wii Cellular
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)		
K3V2E (Hi3620)	40 nm	ARMv7	Cortex-A9 L1: 32 KB instruction + 32 KB data, L2: 1 MB	4	1.5	Vivante GC4000	240	15.3	LPDDR2	64-bit (2x32-bit Dual-channel)	8.5 (533 MHz)	—	—

Kirin 620

• supports – USB 2.0 / 13 MP / 1080p video encode

Model Number	Fab	CPU				GPU			Memory Technology			Nav	Wii Cellular
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)		
Kirin 620 (Hi6220) ^[17]	28 nm	ARMv8-A	Cortex-A53	g ^[18]	1.2	Mali-450 MP4	500	32	LPDDR3	32-bit (1x32-bit Single-channel)	6.4 (800 MHz)	—	Dual SIM LTE Cat.4 (150 Mbit/s)

Kirin 650, 655, 658, 659

Model number	Fab	CPU				GPU			Memory technology			Nav	Wireless	
		ISA	μarch	Cores	Freq (GHz)	μarch	Freq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)		Cellular	WLAN
Kirin 650 (Hi6250)	16 nm FinFET+	ARM v8-A	Cortex-A53 Cortex-A53	4+4	2.0 (4x A53) 1.7 (4x A53)	Mali-T830 MP2	900	57.6	LPDDR3	64-bit (2x32-bit Dual-channel) ^[19]	14.9 (933 MHz)	A-GPS, Glonass	Dual SIM LTE Cat.6 (300 Mbit/s)	WIFI 4 (802.11n)
Kirin 655					2.12 (4x A53) 1.7 (4x A53)									
Kirin 658					2.35 (4x A53) 1.7 (4x A53)									

Kirin 710

Model Number	Fab	CPU				GPU			Memory Technology			Nav	Cellular
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)		
Kirin 710 (Hi6260)	TSMC 12 nm FinFET	ARMv8-A	Cortex-A73 Cortex-A53	4+4	2.2 (A73) 1.7 (A53)	Mali-G51 MP4	1000	64	LPDDR3 LPDDR4	32-bit	A-GPS, GLONASS	DL SIM LTE Cat.6 (64 MB)	
Kirin 710F ^[20]													
Kirin 710A	SMIC 14 nm FinFET ^[21]				2.0 (A73) 1.7 (A53)								

Kirin 810 and 820

- DaVinci NPU based on Tensor Arithmetic Unit
- Kirin 820 supported 5G NSA & SA

Model number	Fab	CPU				GPU			Memory technology			Nav	Wi	
		ISA	μarch	Cores	Freq (GHz)	μarch	Freq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Band width (GB/s)		Cellular	Wi
Kirin 810 (Hi6280)	7 nm FinFET	ARM v8.2-A	Cortex-A76 Cortex-A55 (big.LITTLE)	2+6	2.27 (2x A76) 1.90 (6x A55)	Mali-G52 MP6	820	157.4	LPDDR4X	64-bit (4x16-bit Quad-channel)	34.1 (2133 MHz)	A-GPS, Glonass, BDS	Dual SIM LTE Cat.12 (600 Mbit/s)	Wi (802.11)
Kirin 820 5G (Hi6290L V100)				(1+3)+4	2.36 (1x A76 H) 2.22 (3x A76 L) 1.84 (4x A55)	Mali-G57 MP6							Balong 5000 (Sub-6 GHz Only; NSA & SA)	
Kirin 820E 5G				3+3	2.22 (3x A76 L) 1.84 (3x A55)	Mali-G57 MP6							Balong 5000 (Sub-6 GHz Only; NSA & SA)	

Kirin 910 and 910T

Model Number	Fab	CPU				GPU			Memory Technology			Nav	Wi	
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)		Cellular	Wi
Kirin 910 (Hi6620)	28 nm HPM	ARMv7	Cortex-A9	4	1.6	Mali-450 MP4	533	32	LPDDR3	32-bit (1x32-bit Single-channel)	6.4 (800 MHz)	—	LTE Cat.4	—
Kirin 910T					1.8		700	41.8						

Kirin 920, 925 and 928

- The Kirin 920 SoC also contains an image processor that supports up to 32-megapixel

Model Number	Fab	CPU				GPU			Memory Technology			Nav	Cellular		
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)				
Kirin 920	28 nm HPM	ARMv7	Cortex-A15 Cortex-A7 big.LITTLE	4+4	1.7 (A15) 1.3 (A7)	Mali-T628 MP4	600	76.8	LPDDR3	64-bit (2x32-bit Dual-channel)	12.8 (800 MHz)	—	LTE Cat.6 (300 Mbit/s)		
Kirin 925 (Hi3630)					1.8 (A15) 1.3 (A7)							—		—	—
Kirin 928					2.0 (A15) 1.3 (A7)							—		—	—

Kirin 930 and 935

• supports – SD 3.0 (UHS-I) / eMMC 4.51 / Dual-band a/b/g/n Wi-Fi / Bluetooth 4.0 Low Energy / USB 2.0 / 32 MP ISP / 1080p video encode

Model Number	Fab	CPU				GPU			Memory Technology			Nav	Cellular
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)		
Kirin 930 (Hi3635)	28 nm HPC	ARMv8-A	Cortex-A53 Cortex-A53	4+4	2.0 (A53) 1.5 (A53)	Mali-T628 MP4	600	76.8	LPDDR3	64-bit (2x32-bit Dual-channel)	12.8 (800 MHz)	—	Dual SIM LTE Cat.6 (DL:300 Mbit/s UP:50 Mbit/s)
Kirin 935					2.2 (A53) 1.5 (A53)							680	

Kirin 950 and 955

• supports – SD 4.1 (UHS-II) / UFS 2.0 / eMMC 5.1 / MU-MIMO 802.11ac Wi-Fi / Bluetooth 4.2 Smart / USB 3.0 / NFS / Dual ISP (42 MP) / Native 10-bit 4K video encode / i5 coprocessor / Tensilica HiFi 4 DSP

Model Number	Fab	CPU				GPU			Memory Technology			Nav	Cellular
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)		
Kirin 950 (Hi3650)	TSMC 16 nm FinFET+ ^[26]	ARMv8-A	Cortex-A72 Cortex-A53 big.LITTLE	4+4	2.3 (A72) 1.8 (A53)	Mali-T880 MP4	900	151.2	LPDDR4	64-bit (2x32-bit Dual-channel)	25.6 (1600 MHz)	—	D S L C
Kirin 955 ^[28]					2.5 (A72) 1.8 (A53)							LPDDR3 (3 GB) LPDDR4 (4 GB)	

Kirin 960

- Interconnect: ARM CCI-550, Storage: UFS 2.1, eMMC 5.1, Sensor Hub: i6

Model Number	Fab	CPU				GPU			Memory Technology			Nav	Ce
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)		
Kirin 960 (Hi3660) ^[29]	TSMC 16 nm FFC	ARMv8-A	Cortex-A73 Cortex-A53 big.LITTLE	4+4	2.36 (A73) 1.84 (A53)	Mali-G71 MP8	1037	199.1	LPDDR4	64-bit (2x32-bit Dual-channel)	25.6 (1600 MHz)	—	Du Sil LT Ce LT C/ MI

Kirin 970

- Interconnect: ARM CCI-550, Storage: UFS 2.1, Sensor Hub: i7
- Cadence Tensilica Vision P6 DSP.^[30]
- NPU made in collaboration with Cambricon Technologies. 1.92T FP16 OPS.^[31]

Model Number	Fab	CPU				GPU			Memory Technology			Nav
		ISA	Microarchitecture	Cores	Frq (GHz)	Microarchitecture	Frq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Bandwidth (GB/s)	
Kirin 970 (Hi3670)	TSMC 10 nm FinFET+	ARMv8-A	Cortex-A73 Cortex-A53 big.LITTLE	4+4	2.36 (A73) 1.84 (A53)	Mali-G72 MP12	746	214.8	LPDDR4X	64-bit (4x16-bit Quad-channel)	29.8 (1866 MHz)	Galileo

Kirin 980 and Kirin 985 5G/4G

Kirin 980 is HiSilicon's first SoC based on 7 nm FinFET technology.

- Interconnect: ARM Mali G76-MP10, Storage: UFS 2.1, Sensor Hub: i8
- Dual NPU made in collaboration with Cambricon Technologies.

Kirin 985 5G is the second HiSilicon's 5G SoC based on 7 nm FinFET Technology.

- Interconnect: ARM Mali-G77 MP8, Storage UFS 3.0
- Big-Tiny Da Vinci NPU: 1x Da Vinci Lite + 1x Da Vinci Tiny

Model number	Fab	CPU				GPU			Memory technology			Nav	W Cellular
		ISA	μarch	Cores	Freq (GHz)	μarch	Freq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Band width (GB/s)		
Kirin 980	TSMC 7 nm FinFET	ARM v8.2- A	Cortex-A76 Cortex-A55 (big.LITTLE)	(2+2)+4	2.6 (A76 H) 1.92 (A76 L) 1.8 (A55)	Mali-G76 MP10 ^[32]	720	345.6	LPDDR4X	64-bit (4x16-bit Quad-channel)	34.1 (2133 MHz)	Galileo	Dual SIM LTE Cat.21 LTE 5x CA, No 4x4 MIMO
Kirin 985 5G/4G (Hi6290V110)				(1+3)+4	2.58 (A76 H) 2.40 (A76 L) 1.84 (A55)	Mali-G77 MP8	700	358.4					Balong 5000 (Sub- 6 GHz only; NSA & SA), 4G version available

Kirin 990 4G, Kirin 990 5G and Kirin 990E 5G

Kirin 990 5G is HiSilicon's first 5G SoC based on N7 nm+ FinFET technology.^[33]

- Interconnect
 - Kirin 990 4G: ARM Mali-G76 MP16
 - Kirin 990 5G: ARM Mali-G76 MP16
 - Kirin 990E 5G: ARM Mali-G76 MP14
- Da Vinci NPU.
 - Kirin 990 4G: 1x Da Vinci Lite + 1x Da Vinci Tiny
 - Kirin 990 5G: 2x Da Vinci Lite + 1x Da Vinci Tiny
 - Kirin 990E 5G: 1x Da Vinci Lite + 1x Da Vinci Tiny
- Da Vinci Lite features 3D Cube Tensor Computing Engine (2048 FP16 MACs + 4096 INT8 MACs), Vector unit (1024bit INT8/FP16/FP32)
- Da Vinci Tiny features 3D Cube Tensor Computing Engine (256 FP16 MACs + 512 INT8 MACs), Vector unit (256bit INT8/FP16/FP32)^[34]

Model number	Fab	CPU				GPU			Memory technology			Nav	Wireless	
		ISA	μarch	Cores	Freq (GHz)	μarch	Freq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Band width (GB/s)		Cellular	WLAN
Kirin 990 4G	TSMC 7 nm FinFET (DUV)				2.86 (A76 H) 2.09 (A76 L) 1.86 (A55)								Balong 765 (LTE Cat.19)	—
Kirin 990 5G	TSMC 7 nm+ FinFET (EUV)	ARM v8.2-A	Cortex-A76 Cortex-A55 (big.LITTLE)	(2+2)+4	2.86 (A76 H) 2.36 (A76 L) 1.95 (A55)	Mali-G76 MP16	600	460.8	LPDDR4X	64-bit (4x16-bit Quad-channel)	34.1 (2133 MHz)	Beidou, Galileo, Glonass	Balong 5000 (Sub-6-GHz only; NSA & SA)	—
Kirin 990E 5G						Mali-G76 MP14	600	403.2						—

Kirin 8000

HiSilicon Kirin 8000 is a mid-range Kirin 8 series chip not officially announced, however, it was released along with the announcement of Huawei nova 12.^[35]

Model number	Fab	CPU				GPU			Memory technology			Nav	Cellular
		ISA	µarch	Cores	Freq (GHz)	µarch	Freq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Band width (GB/s)		
Kirin 8000 (Hi6290V110)	SMIC N+2 7 nm FinFET	ARM v8.2-A	Cortex-A77 Cortex-A55 (big.LITTLE)	1+3+4	2.40 (1x A77 H) 2.19 (3x A77 L) 1.84 (4x A55)	Mali-G610 MP4	864	442.4	LPDDR4X LPDDR5	64-bit (4x16-bit Quad-channel)	34.1 (2133 MHz) 51.2 (3200 MHz)	GPS, A-GPS, Glonass, BeiDou, Galileo, QZSS	Balong modem
Kirin T80 (Hi6290V110)													
Kirin 8020													
Kirin T82													
Kirin 8020			HiSilicon Taishan		2.22 (1x Taishan Big) 2.05 (3x Taishan Mid) 1.31 (4x Taishan Small)	Maleoon 920C	840	860.2	LPDDR5X		68.2 (4266 MHz)		

Kirin 9000 5G/4G and Kirin 9000E, Kirin 9000L

Kirin 9000 is HiSilicon's first SoC based on 5 nm+ FinFET (EUV) TSMC technology (N5 node) and the first 5 nm SoC to be launched on the international market.^[36] This octa-core system on a chip is based on the 9th Gen of the HiSilicon Kirin series and is equipped with 15.3 billion transistors in a 1+3+4 core configuration: 4 Arm Cortex-A77 CPU (1x 3.13 GHz and 3x 2.54 GHz), 4 Arm Cortex-A55 (4x 2.05 GHz) and a 24-core Mali-G78 GPU (22-core in the Kirin 9000E version) The Kirin 9000L uses a 1+2+3 core configuration: 3 Arm Cortex-A77 (1x 3.13 GHz and 2x 2.54 GHz), 3 Arm Cortex-A55 (3x 2.05 GHz) and a 22-core Mali-G78 GPU with Kirin Gaming+ 3.0 implementation.^[36]

The integrated quad pipeline NPU (Dual Big Core + 1 Tiny Core configuration) is equipped with the Kirin ISP 6.0 to support advanced computational photography. The Huawei Da Vinci Architecture 2.0 for AI supports 2x Ascend Lite + 1x Ascend Tiny (only 1 Lite in 9000E/L). The system cache is 8 MB and the SoC works with the new LPDDR5/4X memories (made by Samsung in the Huawei Mate 40 series). Due to the integrated 3rd generation 5G proprietary modem "Balong 5000", Kirin 9000 supports 2G, 3G, 4G and 5G SA & NSA Sub-6 GHz connectivity.^[36] The SoC's TDP is 6W.

The 2021 4G version of the Kirin 9000 has the Balong modem limited via software to comply with the ban imposed on Huawei by the US government for non-chinese 5G technologies. The Kirin 9006C is a rebranded variant of the Kirin 9000E for the Huawei Qingyun L420 and L540 laptops.^{[37][38]}

GPU

- Kirin 9000L: ARM Mali-G78 MP22
- Kirin 9000E: ARM Mali-G78 MP22
- Kirin 9000: ARM Mali-G78 MP24
- Da Vinci NPU architecture 2.0
 - Kirin 9000L: 1x Big Core + 1x Tiny Core
 - Kirin 9000E: 1x Big Core + 1x Tiny Core
 - Kirin 9000: 2x Big Cores + 1x Tiny Core

Model number	Fab	CPU				GPU			Memory technology			Nav	Wire		
		ISA	μarch	Cores	Freq (GHz)	μarch	Freq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)	Band width (GB/s)		Cellular	V	
Kirin 9000L	TSMC 5 nm+ FinFET (EUV)	ARM v8.2-A	Cortex-A77 Cortex-A55 (big.LITTLE)	(1+2)+3	3.13 (A77 H) 2.54 (A77 L) 2.05 (A55)	Mali-G78 MP22	759	LPDDR4X LPDDR5	64-bit (4x16-bit) Quad-channel	34.1 (2133 MHz) 44 (2750 MHz)	Beidou, Galileo, Glonass	Balong 5000 (Sub-6-GHz only; NSA & SA)	V		
Kirin 9000E												1068.7			
Kirin 9000 (Hi36A0V101)				(1+3)+4		Mali-G78 MP24						1165.8			

Kirin 9000S, Kirin 90x0 series

The Kirin 9000S, Kirin 9000S1, and Kirin 9010 of the Kirin 9000 Hi36A0 family were the first HiSilicon-developed SoCs manufactured in high volumes in mainland China in 2023 by SMIC. The SoC had its debut with the Huawei Mate 60 in late 2023 with the Kirin 9000S alongside overlocked enhancements of the Kirin 9000S1 and Kirin 9010 with the Huawei Pura 70 series in early 2024.^[39] According to Tom's Hardware, the Taishan V120 core, developed by HiSilicon, was roughly on par with AMD's Zen 3 cores from late 2020.^[40] Four of these cores were used in the 9000 series alongside four efficiency-focused Arm Cortex-A510 cores.^[41] The SoCs are based on SMIC's 7nm technology node, referred to as "N+2". It also includes 1 Da Vinci "big" NPU core and 1 Da Vinci "small" NPU core. Kirin 9000W, a Wi-Fi only SoC for the Huawei MatePad Pro 13.2 Wi-Fi only model, debuted in global markets in Q1 2024. The Kirin 9010 and Kirin 9000S1 debuted in Q2 2024, using a modified 2+6+4 core configuration with a new large Taishan core with the same configurations of medium and small cores from the Kirin 9000S with faster enhancements over the Kirin 9000S.^[42]

Model number	Fab	CPU				GPU			Memory technology			N	
		ISA	µarch	Cores (total)	Threads (total)	Freq (GHz)	µarch	Freq (MHz)	Performance (GFLOPS)	Type	Bus width (bit)		Band width (GB/s)
Kirin 9000S (Hi36A0V120)	SMIC 7 nm FinFET [43][44]	ARMv8.x	HiSilicon Taishan, Cortex- A510	1+3+4 (8)	2+6+4 (12)	2.62 GHz (TaishanV120) 2.15 GHz (TaishanV120) 1.53 GHz (Cortex-A510)	HiSilicon Maleoon 910	750	1536	LPDDR5	64-bit (4x16-bit Quad-channel)	44 (2750 MHz)	Beid Galile GLO
Kirin 9000S1 (Hi36A0V120)													
Kirin 9000W (Hi36A0V120)													
Kirin 9000WL (Hi36A0V120)													
Kirin 9000WE (Hi36A0V120)													
Kirin T90 (Hi36A0V120)													
Kirin T90A (Hi36A0V120)													
Kirin 9000SL (Hi36A0V120)													
Kirin 9000WM (Hi36A0V120)													
Kirin 9010 (Hi36A0V121)													
Kirin 9010E (Hi36A0V121)													
Kirin 9010A (Hi36A0V121)													
Kirin 9010W (Hi36A0V121)													
Kirin T91 (Hi36A0V121)													

Kirin 9010L (Hi36A0V121)			1+2+3 (6)	2+4+3 (9)	2.19 GHz (TaishanV121) 2.18 GHz (TaishanV120) 1.40 GHz (Cortex-A510)					
Kirin 9020 (Hi36C0V110) ^[45]			1+3+4 (8)	2+6+4 (12)	2.50 GHz (TaishanV123) 2.15 GHz (TaishanV120) 1.60 GHz (Taishan- Little)	HiSilicon Maleoon 920	840	1720		68.2 (4266 MHz)
Kirin T92 (Hi36C0V110)										
Kirin 9030			1+3+4 (8)	2+6+4 (12)	2.69 GHz (Taishan V124 Big) 2.27 GHz (Taishan V124 Mid) 1.72 GHz (Taishan V124 Little)	HiSilicon Maleoon 935A		2388		
Kirin 9030 Pro	SMIC 5 nm FinFET	HiSilicon Taishan	1+4+4 (9)	2+8+4 (14)	2.75 GHz (Taishan V124 Big) 2.27 GHz (Taishan V124 Mid) 1.72 GHz (Taishan V124 Little)	HiSilicon Maleoon 935	933	2866	LPDDR5X	76.8 (4800 MHz)
Kirin 9030S			1+3+4 (8)	2+6+4 (12)	2.7 GHz (Taishan V124 Big) 2.15 GHz (Taishan V124 Mid) 1.62 GHz (Taishan V124 Little)	HiSilicon Maleoon 935F		1433	32-bit (2x16- bit Dual- channel)	34.1 (4266 MHz)

Smartphone modems

HiSilicon develops smartphone modems which are primarily used in its parent company [Huawei](#)'s handheld and tablet devices.

Balong 700

The Balong 700 supports LTE TDD/FDD.^[46] Its specs:

- 3GPP R8 protocol
- LTE TDD and FDD
- 4x2/2x2 SU-MIMO

Balong 710

At MWC 2012, HiSilicon released the Balong 710.^[47] It is a multi-mode chipset supporting 3GPP Release 9 and LTE Category 4 at GTI (Global TD-LTE Initiative). The Balong 710 was designed to be used with the K3V2 SoC. Its specs:

- LTE FDD mode : 150 Mbit/s downlink and 50 Mbit/s uplink.
- TD-LTE mode: up to 112 Mbit/s downlink and up to 30 Mbit/s uplink.
- WCDMA Dual Carrier with MIMO: 84 Mbit/s downlink and 23 Mbit/s uplink.

Balong 720

The Balong 720 supports LTE Cat6 with 300 Mbit/s peak download rate.^[46] Its specs:

- TSMC 28 nm HPM process
- TD-LTE Cat.6 standard
- Dual-carrier aggregation for the 40 MHz bandwidth
- 5-mode LTE Cat6 Modem

Balong 750

The Balong 750 supports LTE Cat 12/13, and it is first to support 4CC CA and 3.5 GHz.^[46] Its specs:

- LTE Cat.12 and Cat.13 UL network standards
- 2CC (dual-carrier) data aggregation
- 4x4 multiple-input multiple-output (MIMO)
- TSMC 16 nm FinFET+ process

Balong 765

The Balong 765 supports 8×8 MIMO technology, LTE Cat.19 with downlink data-rate up to 1.6 Gbit/s in FDD network and up to 1.16 Gbit/s in the TD-LTE network.^[48] Its specs:

- 3GPP Rel.14
- LTE Cat.19 Peak data rate up to 1.6 Gbit/s
- 4CC CA + 4×4 MIMO/2CC CA + 8×8 MIMO
- DL 256QAM
- C-V2X

Balong 5G01

The Balong 5G01 supports the 3GPP standard for 5G with downlink speeds of up to 2.3 Gbit/s. It supports 5G across all frequency bands including sub-6 GHz and millimeter wave (mmWave).^[46] Its specs:

- 3GPP Release 15
- Peak data rate up to 2.3 Gbit/s
- Sub-6 GHz and mmWave
- NSA/SA
- DL 256QAM

Balong 5000

The Balong 5000 was the world's first 7 nm TSMC 5G multi-mode chipset (launched in Q1 2019), the world's first SA/NSA implementation, and the first smartphone chipset to support the full NR TDD/FDD spectrum.^[49] The modem has an advanced 2G, 3G, 4G, and 5G connectivity.^[50] Its specs:

- 2G/3G/4G/5G Multi Mode
- Fully compliant with 3GPP Release 15
- Sub-6 GHz: 100 MHz x 2CC CA
- Sub-6 GHz: Downlink up to 4.6 Gbit/s, Uplink up to 2.5 Gbit/s
- mmWave: Downlink up to 6.5 Gbit/s, Uplink up to 3.5 Gbit/s
- NR+LTE: Downlink up to 7.5 Gbit/s
- FDD & TDD Spectrum Access
- SA & NSA Fusion Network Architecture
- Supports 3GPP R14 V2X
- 3 GB LPDDR4X RAM^[51]

Balong 6000

The Balong 6000 is an iteration of the HiSilicon Balong 5G baseband series and first appeared in the Huawei Mate 70 Pro, launched on November 26, 2024.

It is one of the first 3GPP Rel. 18 and therefore 5.5G/5G-Advanced supporting modem in the world alongside the Qualcomm Snapdragon X75/X80 and onwards series.^[52]

- 2G/3G/4G/5G Multi Mode
- Fully compliant with 3GPP Release 17, probably compliant with 3GPP Release 18^[53]
- Sub-6 GHz: 100 MHz x 4CC CA
- Sub-6 GHz: Downlink up to 4.6 Gbit/s, Uplink up to 2.5 Gbit/s
- mmWave: Downlink up to 12 Gbit/s, Uplink up to 3.5 Gbit/s
- NR+LTE: Downlink up to 10 Gbit/s
- FDD & TDD Spectrum Access
- SA & NSA Fusion Network Architecture

Wearable SoCs

HiSilicon develops SoCs for wearables such as wireless earbuds, wireless headphones, neckband earbuds, smart speakers, smart eyewear, and smartwatches.^[54]

Kirin A1

The Kirin A1 (Hi1132) was announced on 6 September 2019 built for TWS devices.^[54] It features:

- BT/BLE dual-mode Bluetooth 5.1^[55]
- Isochronous Dual Channel transmission technology
- 356 MHz audio processor
- Cortex-M7 microprocessor

Kirin A2

The Kirin A2 was announced on September 25, 2023.^[56] It features:

- Faster Transmission
- Stable signal with Polar code technology
- Increase of 50% in computing power performance
- Audio Vivid
- Ascend Nano NPU
- NearLink compatible

Kirin W80

The Kirin W80 was announced on May 15, 2025 built for Watches.^[57] It features:

- arm64-v8a design
- NearLink compatible
- Ascend Nano NPU
- XTAP health sensor support
- 1.7GHz Quad-core processor
- 492MHz GPU

Server processors

HiSilicon develops server processor SoCs based on the ARM architecture.

Hi1610

The Hi1610 is HiSilicon's first generation server processor announced in 2015. It features:

- 16x ARM Cortex-A57 at up to 2.1 GHz^[58]
- 48 KB L1-I, 32 KB L1-D, 1 MB L2/4 cores and 16 MB CCN L3
- TSMC 16 nm
- 2x DDR4-1866
- 16 PCIe 3.0

Hi1612

The Hi1612 is HiSilicon's second generation server processor launched in 2016. It is the first chiplet-based Kunpeng with two computing dies. It features:

- 32x ARM Cortex-A57 at up to 2.1 GHz^[58]
- 48 KB L1-I, 32 KB L1-D, 1 MB L2/4 cores and 32 MB CCN L3
- TSMC 16 nm
- 4x DDR4-2133
- 16 PCIe 3.0

Kunpeng 916 (formerly Hi1616)

The Kunpeng 916 (formerly known as Hi1616) is HiSilicon's third generation server processor launched in 2017. The Kunpeng 916 is used in Huawei's TaiShan 2280 Balanced Server, TaiShan 5280 Storage Server, TaiShan XR320 High-Density Server Node and TaiShan X6000 High-Density Server.^{[59][60][61][62]} It features:

- 32x ARM Cortex-A72 at up to 2.4 GHz^[58]
- 48 KB L1-I, 32 KB L1-D, 1 MB L2/4 cores and 32 MB CCN L3
- TSMC 16 nm
- 4x DDR4-2400
- 2-way Symmetric multiprocessing (SMP), Each socket has 2x ports with 96 Gbit/s per port (total of 192 Gbit/s per each socket interconnects)
- 46 PCIe 3.0 and 8x 10 Gigabit Ethernet
- 85 W

Kunpeng 920 (formerly Hi1620)

The Kunpeng 920 (formerly known as Hi1620) is HiSilicon's fourth generation server processor announced in 2018, and launched in 2019. Huawei claims the Kunpeng 920 CPU scores more than an estimated 930 on SPECint_rate_base2006.^[63] The Kunpeng 920 is used in Huawei's TaiShan 2280 V2 Balanced Server, TaiShan 5280 V2 Storage Server, and TaiShan XA320 V2 High-Density Server Node.^{[64][65][66]} It features:

- 32 to 64x custom TaiShan V110 cores at up to 2.6 GHz.^[67]
- The TaiShan V110 core is a 4-way superscalar, out-of-order microarchitecture that implements the ARMv8.2-A ISA. Huawei reports the core supports almost all the ARMv8.4-A ISA features with a few exceptions, including the dot product and FP16 FML extensions.^[67]
- The TaiShan V110 cores are likely a new core not based on ARM designs^[68]
- 3x Simple ALUs, 1x Complex MDU, 2x BRUs (sharing ports with ALU2/3), 2x FSUs (ASIMD FPU), 2x LSUs^[68]
- 64 KB L1-I, 64 KB L1-D, 512 KB Private L2 and 1 MB L3/core Shared.
- TSMC 7 nm HPC
- 8x DDR4-3200
- 2-way and 4-way symmetric multiprocessing (SMP). Each socket has 3x Hydra ports with 240 Gbit/s per port (total of 720 Gbit/s per each socket interconnects)
- 40 PCIe 4.0 with CCIX support, 4x USB 3.0, 2x SATA 3.0, 8x SAS 3.0 and 2x 100 Gigabit Ethernet
- 100 to 200 W
- Compression engine (GZIP, LZS, LZ4) capable of up to 40 Gbit/s compress and 100 Gbit/s decompress
- Crypto offload engine (for AES, DES, 3DES, SHA1/2, etc..) capable of throughputs up to 100 Gbit/s

Kunpeng 920B (formerly Hi1630V100)

The Kunpeng 920B (formerly known as Hi1630V100) is HiSilicon's fifth-generation server processor announced in 2019 and scheduled for launch in 2021. It features:

- 80 custom TaishanV120 cores at 2.9 GHz frequency, with support for simultaneous multithreading (SMT) and ARM's Scalable Vector Extension (SVE).^[67]
- 64 KB L1-I, 64 KB L1-D, 512 KB Private L2 and 1 MB L3/core Shared
- TSMC 5 nm
- 8x DDR5

Kunpeng 950

The Kunpeng 950 is HiSilicon's sixth-generation server processor announced in 2019 and scheduled for launch in 2023.

AI acceleration

HiSilicon also develops AI Acceleration chips.

Da Vinci architecture

Each Da Vinci Max AI Core features a 3D Cube Tensor Computing Engine (4096 FP16 MACs + 8192 INT8 MACs), a vector unit (2048bit INT8/FP16/FP32), and a scalar unit. It includes a new AI framework called "MindSpore", a platform-as-a-service product called ModelArts, and a lower-level library called Compute Architecture for Neural Networks (CANN).^[34]

Ascend 310

The Ascend 310 is an AI inference SoC, it was codenamed Ascend-Mini. The Ascend 310 is capable of 16 TOPS@INT8 and 8 TOPS@FP16.^[69] The Ascend 310 features:

- 2x Da Vinci Max AI cores^[34]
- 8x ARM Cortex-A55 CPU cores
- 8 MB on-chip buffer
- 16 channel video decode – H.264/H.265
- 1 channel video encode – H.264/H.265
- TSMC 12 nm FFC process
- 8W TDP

Ascend 910

The Ascend 910 is an AI training SoC, it was codenamed Ascend-Max. which delivers 256 TFLOPS@FP16 and 512 TOPS@INT8. The Ascend 910 features:

- 32x Da Vinci Max AI cores arranged in 4 clusters^[34]
- 1024-bit NoC Mesh @ 2 GHz, with 128 GB/s bandwidth Read/Write per core
- 3x 240 Gbit/s HCCS ports for Numa connections
- 2x 100 Gbit/s RoCE interfaces for networking
- 4x HBM2E, 1.2 TB/s bandwidth
- 3D-SRAM stacked below AI SoC die
- 1228 mm² Total die size (456 mm² Virtuvian AI SoC, 168 mm² Nimbus V3 IO Die, 4x96 mm² HBM2E, 2x110 mm² Dummy Die)

- 32 MB on-chip buffer
- 128 channel video decode – H.264/H.265
- TSMC 7 nm EUV (N7+) process
- 350 W

Ascend 910B

Ascend 910B is manufactured by SMIC and is very different from Ascend 910.^[70]

- 21.32 mm × 31.22 mm size
- 25 DaVinci AI cores
- produced using SMIC 7nm N+1 process

Ascend 910C

Huawei Ascend 910C is expected to be mass shipped in May 2025, Ascend 910C combines two Ascend 910B processors. Ascend 910C is an evolution rather than a breakthrough, it achieves performance similar to [NVIDIA H100](#). NVIDIA H100 chips were banned from sale to China by US government in 2022.^[71]

DeepSeek researchers say Huawei Ascend 910C provides 60% of [NVIDIA H100](#) inference performance. Ascend 910C compute chiplet is made by [SMIC](#) at 2nd generation 7nm process known as N+2.^[72]

[DeepSeek R1](#) model was trained on NVIDIA H800, but runs inference on Ascend 910C.^[73]

Huawei is expected to sell more than 800,000 of Ascend 910B and Ascend 910C in 2025.^[74]

In late April 2025 Huawei started delivering to customers CloudMatrix 384 - a cluster consisting of Ascend 910C chips. The system performs better than NVL72 (72 [GB200](#) chips) from NVIDIA, however the power consumption is significantly higher. CloudMatrix 384 sells for Rmb60mn (\$8.2mn) a set.^[75] CloudMatrix 384 solution provides 2.3x lower performance per watt than Nvidia's GB200 NVL72. The systems consists of 16 racks including 12 computing racks and 4 networking ones facilitating high-bandwidth using 6912 800G LPO optical transceivers. CloudMatrix uses entirely optical connections for intra- and inter-rack connectivity.^[76]

Ascend 910D

In late April 2025 [WSJ](#) has reported that Huawei approached several China based companies about testing Ascend 910D, the companies will receive first samples in May 2025.^[74]

Ascend 920

Ascend 920 was announced in April 2025 and expected to provide performance similar to NVIDIA H20 chip (which was banned in April 2025 from selling to China). Ascend 920 is expected to be mass produced in late 2025. Ascend 920 features:^[77]

- 6nm SMIC process
- HBM3 memory, 4 TB/s bandwidth
- 900 TFLOPs per card

Semiconductor equipment export control by US

The US government started to pressure [ASML Holding](#) not to sell new [EUV](#) machines to China in 2018.^[78]

In 2022, the US government was lobbying the Dutch government to bar ASML from selling older DUV (deep ultraviolet lithography) machines to China. These DUV machines are a generation behind of newer [EUV](#) models.^[79]

[Lam Research](#) and [Applied Materials](#) have suspended sales and services to Chinese counterparts in 2022.^[80]

In late 2024, the US government expanded export control which will hit semiconductor toolmakers such as [KLA Corporation](#), [Lam Research](#) and [Applied Materials](#).^[81]

China based [SiCarrier](#) is developing equipment to replace products from [ASML Holding](#), [Lam Research](#) and [Applied Materials](#).^[82]

In late May 2025, the US administration has told to [Cadence Design Systems](#), [Synopsys](#) and [Siemens EDA](#) to stop supplying their products to China. The restrictions have encouraged the local [EDA](#) companies such as [Empyrean Technology](#), [Primarius](#) and [Semitronix](#) to significantly grow market share.^[83]

In September 2025, the SMIC (the largest foundry in China) has started testing the first domestically produced DUV lithography equipment (DUV is the previous generation before [EUV](#)). This set of tools was developed by Shanghai Yuliangsheng Technology Co.. The machine is designed for 28nm fabrication, although it can be used for 7nm and 5nm fabrication using multipatterning techniques. It is expected that the mass production of DUV machines will begin in 2027.^[84]

See also



- [Semiconductor industry](#)

- Semiconductor industry in China

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