

Tegra

Tegra is a system on a chip (SoC) series developed by Nvidia for mobile devices such as smartphones, personal digital assistants, and mobile Internet devices. The Tegra integrates an ARM architecture central processing unit (CPU), graphics processing unit (GPU), northbridge, southbridge, and memory controller onto one package. Early Tegra SoCs are designed as efficient multimedia processors. The Tegra-line evolved to emphasize performance for gaming and machine learning applications without sacrificing power efficiency, before taking a drastic shift in direction towards platforms that provide vehicular automation with the applied *Nvidia Drive* brand name on reference boards and its semiconductors; and with the *Nvidia Jetson* brand name for boards adequate for AI applications (e.g. within robots or drones) and for various smart high-level automation purposes.

History

The Tegra APX 2500 was announced on February 12, 2008. The Tegra 6xx product line was revealed on June 2, 2008,^[1] and the APX 2600 was announced in February 2009. The APX chips were designed for smartphones, while the Tegra 600 and 650 chips were intended for smartbooks and mobile Internet devices (MID).^[2]

The first product to use the Tegra was Microsoft's Zune HD media player in September 2009, followed by the Samsung M1.^[3] Microsoft's Kin was the first cellular phone to use the Tegra;^[4] however, the phone did not have an app store, so the Tegra's power did not provide much advantage. In September 2008, Nvidia and Opera Software announced that they would produce a version of the Opera 9.5 browser optimized for the Tegra on Windows Mobile and Windows CE.^{[5][6]} At Mobile World Congress 2009, Nvidia introduced its port of Google's Android to the Tegra.

On January 7, 2010, Nvidia officially announced and demonstrated its next generation Tegra system-on-a-chip, the Nvidia Tegra 250, at Consumer Electronics Show 2010.^[7] Nvidia primarily supports Android on Tegra 2, but booting other ARM-supporting operating systems is possible on devices where the bootloader is accessible. Tegra 2 support for the Ubuntu Linux distribution was also announced on the Nvidia developer forum.^[8]

Nvidia announced the first quad-core SoC at the February 2011 Mobile World Congress event in Barcelona. Though the chip was codenamed Kal-El, it is now branded as Tegra 3. Early benchmark results show impressive gains over Tegra 2,^{[9][10]} and the chip was used in many of the tablets released in the second half of 2011.

In January 2012, Nvidia announced that Audi had selected the Tegra 3 processor for its In-Vehicle Infotainment systems and digital instruments display.^[11] The processor will be integrated into Audi's entire line of vehicles worldwide, beginning in 2013. The process is ISO 26262-certified.^[12]

In summer of 2012 Tesla Motors began shipping the Model S electric sedan, which contains two NVIDIA Tegra 3D Visual Computing Modules (VCM). One VCM powers the 17-inch touchscreen infotainment system, and one drives the 12.3-inch all digital instrument cluster.^[13]

In March 2015, Nvidia announced the Tegra X1, the first SoC to have a graphics performance of 1 teraflop. At the announcement event, Nvidia showed off Epic Games' Unreal Engine 4 "Elemental" demo, running on a Tegra X1.

On October 20, 2016, Nvidia announced that the Nintendo Switch hybrid video game console will be powered by Tegra hardware.^[14] On March 15, 2017, TechInsights revealed the Nintendo Switch is powered by a custom Tegra X1 (model T210), with lower clockspeeds.^[15]

Models

Tegra APX

Tegra APX 2500

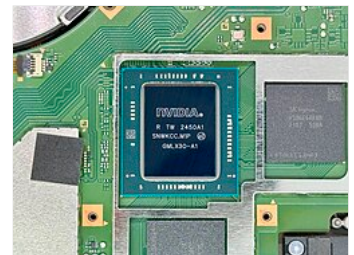
- Processor: ARM11 600 MHz MPCore (originally GeForce ULV)
 - Suffix: APX (formerly CSX)
- Memory: NOR or NAND flash, Mobile DDR
- Graphics: Image processor (FWVGA 854×480 pixels)
 - Up to 12 megapixels camera support
 - LCD controller supports resolutions up to 1280×1024
- Storage: IDE for SSD
- Video codecs: up to 720p MPEG-4 AVC/H.264 and VC-1 decoding
- Includes GeForce ULV support for OpenGL ES 2.0, Direct3D Mobile, and programmable shaders
- Output: HDMI, VGA, composite video, S-Video, stereo jack, USB
- USB On-The-Go



Nvidia Tegra T20 (Tegra 2) and T30 (Tegra 3) chips



A Tegra X1 inside a Shield TV



A Tegra T239 inside a Nintendo Switch 2

Tegra APX 2600

- Enhanced NAND flash
- Video codecs:^[16]
 - 720p H.264 Baseline Profile encode or decode
 - 720p VC-1/WMV9 Advanced Profile decode
 - D-1 MPEG-4 Simple Profile encode or decode

Tegra 6xx

Tegra 600

- Targeted for GPS segment and automotive
- Processor: ARM11 700 MHz MPCore
- Memory: low-power DDR (DDR-333, 166 MHz)
- SXGA, HDMI, USB, stereo jack
- HD camera 720p

Tegra 650

- Targeted for GTX of handheld and notebook
- Processor: ARM11 800 MHz MPCore
- Low power DDR (DDR-400, 200 MHz)
- Less than 1 watt envelope
- HD image processing for advanced digital still camera and HD camcorder functions
- Display supports 1080p at 24 frame/s, HDMI v1.3, WSXGA+ LCD and CRT, and NTSC/PAL TV output
- Direct support for Wi-Fi, disk drives, keyboard, mouse, and other peripherals
- A complete board support package (BSP) to enable fast time to market for Windows Mobile-based designs

Tegra 2

The second generation Tegra SoC has a dual-core ARM Cortex-A9 CPU, an ultra low power (ULP) GeForce GPU,^[17] a 32-bit memory controller with either LPDDR2-600 or DDR2-667 memory, a 32 KB/32 KB L1 cache per core and a shared 1 MB L2 cache.^[18] Tegra 2's Cortex A9 implementation does not include ARM's SIMD extension, NEON. There is a version of the Tegra 2 SoC supporting 3D displays; this SoC uses a higher clocked CPU and GPU.

The Tegra 2 video decoder is largely unchanged from the original Tegra and has limited support for HD formats.^[19] The lack of support for high-profile H.264 is particularly troublesome when using online video streaming services.

Common features:

- CPU cache: L1: 32 KB instruction + 32 KB data, L2: 1 MB
- 40 nm semiconductor technology



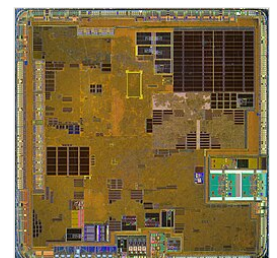
Nvidia Tegra 2 T20

Model number	CPU			GPU			Memory				Adoption
	Processor	Cores	Frequency	Micro-architecture	Core config ¹	Frequency	Type	Amount	Bus width	Band-width	Availability
AP20H (Ventana/Unknown)	Cortex-A9	2	1.0 GHz	VLIW-based VEC4 units ^[20]	4:4:4:4 ^[21]	300 MHz	LPDDR2 300 MHz DDR2 333 MHz	?	32 bit single-channel	2.4 GB/s 2.7 GB/s	Q1 2010
T20 (Harmony/Ventana)						333 MHz					
AP25			400 MHz			Q1 2011					
T25			1.2 GHz								

¹ Pixel shaders : Vertex shaders : Texture mapping units : Render output units

Devices

Model	Devices
AP20H	Motorola Atrix 4G, Motorola Droid X2, Motorola Photon, LG Optimus 2X / LG Optimus Dual P990 / Optimus 2x SU660 (?), Samsung Galaxy R, Samsung Captivate Glide, T-Mobile G2X P999, Acer Iconia Tab A200 and A500, LG Optimus Pad, Motorola Xoom, ^[22] Sony Tablet S, Dell Streak Pro, ^[23] Toshiba Thrive ^[24] tablet, T-Mobile G-Slate
AP215	Fusion Garage Grid 10
T20	Avionic Design Tamonten Processor Board, ^[25] Notion Ink Adam tablet, Olivetti OliPad 100, ViewSonic G Tablet, ASUS Eee Pad Transformer, Samsung Galaxy Tab 10.1, Toshiba AC100, CompuLab Trim-Slice nettop, Velocity Micro Cruz Tablet L510, Acer Iconia Tab A100
Unknown	Tesla Motors Model S 2012–2017 and Model X 2015–2017 instrument cluster (IC) ^{[26][27]}



Nvidia Tegra 2 T20 die shot

Tegra 3

NVIDIA's Tegra 3 (codenamed "Kal-El")^[28] is functionally a SoC with a quad-core ARM Cortex-A9 MPCore CPU, but includes a fifth "companion" core in what Nvidia refers to as a "variable SMP architecture".^[29] While all cores are Cortex-A9s, the companion core is manufactured with a low-power silicon process. This core operates transparently to applications and is used to reduce power consumption when processing load is minimal. The main quad-core portion of the CPU powers off in these situations.

Tegra 3 is the first Tegra release to support ARM's SIMD extension, NEON.

The GPU in Tegra 3 is an evolution of the Tegra 2 GPU, with 4 additional pixel shader units and higher clock frequency. It can also output video up to 2560×1600 resolution and supports 1080p MPEG-4 AVC/h.264 40 Mbit/s High-Profile, VC1-AP, and simpler forms of MPEG-4 such as DivX and Xvid.^[30]



Nvidia Tegra 3 T30L

The Tegra 3 was released on November 9, 2011.^[31]

Common features:

- CPU cache: L1: 32 KB instruction + 32 KB data, L2: 1 MB
- 40 nm LPG semiconductor technology by TSMC

Model number	CPU			GPU			Memory				Adoption
	Processor	Cores	Frequency (multi-/single-core mode)	Micro-architecture	Core config ¹	Frequency	Type	Amount	Bus width	Bandwidth	Availability
T30L	Cortex-A9	4+1	1.2 GHz / up to 1.3 GHz	VLIW-based VEC4 units ^[20]	8:4:8:8 ^[32]	416 MHz	DDR3-1333	?	32 bit single-channel	5.3 GB/s ^[33]	Q1 2012
T30			1.4 GHz / up to 1.5 GHz			520 MHz	LPDDR2-1066	?		4.3 GB/s	Q4 2011
AP33			1.5 GHz				DDR3-L-1500	?		6.0 GB/s ^[34]	
T33			1.6 GHz / up to 1.7 GHz ^[33]			DDR3-1600	?	6.4 GB/s ^[33]		Q2 2012	

¹ Pixel shaders : Vertex shaders : Texture mapping units : Render output units

Devices

Model	Devices
AP33	LG Optimus 4X HD, HTC One X, XOLO Play T1000, ^[35] Coolpad 8735
T30	Asus Eee Pad Transformer Prime (TF201), ^[36] IdeaTab K2 / LePad K2, ^[37] Acer Iconia Tab A510, Fuhu Inc. nabi 2 Tablet, ^[38] Microsoft Surface RT, ^[39] Lenovo IdeaPad Yoga 11, ^{[40][41]}
T30I	Tesla Model S 2012–2017 and Model X 2015–2017 media control unit (MCU) ^{[27][42]}
T30L	Asus Transformer Pad TF300T, Microsoft Surface, Nexus 7 (2012), ^[43] Sony Xperia Tablet S, Acer Iconia Tab A210, Toshiba AT300 (Excite 10), ^[44] BLU Quattro 4.5, ^[45] Coolpad 9070
T33	Asus Transformer Pad Infinity (TF700T), Fujitsu ARROWS X F-02E, HTC One X+, Ouya (T33-P-A3)



The Ouya uses a Tegra 3 T33-P-A3.

Tegra 4

The Tegra 4 (codenamed "Wayne") was announced on January 6, 2013, and is a SoC with a quad-core CPU, but includes a fifth low-power Cortex A15 companion core which is invisible to the OS and performs background tasks to save power. This power-saving configuration is referred to as "variable SMP architecture" and operates like the similar configuration in Tegra 3.^[46]

The GeForce GPU in Tegra 4 is again an evolution of its predecessors. However, numerous feature additions and efficiency improvements were implemented. The number of processing resources was dramatically increased, and clock rate increased as well. In 3D tests, the Tegra 4 GPU is typically several times faster than that of Tegra 3.^[47] Additionally, the Tegra 4 video processor has full support for hardware decoding and encoding of WebM video (up to 1080p 60 Mbit/s @ 60fps).^[48]

Along with Tegra 4, Nvidia also introduced i500, an optional software modem based on Nvidia's acquisition of Icera, which can be reprogrammed to support new network standards. It supports category 3 (100 Mbit/s) LTE but will later be updated to Category 4 (150 Mbit/s).

Common features:

- CPU cache: L1: 32 KB instruction + 32 KB data, L2: 2 MB
- 28 nm HPL semiconductor technology

Model number	CPU	GPU			Memory				Adoption
	Processor (Cores/Freq)	Micro-architecture	Core config ¹	Frequency	Type	Amount	Bus width	Band-width	Availability
T114 ^[49]	4+1 × 1.9 GHz Cortex-A15	VLIW-based VEC4 units ^[50]	72 ^[20] [50] (48:24:4)	672 MHz ^[51]	DDR3L or LPDDR3	?	32-bit dual-channel	up to 14.9 GB/s (1866 MT/s data rate) ^[52] [53]	Q2 2013 ^[54]

¹ Pixel shaders : Vertex shaders : Pixel pipelines (pairs 1x TMU and 1x ROP)

Devices

Model	Devices
T114	Nvidia Shield Portable, Tegra Note 7, Microsoft Surface 2, HP Slate 7 Extreme, ^[55] HP Slate 7 Beats Special Edition, ^[56] HP Slate 8 Pro, ^[57] HP SlateBook x2, ^[58] HP SlateBook 14, ^[59] HP Slate 21, ^[60] ZTE N988S, nabi Big Tab, Nuvola NP-1, Project Mojo, Asus Transformer Pad TF701T, Toshiba AT10-LE-A (Excite Pro), Vizio 10" tablet, Wexler.Terra 7, Wexler.Terra 10, Acer TA272HUL AIO, Xiaomi Mi 3 (TD-LTE version), ^[61] Coolpad 8970L (大观 4), ^[62] Audi Tablet, ^[63] Le Pan TC1020 10.1", ^[64] Matrimax iPLAY 7, ^[65] Kobo Arc 10HD ^[66]

Tegra 4i

The Tegra 4i (codenamed "Grey") was announced on February 19, 2013. With hardware support for the same audio and video formats,^[48] but using Cortex-A9 cores instead of Cortex-A15, the Tegra 4i is a low-power variant of the Tegra 4 and is designed for phones and tablets. Unlike its Tegra 4 counterpart, the Tegra 4i also integrates the Icera i500 LTE/HSPA+ baseband processor onto the same die.

Common features:

- 28 nm HPM semiconductor technology
- CPU cache: L1: 32 KB instruction + 32 KB data, L2: 1 MB

Model number	CPU	GPU			Memory				Adoption
	Processor (Cores/Freq)	Micro-architecture	Core config ¹	Frequency	Type	Amount	Bus width	Band-width	Availability
T148? ^[67]	4+1 × 2.0 GHz Cortex-A9 "R4"	VLIW-based VEC4 units ^[50]	60 ^[50] (48:12:2)	660 MHz ^[51]	LPDDR3		32-bit single-channel	6.4–7.5 GB/s (800–933 MHz) ^[53]	Q1 2014

¹ Pixel shaders : Vertex shaders : Pixel pipelines (pairs 1x TMU and 1x ROP)

Devices

Model	Devices
T148?	Blackphone, LG G2 mini LTE, Wiko Highway 4G, ^[68] Explay 4Game, ^[69] Wiko Wax ^[70] [71] QMobile Noir LT-250 ^[72]

Tegra K1

Nvidia's Tegra K1 (codenamed "Logan") features ARM Cortex-A15 cores in a 4+1 configuration similar to Tegra 4, or Nvidia's 64-bit Project Denver dual-core processor as well as a Kepler graphics processing unit with support for Direct3D 12, OpenGL ES 3.1, CUDA 6.5, OpenGL 4.4/OpenGL 4.5, and Vulkan.^[73][74] Nvidia claims that it outperforms both the Xbox 360 and the PS3, whilst consuming significantly less power.^[75]

Support Adaptive Scalable Texture Compression.^[76]

In late April 2014, Nvidia shipped the "Jetson TK1" development board containing a Tegra K1 SoC and running Ubuntu Linux.^[77]

- Processor:
 - 32-bit variant quad-core ARM Cortex-A15 MPCore R3 + low power companion core
 - or 64-bit variant with dual-core Project Denver^[78] (variant once codenamed "Stark"^[79])
- GPU consisting of 192 ALUs using Kepler technology
- 28 nm HPM process
- Released in Q2 2014
- Power consumption: 8 watts^[75]

Model	CPU	GPU			Memory				Adoption	
	Processor (Cores/Freq)	Micro-architecture	Core config ¹	Frequency	GFLOPS (FP32)	Type	Amount	Bus width	Band-width	Availability
T124 ^[80] [81]	4+1 × 2.3 GHz Cortex-A15 R3 (32-bit)	GK20A (Kepler)	192:8:4	756–951 MHz	290–365	DDR3L, LPDDR3	max 8 GB (with 40-bit address extension ²)	64-bit	17 GB/s	Q2 2014
T132 ^[82] [83]	2x 2.5GHz Denver (64-bit)						max 8 GB	?	?	Q3 2014

- ¹ Unified Shaders : Texture mapping units : Render output units
² ARM Large Physical Page Extension (LPAE) supports 1 TiB (2⁴⁰ bytes).
The 8 GiB limitation is part-specific.

Devices

Model	Devices
T124	Jetson TK1 development board, ^[84] Nvidia Shield Tablet, ^[85] Acer Chromebook 13, ^[86] HP Chromebook 14 G3, ^[87] Xiaomi MiPad, ^[88] Snail Games OBox, UTStarcom MC8718, Google Project Tango tablet, ^[89] Fuze Tomahawk F1, ^[90] Apalis TK1 System on Module, ^[91] JXD Singularity S192 ^[92]
T132	HTC Nexus 9 ^{[93][94]}

In December 2015, the web page of wccftech.com published an article stating that Tesla is going to use a Tegra K1 based design derived from the template of the Nvidia Visual Computing Module (VCM) for driving the infotainment systems and providing visual driving aid in the respective vehicle models of that time.^[95] This news has, as of now, found no similar successor or other clear confirmation later on in any other place on such a combination of a multimedia with an auto pilot system for these vehicle models.

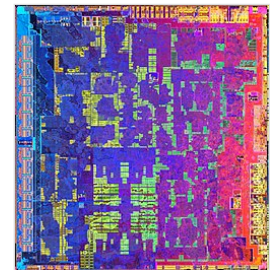
Tegra X1

Released in 2015, Nvidia's Tegra X1 (codenamed "Erista") features two CPU clusters, one with four ARM Cortex-A57 cores and the other with four ARM Cortex-A53 cores, as well as a Maxwell-based graphics processing unit.^{[96][97]} It supports Adaptive Scalable Texture Compression.^[76] Only one cluster of cores can be active at once, with the cluster switch being handled by software on the BPMP-L. Devices utilizing the Tegra X1 have only been seen to utilize the cluster with the more powerful ARM Cortex-A57 cores. The other cluster with four ARM Cortex-A53 cores cannot be accessed without first powering down the Cortex-A57 cores (both clusters must be in the CC6 off state).^[98] Nvidia has removed the ARM Cortex-A53 cores from later versions of technical documentation, implying that they have been removed from the die.^{[99][100]} The Tegra X1 was found to be vulnerable to a Fault Injection (FI) voltage glitching attack, which allowed for arbitrary code execution and homebrew software on the devices it was implemented in.^[101]



Tegra X1 in Nvidia Shield TV

A revision (codenamed "Mariko") with greater power efficiency, named officially as **Tegra X1+** was released in 2019,^[102] fixing the Fusée Gelée (meaning: Frozen Rocket)^{[103][104]} exploit as reported by Katherine Temkin (founder of Insomnia Security, an advocate for secure hardware)^[105]. That revision is also known as model numbers T214 and T210B01.



Die shot of the Tegra X1

- CPU: ARMv8 ARM Cortex-A57 quad-core (64-bit) + (unused?) ARM Cortex-A53 quad-core (64-bit)
- GPU: Maxwell-based 256 core GPU (Jetson Nano: only 128 cores)
- MPEG-4 HEVC VP8 encoding/decoding & VP9 decoding support^[106] (Jetson Nano: encoders are H.265, H.264/Stereo, VP8, JPEG; decoders are H.265, H.264/Stereo, VP8, VP9, VC-1, MPEG-2, JPEG)
- TSMC 20 nm process for the Tegra X1
- TSMC 16 nm process for the Tegra X1+.
- TDP:
 - T210: 15 W,^[107] with average power consumption less than 10 W^[106]
 - Jetson Nano: 10 W (mode 0);^[108] mode 1: 5W (only 2 CPU cores @ 918 MHz, GPU @ 640 MHz)

Model number	SoC / Variant	Process	CPU		GPU			Memory				Adoption
			Processor (Cores/Freq ¹)	Micro-architecture	Frequency (Core config ²)	GFLOPS (FP32)	GFLOPS (FP16)	Type	Amount ³	Bus width	Bandwidth ⁴	Availability
T210	ODNX02-A2 TM670D-A1 TM670M-A2 TM671D-A2	TSMC 20 nm	4 × 2.2 GHz ^[109] Cortex-A57 + 4 × 1.3 GHz Cortex-A53	GM20B (Maxwell) ^{[110]:14}	1000 MHz (256:16:16) ^{[110]:753}	512	1024	LPDDR3 LPDDR4	8 GB	64-bit	25.6 GB/s	Q2 2015
	TM660M-A2		4 × 1.4 GHz Cortex-A57 + 4 × 1.0 GHz Cortex-A53		921 MHz (128:16:16) :773	236	472	LPDDR3? LPDDR4	4 GB			March 2019
T214 / T210b01	ODNX10-A1 TM675M-A1	TSMC 16 nm	4 × 2.1 GHz ^[111] Cortex-A57	GM21B (Maxwell) ^[112]	1267 MHz (256:16:16) ^[113]	649	1298	LPDDR4 LPDDR4X	8 GB			

¹ CPU frequency may be clocked differently than the maximum validated by Nvidia at the OEM's discretion

² Unified Shaders : Texture mapping units : Render output units

³ Maximum validated amount of memory, implementation is board specific

⁴ Maximum validated memory bandwidth, implementation is board specific

Devices

Model	SoC / Variant	Devices
T210	ODNX02-A2	Nintendo Switch (2017, HAC-001) ^{[114][115]}
	TM670D-A1	Nvidia Shield Android TV (2015)
	TM670M-A2	Nvidia Shield Android TV (2017)
	TM660M-A2	Jetson Nano 4 GB, Jetson Nano 2 GB
	TM671D-A2	Google Pixel C
	TM670D-A2	Nvidia Jetson TX1 development board, ^[115] Nvidia Drive CX & PX
T210b01	ODNX10-A1	Nintendo Switch (2019, HAC-001(-01)), Nintendo Switch Lite (HDH-001), Nintendo Switch: OLED Model (HEG-001)
	TM675M-A1	Nvidia Shield Android TV (2019)



The X1 is the basis for the [Nintendo Switch](#) video game console.

Tegra X2

Nvidia's Tegra X2^{[116][117]} (codenamed "Parker") features Nvidia's own custom general-purpose ARMv8-compatible core Denver 2 as well as code-named Pascal graphics processing core with GPGPU support.^[118] The chips are made using FinFET process technology using TSMC's 16 nm FinFET+ manufacturing process.^{[119][120][121]}

- CPU: Nvidia Denver2 ARMv8 (64-bit) dual-core + ARMv8 ARM Cortex-A57 quad-core (64-bit)
- RAM: up to 8 GB LPDDR4^[122]
- GPU: Pascal-based, 256 CUDA cores; type: GP10B^[123]
- TSMC 16 nm, FinFET process
- TDP: 7.5–15 W^[124]

Model number	SoC Variant	CPU		GPU			Memory				Adoption
		Processor (Cores / Freq)	Micro-architecture	Frequency (Core config ¹)	GFLOPS (FP32)	GFLOPS (FP16)	Type	Amount	Bus width	Bandwidth	Availability
T186	Tegra X2 (Parker)	2 × 1.4–2.0 GHz Denver2 + 4 × 1.2–2.0 GHz Cortex-A57	GP10B (Pascal) ^[125]	854–1465 MHz 256:16:16 (2) ^[126]	437–750	874–1500	LPDDR4	8 GB	128-bit	59.7 GB/s	

¹ Unified Shaders : Texture mapping units : Render output units (SM count)

Devices

Model	Devices
T186	Nvidia Drive PX2 (variants), ZF ProAI 1.1 ^[127]
T186	Nvidia Jetson TX2 ^[124]
Unknown	Mercedes-Benz MBUX (infotainment system) ^[128]
Unknown	1 unit along with 1 GPU semiconductor is part of the ECU for "Tesla vision" functionality in all Tesla vehicles since October 2016 ^{[129][130]}
T186	Magic Leap One ^{[131][132]} (mixed environment glasses)
Unknown	Skydio 2 (drone) ^[133]

Xavier

The Xavier Tegra SoC, named after the comic book character [Professor X](#), was announced on 28 September 2016, and by March 2019, it had been released.^[134] It contains 7 billion transistors and 8 custom ARMv8 cores, a Volta GPU with 512 CUDA cores, an open sourced TPU (Tensor Processing Unit) called DLA (Deep Learning Accelerator).^{[135][136]} It is able to encode and decode 8K Ultra HD (7680×4320). Users can configure operating modes at 10 W, 15 W, and 30 W TDP as needed and the die size is 350 mm².^{[137][138][139]} Nvidia confirmed the fabrication process to be 12 nm FinFET at CES 2018.^[140]

- CPU: Nvidia custom Carmel ARMv8.2-A (64-bit), 8 cores 10-wide superscalar^[141]
- GPU: Volta-based, 512 CUDA cores with 1.4 TFLOPS;^[142] type: GV11B^{[143][123]}
- TSMC 12 nm, FinFET process^[140]
- 20 TOPS DL and 160 SPECint @ 20 W;^[137] 30 TOPS DL @ 30 W^[139] (TOPS DL = Deep Learning Tera-Ops)
 - 20 TOPS DL via the GPU based tensor cores
 - 10 TOPS DL (INT8) via the DLA unit that shall achieve 5 TFLOPS (FP16)^[142]
- 1.6 TOPS in the PVA unit (Programmable Vision Accelerator,^[144] for StereoDisparity/OpticalFlow/ImageProcessing)
- 1.5 GPix/s in the ISP unit (Image Signal Processor, with native full-range HDR and tile processing support)
- Video processor for 1.2 GPix/s encoding and 1.8 GPix/s decode^[142] including 8k video support^[138]
- MIPI-CSI-3 with 16 lanes^{[145][146]}
- 1 Gbit/s Ethernet
- 10 Gbit/s Ethernet

Module (Model)	SoC Variant	CPU	GPU				Deep Learning	Memory			Adoption	TDP (W)	
		Processor (Cores/Freq)	Micro-architecture	Frequency (Core config ¹)	TFLOPS (FP32)	TFLOPS (FP16)		TOPS (INT8)	Type	Amount	Bus width		Bandwidth
Xavier AGX	64 GB	Carmel (12 MB cache) 8x 2.0 GHz	GV11B (Volta)	1377 MHz 512:64 (8, 4, 1)	1.41	2.82	32	LPDDR4X	64 GB	256-bit	136.5 GB/s		10-30
Xavier AGX	32 GB								32 GB				
Xavier AGX	Industrial	Carmel (12 MB cache) 8x 2.0 GHz		1221 MHz 512:64 (8, 4, 1)	1.24	2.48	30	LPDDR4X	32 GB	256-bit	136.5 GB/s		20-40
Xavier NX	16 GB	Carmel (10 MB cache) 6x 1.9 GHz	Volta	1100 MHz 384:48 (6, 3, 1)	0.84	1.69	21	LPDDR4X	16 GB	128-bit	59.7 GB/s		10-20
Xavier NX	8 GB								8 GB				

¹ CUDA cores : Tensor cores (SMs, TPCs, GPCs)

Devices

Model	SoC Variant	Devices
T194	Unknown	Nvidia Drive Xavier (Drive PX-series) ^[147] (formerly named Xavier AI Car Supercomputer)
	Unknown	Nvidia Drive Pegasus (Drive PX-series) ^[147]
	Unknown	Nvidia Drive AGX Xavier Developer Kit ^[148]
	Unknown	Nvidia Jetson AGX Xavier Developer Kit ^[149]
	Unknown	Nvidia Jetson Xavier ^[149]
	TE860M-A2	Nvidia Jetson Xavier NX ^[150]
	Unknown	Nvidia Clara AGX ^[151] "Clara AGX is based on NVIDIA Xavier and NVIDIA Turing GPUs." ^[152]
	Unknown	Bosch and Nvidia designed Self Driving System ^[153]
	Unknown	ZF ProAI ^{[154][155]}

On the Linux Kernel Mailing List, a Tegra194 based development board with type ID "P2972-0000" got reported:

The board consists of the P2888 compute module and the P2822 baseboard.^[156]

Orin

Nvidia announced the next-gen SoC codename Orin on March 27, 2018, at GPU Technology Conference 2018.^[157]

It contains 17 billion transistors and 12 ARM Hercules cores and is capable of 200 INT8 TOPs @ 65W.^[158]
The Drive AGX Orin board system family was announced on December 18, 2019, at GTC China 2019.

Nvidia has sent papers to the press documenting that the known (from Xavier series) clock and voltage scaling on the semiconductors

and by pairing multiple such chips a wider range of application can be realized with the thus resulting board concepts.^[159]
In early 2021, Nvidia announced the Chinese vehicle company NIO will be using an Orin-based chip in their cars.^[160]

The so far published specifications for Orin are:

- **CPU:** 12× Arm Cortex-A78AE (*Hercules*) ARMv8.2-A (64-bit)^{[161][162]}
- **GPU:** Ampere-based, 2048^[160] CUDA cores and 64 tensor cores¹; "with up to 131 Sparse TOPs of INT8 Tensor compute, and up to 5.32 FP32 TFLOPs of CUDA compute."^[163]
 - 5.3 CUDA TFLOPs (FP32)^[164]
 - 10.6 CUDA TFLOPs (FP16)^[164]
- Samsung 8N process (derived from 8LPU)^{[164][165]}
- 275 TOPS (INT8) DL^[164]
 - 170 TOPS DL (INT8) via the GPU
 - 105 TOPS DL (INT8) via the 2x NVDLA 2.0 units (DLA, Deep Learning Accelerator)
- 85 TOPS DL (FP16)^[164]
- 5 TOPS in the PVA v2.0 unit (Programmable Vision Accelerator for Feature Tracking)
- 1.85 GPix/s in the ISP unit (Image Signal Processor, with native full-range HDR and tile processing support)
- Video processor for ? GPix/s encoding and ? GPix/s decode
- 4× 10 Gbit/s Ethernet, 1× 1 Gbit/s Ethernet

¹ Orin uses the double-rate tensor cores in the A100, not the standard tensor cores in consumer Ampere GPUs.

Nvidia announced the latest member of the family, "Orin Nano" in September 2022 at the GPU Technology Conference 2022.^[166]

The Orin product line now features SoC and SoM (System-On-Module) based on the core Orin design and scaled for different uses from 60W all the way down to 5W. While less is known about the exact SoC's that are being manufactured, Nvidia has publicly shared detailed technical specifications about the entire Jetson Orin SoM product line. These module specifications illustrate how Orin scales providing insight into future devices that contain an Orin derived SoC.

Module (Model)	SoC Variant	CPU		GPU			Deep Learning	Memory			Adoption		
		Processor (Cores × Freq)	Micro-architecture	Frequency (Core config ¹)	TFLOPS (FP32)	TFLOPS (FP16)	TOPS (INT8)	Type	Amount	Bus width	Bandwidth	Availability	
Orin AGX 64 GB ^{[167][168]}		Cortex-A78AE (9 MB cache) 12× 2.2 GHz	Ampere	1300 MHz 2048:64:8 (16, 8, 2)	5.32 ^[163]	10.649	275	LPDDR5	64 GB	256-bit	204.8 GB/s	Sample: 2021, Dev-Kit: Q1 2022, Prod: Dec 2022	
Orin AGX 32 GB ^[169]		Cortex-A78AE (6 MB cache) 8× 2.2 GHz		930 MHz 1792:56:7 (14, 7, 2)	3.365 ^[163]	6.73	200		32 GB			Oct 2022	
Orin NX 16 GB ^[170]	TE980-M ^[171]	Cortex-A78AE (6 MB cache) 8× 2.0 GHz		918 MHz 1024:32:4 (8, 4, 1)	1.88	3.76	100		16 GB	128-bit	102.4 GB/s	Dec 2022	
Orin NX 8 GB ^[169]	TE980-M ^[171]	Cortex-A78AE (5.5 MB cache) 6× 2.0 GHz		765 MHz 1024:32:4 (8, 4, 1)	1.57	3.13	70		8 GB			68 GB/s	Jan 2023
Orin Nano 8 GB ^[169]		Cortex-A78AE (5.5 MB cache) 6× 1.5 GHz		625 MHz 1024:32:4 (8, 4, 1)	1.28	2.56	40						
Orin Nano 4 GB ^[169]				625 MHz 512:16:2 (4, 2, 1)	0.64	1.28	20						

Module (Model)	SoC Variant	CPU		GPU			Deep Learning	Memory			Adoption	
		Processor (Cores × Freq)	Micro-architecture	Frequency (Core config ¹)	TFLOPS (FP32)	TFLOPS (FP16)	TOPS (INT8)	Type	Amount	Bus width	Bandwidth	Availability
Orin Nano Super 8 GB ^[172]		Cortex-A78AE (5.5 MB cache) 6× 1.7 GHz	Ampere	1020 MHz 1024:32:4 (8, 4, 1)	2.09	4.18	67	LPDDR5	8 GB	128-bit	102.4 GB/s	Dec 2022

¹ CUDA cores : Tensor cores : RT cores (SMs, TPCs, GPCs)

Devices

Model	Devices	Comments
T234 ^[173]	Nvidia Jetson AGX Orin ^{[174][163]}	comes in 32 GB and 64 GB RAM configurations, available as standalone module or devkit; intended for industrial robotics and/or embedded HPC applications
Unknown	Nvidia Jetson Orin NX ^[170]	mid-power SODIMM-form factor Orin-series module, available only as standalone module; pin-compatible with Xavier NX carrier
Unknown	Nvidia Jetson Orin Nano ^[175]	low-power, cost-effective SODIMM-form factor Orin-series module, available as standalone module or devkit; intended for entry-level usage
Unknown	Nvidia DRIVE AGX Orin	used in automotive ADAS applications. 1×Orin 12×A78AE 32GB LPDDR5 @100W, 167+87 INT8 TOPS
Unknown	Nio Adam ^{[176][177]}	built from 4× Nvidia Drive Orin, totals to 48 CPU cores and 8,192 CUDA cores; for use in vehicles ET7 in March 2022 and ET5 in September 2022
T239 "Drake"	Nintendo Switch 2	8 × ARM Cortex-A78C, ^[178] 1536 Ampere CUDA cores, ^[179] 102.4 GB/s LPDDR5X ^[180]

Grace

The Grace CPU is an NVIDIA-developed ARM Neoverse V2 (*Demeter*) CPU platform, targeted at large-scale AI and HPC applications, available within several NVIDIA products. The NVIDIA OVX platform combines the Grace Superchip (two Grace dies on one board) with desktop NVIDIA GPUs in a server form-factor, while the NVIDIA HGX platform is available with either the Grace Superchip or the Grace Hopper Superchip.^[181]

The latter is an HPC platform in and of itself, combining a Grace CPU with a Hopper-based GPU, announced by NVIDIA on March 22, 2022.^[182]

Linux kernel patch sets indicate that a single Grace CPU is also known as T241, placing it under the Tegra SoC branding, despite the chip itself not including a GPU (a referenced T241 patch set cites impact to "NVIDIA server platforms that use more than two T241 chips...interconnected," pointing to the Grace Superchip design).^[183]

Model number	CPU			Memory				Adoption
	Processor (Cores/Frequency)	Cache	TFLOPS (FP64)	Type	Amount	Bus width	Bandwidth	Availability
T241 ^[184]	Grace - 72x ARM Neoverse V2 cores (ARMv9) ^[185]	L1: 64 KB I-cache + 64 KB D-cache per core L2: 1 MB per core L3: 117 MB shared ^[185]	3.55 ^[185]	LPDDR5X ECC ^[185]	Up to 480 GB ^[185]	?	500 GB/s ^[185]	H2 2023 ^[186]

¹Figures cut in half from full Grace Superchip specification

Atlas

Nvidia announced the next-gen SoC codename Atlas on April 12, 2021,^[187] at GPU Technology Conference 2021.^[188]

Nvidia announced the cancellation of Atlas on September 20, 2022, and their next SoC will be Thor.^[189]

Functional units known so far are:

- Grace Next CPU^[188]
- Ada Lovelace GPU^[190]
- Bluefield DPU (Data Processing Unit)
- other Accelerators
- Security Engine
- Functional Safety Island
- On-Chip-Memory
- External Memory Interface(s)
- High-Speed-IO Interfaces

Model number	CPU	GPU					Deep Learning	Memory				Adoption
	Processor (Cores/Freq)	Micro-architecture	Core config ¹	Freq	GFLOPS (FP32)	GFLOPS (FP16)	TOPS (INT8)	Type	Amount	Bus width	Bandwidth	Availability
T254?	Grace-Next ^[188] (??)	Ada Lovelace ^[190]	?	?	?	?	>1000 ^[190]	?	?	?	?	Cancelled ^[190] Sept.2022

Thor

Nvidia announced the next-gen SoC codename Thor on September 20, 2022, at GPU Technology Conference 2022, replacing the cancelled Atlas.^[189]

A patchset adding support for Tegra264 to mainline Linux was submitted May 5, 2023, likely indicating initial support for Thor.^[191]

The ARM Neoverse V3AE (Poseidon-AE) CPU is built to deliver maximum performance for automotive applications, central compute and machine learning (ML) workloads.^[192]

Model number	CPU	GPU					Deep Learning	Memory				Adoption	TDP (W)
	Processor (Cores/Freq)	Micro-architecture	Core config ¹	Freq.	TFLOPS (FP32)	TFLOPS (FP16)	TOPS (FP8)	Type	Amount	Bus width	Bandwidth	Availability	
T264 ^[193]	12x Neoverse V3AE (2.6 GHz)	Blackwell	1536:64:? (12, 6, 2)	1575 MHz	4.838	?	600 ^[189]	LPDDR5X	64 GB	256-bit	273 GB/s	2025 ^[189]	40-70
	14 x Neoverse V3AE ^[194] (2.6 GHz)		2560:96:? (20, 10, 3)		8.064	500	1035 ^[189]		128 GB				40-130

Devices

- Nvidia DRIVE Thor^{[189][195]}
- Jetson AGX Thor^[196]

Comparison

Generation		Tegra 2 (Ventana)	Tegra 3 (Kal-EI)	Tegra 4 (Wayne)	Tegra 4i (Grey)	Tegra K1 (Logan)		Tegra X1 (Erista)	Tegra X1+ (Mariko)	Tegra X2 (Parker)	Tegra Xavier	Tegra Orin	
CPU	Models	T25	T30/T33	T114	T148?	T124	T132	T210	T214	T186	T194	T234	
	Cores	2 × Cortex-A9	4+1 × Cortex-A9	4+1 × Cortex-A15	4+1 × Cortex-A9	4+1 × Cortex-A15	2 × Denver	4 × Cortex-A53 + 4 × Cortex-A57		2 × Denver2 + 4 × Cortex-A57	8 × Carmel	12 × Cortex-A78AE	
	Instruction set	ARMv7-A (32-bit)					ARMv8-A (64-bit)				ARMv8.2-A (64-bit)		
	L1 cache (I/D)	32/32 KB					128/64 KB	32/32 KB + 64/32 KB		128/64 KB + 48/32 KB		128/64 KB	64/
	L2 cache	1 MB		2 MB			128 KB + 2 MB		2 MB + 2 MB		8 MB	3 MB	
	L3 cache	N/A										4 MB	6 MB
GPU	Architecture	Vec4				Kepler		Maxwell		Pascal		Volta	Ampere
	CUDA cores	4+4*	8+4*	48+24*	48+12*	192		256		512		2048	
	Tensor cores	N/A										64	
	RT cores	N/A										8	
RAM	Protocol	DDR2/LPDDR2	DDR3/LPDDR2	DDR3/LPDDR3			LPDDR3/LPDDR4	LPDDR4/LPDDR4X				LPDDR5	
	Max. size	1 GB	2 GB	4 GB			8 GB				64 GB		
	Bandwidth	2.7 GB/s	6.4 GB/s		7.5 GB/s	14.9 GB/s		25.6 GB/s	34.1 GB/s	59.7 GB/s	136.5 GB/s	204.8 GB/s	
Process		40 nm		28 nm			20 nm		16 nm		12 nm	8 nm	

* VLIW-based Vec4: Pixel shaders + Vertex shaders. Since Kepler, Unified shaders are used.

Software support

FreeBSD

FreeBSD supports a number of different Tegra models and generations, ranging from Tegra K1,^[199] to Tegra 210.^[200]

Linux

Nvidia distributes proprietary device drivers for Tegra through OEMs and as part of its "Linux for Tegra" (formerly "L4T") development kit, also Nvidia provides JetPack SDK with "Linux for Tegra" and other tools with it. The newer and more powerful devices of the Tegra family are now supported by Nvidia's own Vibrante Linux distribution. Vibrante comes with a larger set of Linux tools plus several Nvidia provided libraries for acceleration in the area of data processing and especially image processing for driving safety and automated driving up to the level of deep learning and neuronal networks that make e.g. heavy use of the CUDA capable accelerator blocks, and via OpenCV can make use of the NEON vector extensions of the ARM cores.

As of April 2012, due to different "business needs" from that of their GeForce line of graphics cards, Nvidia and one of their Embedded Partners, Avionic Design GmbH from Germany, are also working on submitting open-source drivers for Tegra upstream to the mainline Linux kernel.^{[201][202]} Nvidia co-founder & CEO laid out the Tegra processor roadmap using Ubuntu Unity in GPU Technology Conference 2013.^[203]

By end of 2018 it is evident that Nvidia employees have contributed substantial code parts to make the T186 and T194 models run for HDMI display and audio with the upcoming official Linux kernel 4.21 in about Q1 2019. The affected software modules are the open source Nouveau and the closed source Nvidia graphics drivers along with the Nvidia proprietary CUDA interface.^[204]

As of May, 2022, NVIDIA has open-sourced their GPU kernel modules for both Jetson and desktop platforms, allowing all but proprietary userspace libraries to be open-source on Tegra platforms with official NVIDIA drivers starting with T234 (Orin).^[205]

QNX

The Drive PX2 board was announced with QNX RTOS support at the April 2016 GPU Technology Conference.^[206]

Similar platforms

SoCs and platforms with comparable specifications (e.g. audio/video input, output and processing capability, connectivity, programmability, entertainment/embedded/automotive capabilities & certifications, power consumption) are:

- A-Series by AllWinner
- Apple silicon by Apple

- Atom by Intel
- Exynos by Samsung
- i.MX by Freescale Semiconductor
- Jaguar and Puma by AMD
- K3Vx/Kirin by HiSilicon
- MTxxxx by MediaTek
- NovaThor by ST-Ericsson
- OCTEON by Cavium
- OMAP / Sitara ARM Processor by Texas Instruments
- Qualcomm Snapdragon
- R-Car by Renesas
- RK3xxx by Rockchip
- VideoCore by Broadcom

See also

- Project Denver
- Nomadik
- XScale
- ZiiLABS

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External links

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