1/4” QSXGA CMOS Image Sensor

GC5004

DataSheet

V1.0

2013-07-29

GalaxyCore Inc.

Content

1. Sensor Overview

1.1 General Description

GC5004 is a high quality 5Mega CMOS image sensor, for mobile phone camera applications and digital camera products. GC5004 incorporates a 2608V x 1976H pixel array, on-chip 10-bit ADC, and image signal processor.

The full scale integration of high-performance and low-power functions makes the GC5004 best fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/4 inch
- 1.4umx1.4um BSI pixel
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD28: 2.7~3.0V
  DVDD15: 1.5V±5%
  IOVDD: 1.7~3.0V
- PLL support
- Windowing support
- MIPI(1_lane/2_lane/4_lane) interface support
- Horizontal/Vertical mirror
- Image processing module
- Package: CSP/wafer

1.3 Application

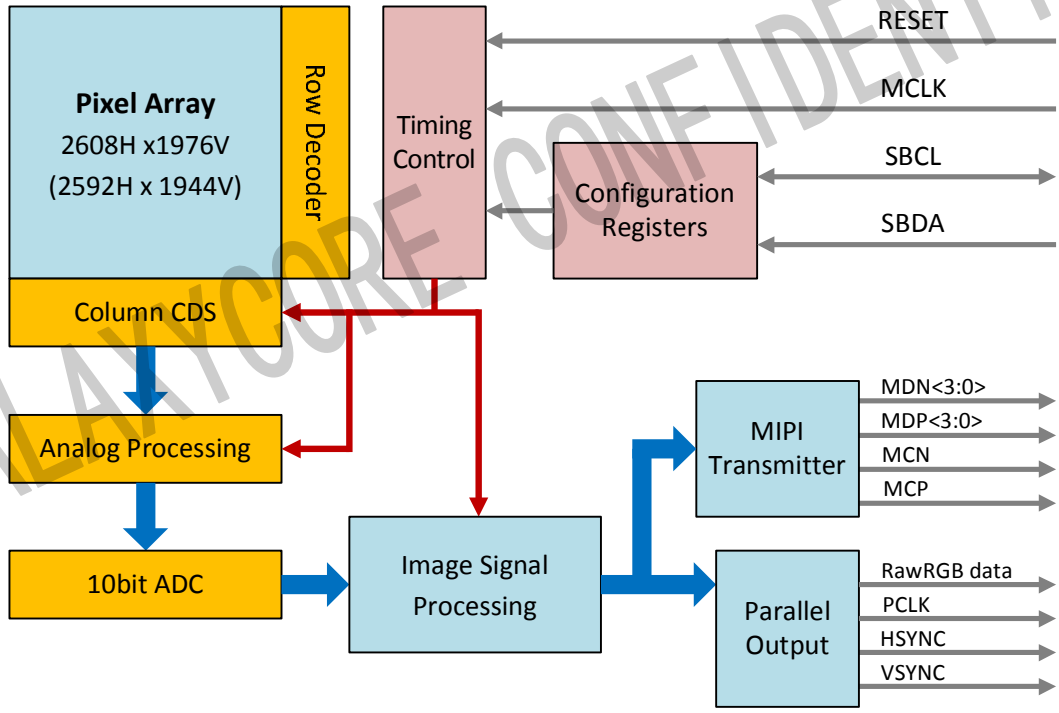
- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/4 inch
Pixel Size	1.4um x 1.4um(BSI)
Active pixel array	2608 x 1976
ADC resolution	10 bit ADC
Max Frame rate	TBD
Power Supply	AVDD28: 2.7~3.0V DVDD15: 1.5V±5% IOVDD: 1.7~3.0V
Power Consumption	TBD
SNR	35.6 dB
Dark Current	30 e-/sec@60℃
Sensitivity	4800 e-/lux • sec
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	29° (non-linear)
Package type	CSP/wafer

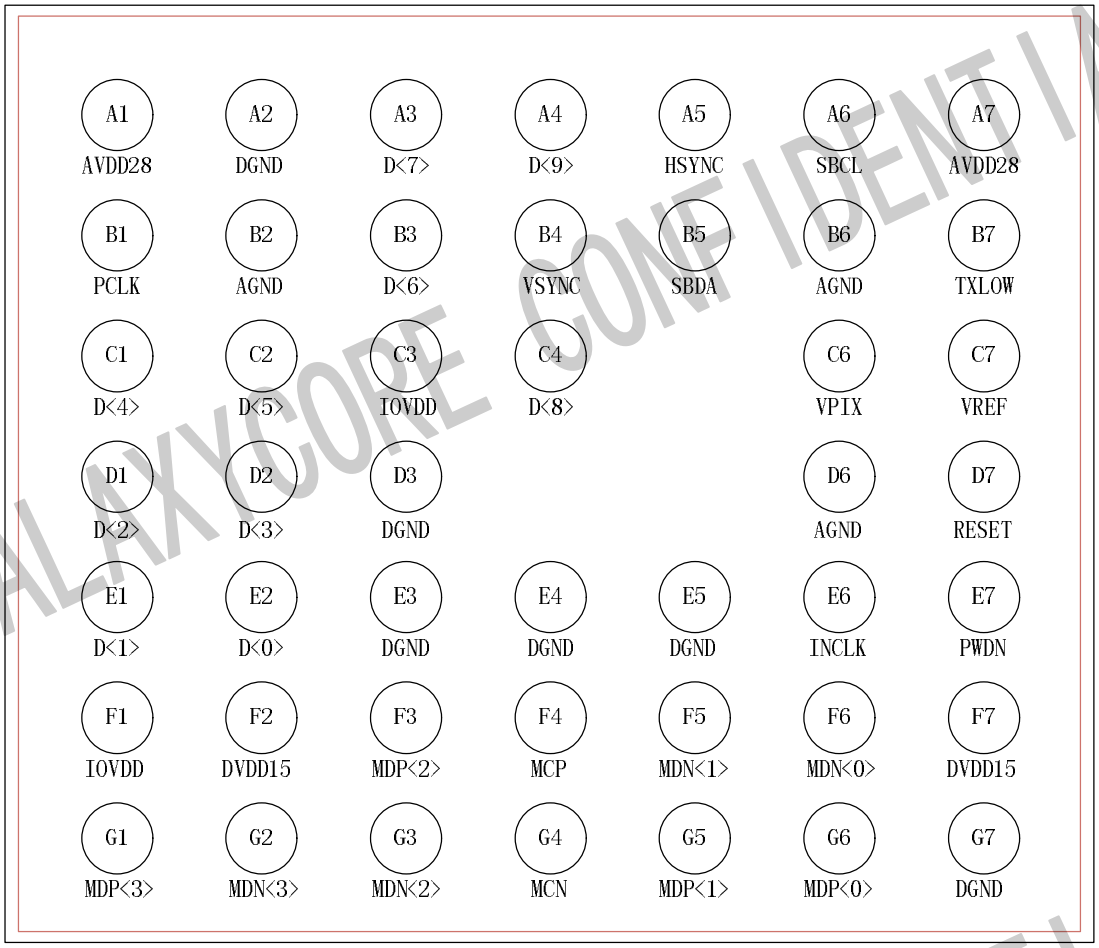
2. Block Diagram

2.1 Block Diagram



GC5004 has an active image array of 2608x1976 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block, including BLK, Gain-CTL and MIPI transmitter. Users can easily control these functions via two-wire serial interface bus.

2.2 Pin Diagram



Top View

2.3 Signal Descriptions

Pin	Name	Pin Type	Function
A1	**AVDD28**	Power	Main power supply pin: 2.7~3.0V, Please connect 0.1μF or 1μF capacity to ground.
A2	**DGND**	Ground	DGND
A3	**D<7>**	Output	Raw RGB data output bit[7]
A4	**D<9>**	Output	Raw RGB data output bit[9]
A5	**HSYNC**	Output	HSYNC output
A6	**SBCL**	Input	Two-wire serial bus, clock
A7	**AVDD28**	Power	Main power supply pin: 2.7~3.0V, Please connect 0.1μF or 1μF capacity to ground.
B1	**PCLK**	Output	Pixel clock output
B2	**AGND**	Ground	AGND
B3	**D<6>**	Output	Raw RGB data output bit[6]
B4	**VSYNC**	Output	VSYNC output

B5	**SBDA**	I/O	Two-wire serial bus, data
B6	**AGND**	Ground	AGND
B7	**TXLOW**	Power	Internal power supply, please connect 0.1μF or 1μF capacity to ground.
C1	**D<4>**	Output	Raw RGB data output bit[4]
C2	**D<5>**	Output	Raw RGB data output bit[5]
C3	**IOVDD**	Power	Power supply for I/O circuits: 1.7~3.0V, Please connect 0.1μF or 1μF capacity to ground.
C4	**D<8>**	Output	Raw RGB data output bit[8]
C6	**Vpix**	Power	Internal power supply, please connect 0.1μF or 1μF capacity to ground.
C7	**Vref**	Power	Internal power supply, please connect 0.1μF or 1μF capacity to ground.
D1	**D<2>**	Output	Raw RGB data output bit[2]
D2	**D<3>**	Output	Raw RGB data output bit[3]
D3	**DGND**	Ground	DGND
D6	**AGND**	Ground	AGND
D7	**RESET**	Input	Chip reset control: 0: chip reset 1: normal work
E1	**D<1>**	Output	Raw RGB data output bit[1]
E2	**D<0>**	Output	Raw RGB data output bit[0]
E3	**DGND**	Ground	DGND
E4	**DGND**	Ground	DGND
E5	**DGND**	Ground	DGND
E6	**INCLK**	Input	Main clock
E7	**PWDN**	Input	Sensor power down control: 0: normal work 1: standby
F1	**IOVDD**	Power	Power supply for I/O circuits: 1.7~3.0V, Please connect 0.1μF or 1μF capacity to ground.
F2	**DVDD15**	Power	Digital power supply pin: 1.5V, please connect 0.1μF or 1μF capacity to ground.
F3	**MDP<2>**	Output	MIPI data<2> (+)
F4	**MCP**	Output	MIPI clock (+)
F5	**MDN<1>**	Output	MIPI data<1> (-)
F6	**MDN<0>**	Output	MIPI data<0> (-)
F7	**DVDD15**	Power	Digital power supply pin: 1.5V, please connect 0.1μF or 1μF capacity to ground.
G1	**MDP<3>**	Output	MIPI data<3> (+)

G2	**MDN<3>**	Output	MIPI data<3> (-)
G3	**MDN<2>**	Output	MIPI data<2> (-)
G4	**MCN**	Output	MIPI clock (-)
G5	**MDP<1>**	Output	MIPI data<1> (+)
G6	**MDP<0>**	Output	MIPI data<0> (+)
G7	**DGND**	Ground	DGND

- **10-bit output (RAW): D<9>~D<0>.**
- **8-bit output (RAW): D<9>~D<2>.**

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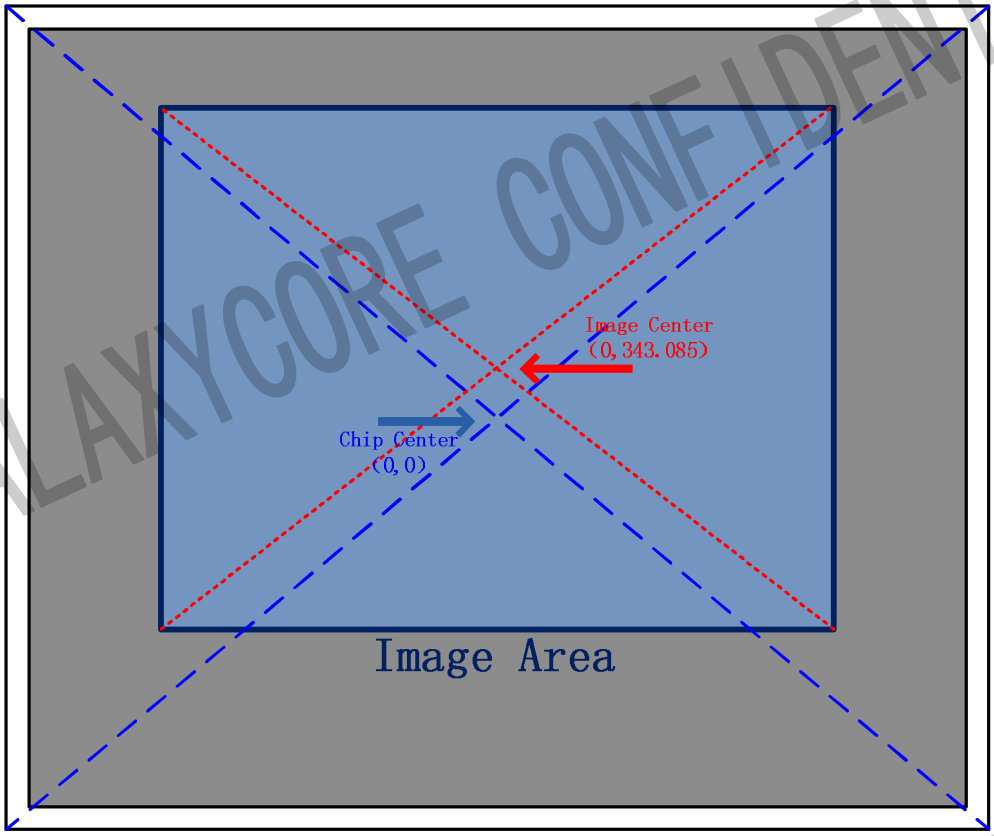
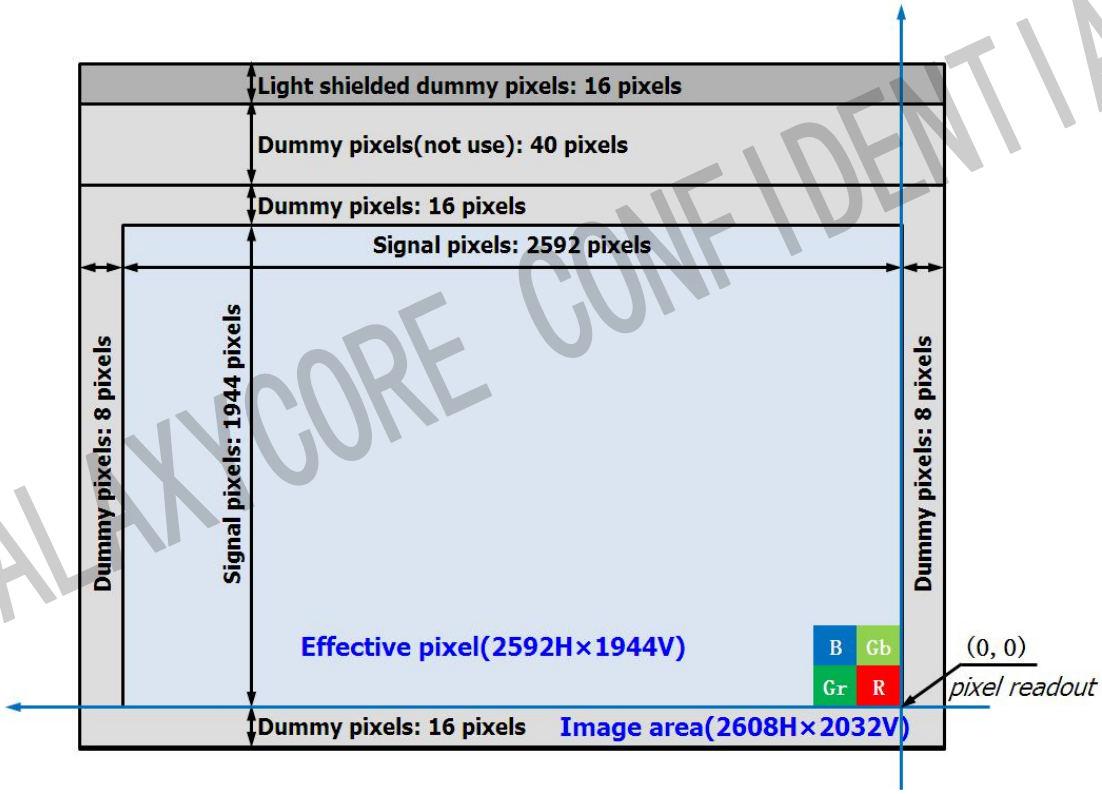
3. Optical Specifications

3.1 Sensor Array Center



3.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 2607. If flip in column, column is read out from 2607 to 0.

If no flip in row, row is read out from 0 to 1975.If flip in row, row is read out from 1975 to 0.

3.3 Lens Chief Ray Angle (CRA)

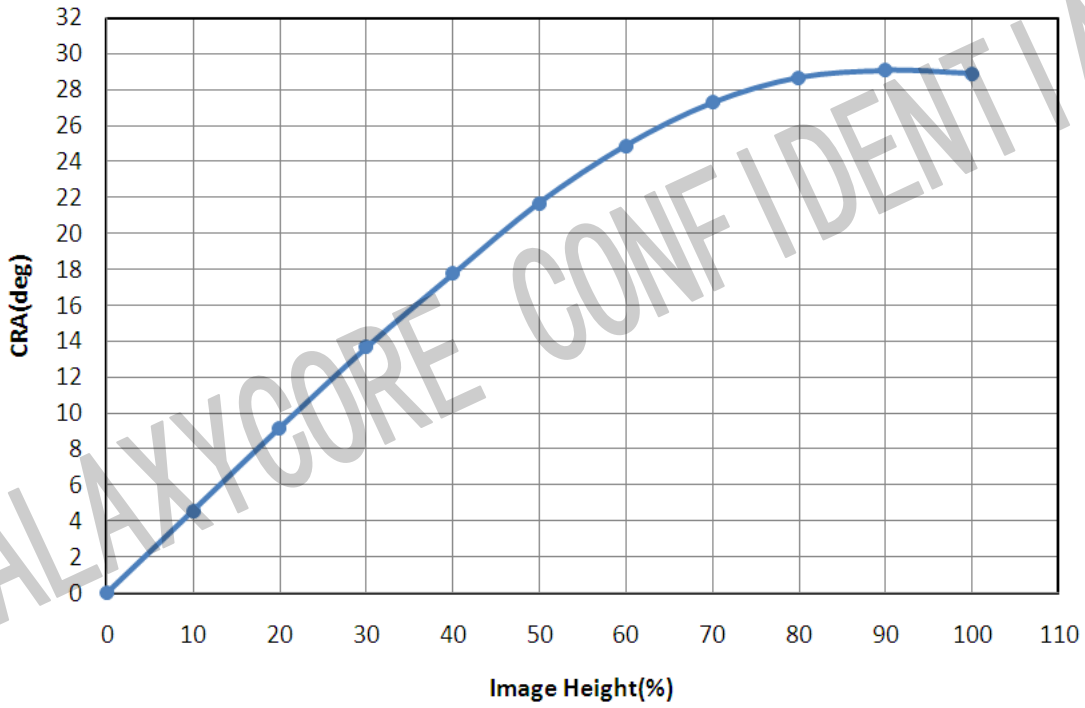
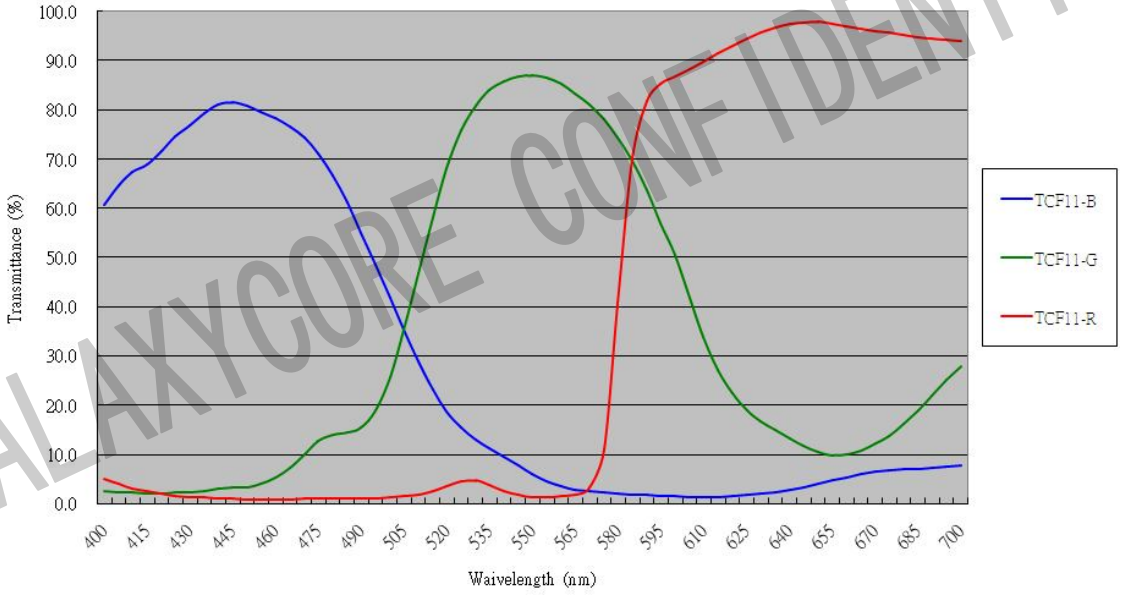


Image Height		CRA
（%）	（mm)	(deg)
0	0.0000	0.0
10	0.2268	4.6
20	0.4536	9.2
30	0.6804	13.7
40	0.9072	17.8
50	1.1340	21.7
60	1.3608	24.9
70	1.5876	27.3
80	1.8144	28.7
90	2.0412	29.1
100	2.2680	28.9

3.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



4. Two-wire Serial Bus Communication

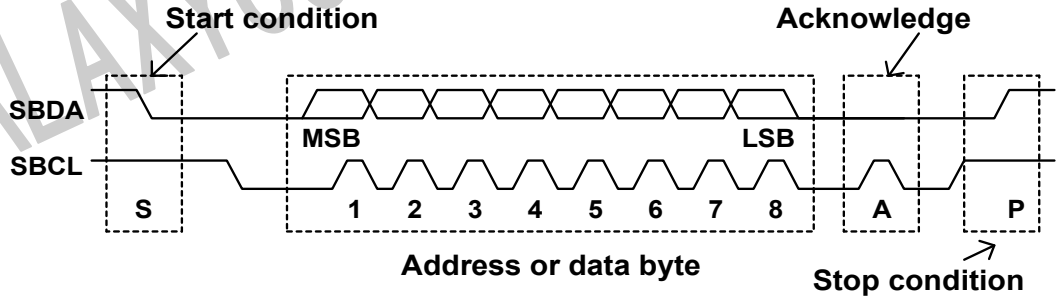
GC5004 Device Address:

serial bus write address = 0x6c, serial bus read address = 0x6d

4.1 Protocol

The host must perform the role of a communications master and GC5004 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	6CH	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	6CH	A	Register Address	A	Data(1)	A	.....	Data(N)	A	P

Single Register Reading:

S	6DH	A	Register Address	A	S	6DH	A	Data	NA	P

Notes:

From master to slave From slave to master

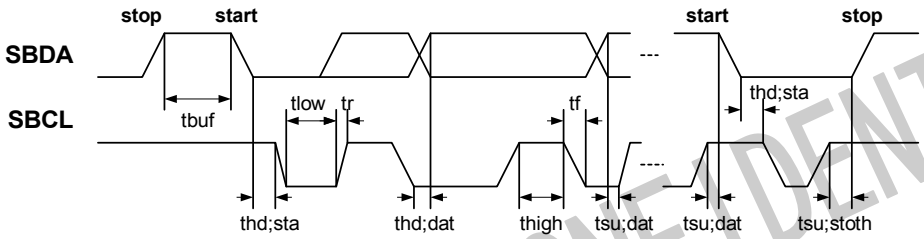
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

4.2 Serial Bus Timing

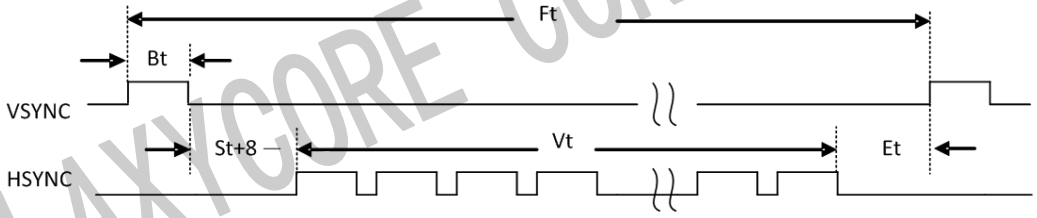


Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a stop and a start	tbuf	1.2	*	μs
Hold time for a repeated start	thd;sta	1.0	*	μs
LOW period of SBCL	tlow	1.2	*	μs
HIGH period of SBCL	thigh	1.0	*	μs
Set-up time for a repeated start	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

5. Applications

5.1 DVP Timing

Suppose Vsync is low active and Hsync is high active, and output format is RAW Bayer 10bit/8bit, then the timing of Vsync and Hsync is bellowing (take capture mode for example, preview mode is the same):



Ft =VB+ Vt +8 (unit is row_time)

VB = Bt + St + Et, Vblank/Dummy line, setting by register P0:0x07 and P0:0x08.

Ft -> Frame time, one frame time.

Bt -> Blank time, Vsync no active time.

St -> Start time, setting by register P0:0x13.

Et –> End time, setting by register P0:0x14.

Vt -> valid line time. QSXGA is 1944, Vt = win_height-32, win_height is setting by register P0:0x0d and P0:0x0e.

When exp_time ≤ win_height + VB, Bt = VB – St - Et. Frame rate is controlled by window_height + VB.

When exp_time > win_height + VB, Bt = exp_time - win_height – St - Et. Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = (Hb + Sh_delay + win_width /4+ 4)/QPCLK.

Hb –> HBlank or dummy pixel，Setting by register P0:0x05 and P0:0x06.

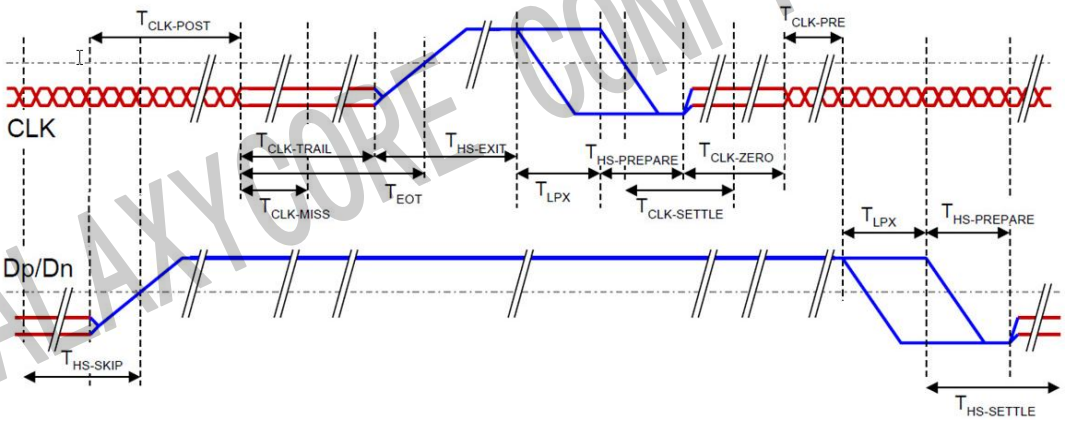
Sh_delay -> Setting by register P0:0x11, P0:0x12.

win_width -> Setting by register P0:0x0f and P0:0x10, win_width = final_output_width + 16. So for QSXGA, we should set win_width as 2608.

QPCLK -> quarter PCLK.

5.2 MIPI

5.2.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

  T_{CLK_PRE}: setting by Register P3: 0x24

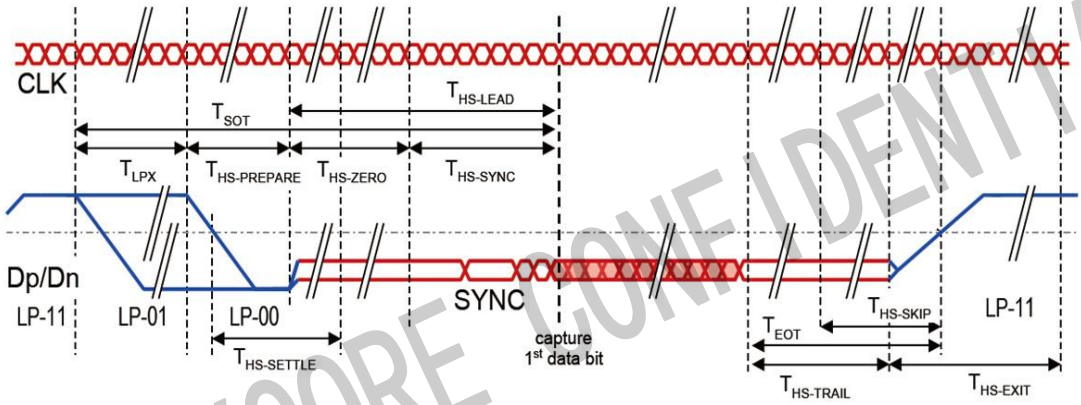
  $T_{CLK\_HS\_PRE}$: setting by Register P3: 0x22

  T_{CLK_POST} : setting by Register P3: 0x25

  T_{CLK_ZERO}: setting by Register P3: 0x23

  T_{CLK_TRAIL}: setting by Register P3: 0x26

5.2.2 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

  T_{LPX}: setting by Register P3:0x21

  $T_{HS\_PREPARE}$: setting by Register P3: 0x29

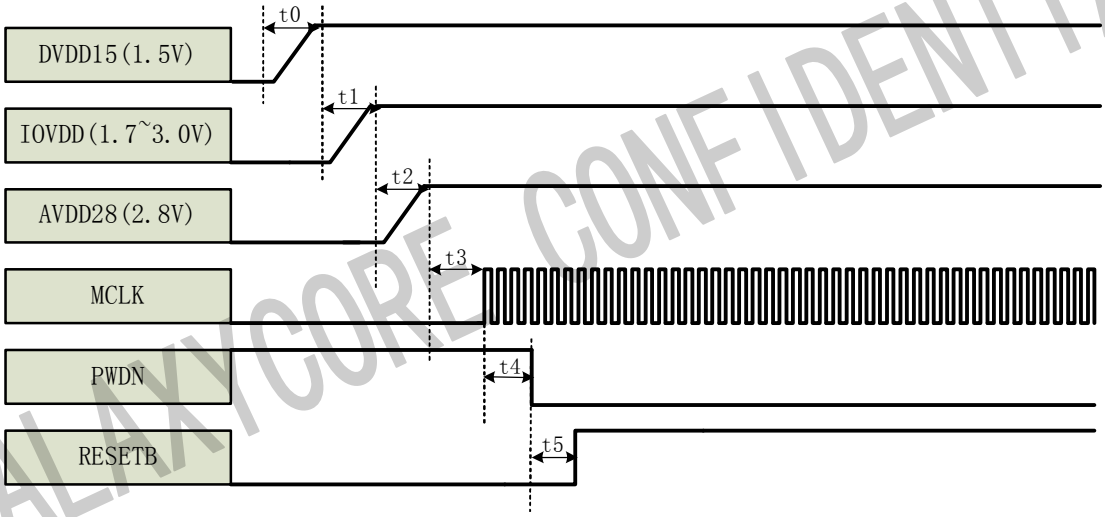
  T_{HS_ZERO}: setting by Register P3: 0x2a

  T_{HS_TRAIL}: setting by Register P3: 0x2b

  T_{HS_EXIT}: setting by Register P3: 0x27

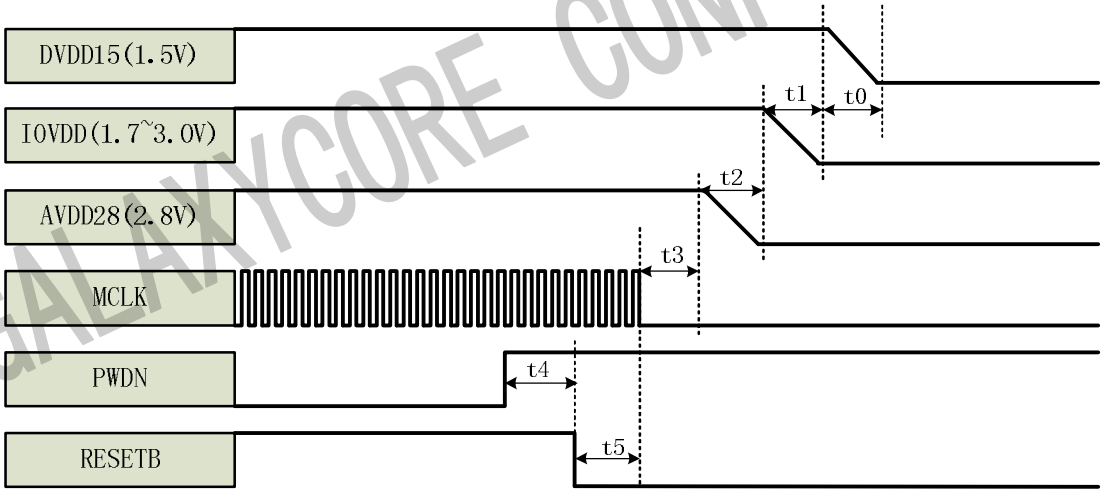
5.3 Power On/Off Sequence

5.3.1 Power On Sequence



Parameter	Description	Min.	Max.	Unit
t0	DVDD15 rising time	100		us
t1	From DVDD15 to IOVDD	50		us
t2	From IOVDD to AVDD28	50		us
t3	From AVDD28 to MCLK applied	>0		us
t4	From MCLK applied to Sensor enable	>0		us
t5	From PWDN pull low to RESET pull high	>0		us

5.3.2 Power Off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From IOVDD to DVDD15 falling time	>0		us
t1	From AVDD28 to IOVDD falling time	>0		us
t2	AVDD28 falling time	>0		us
t3	From MCLK disable to sensor AVDD28 power down	>0		us
t4	From sensor disable to RESET pull low	>0		us
t5	From sensor RESET pull low to MCLK disable	>0		us

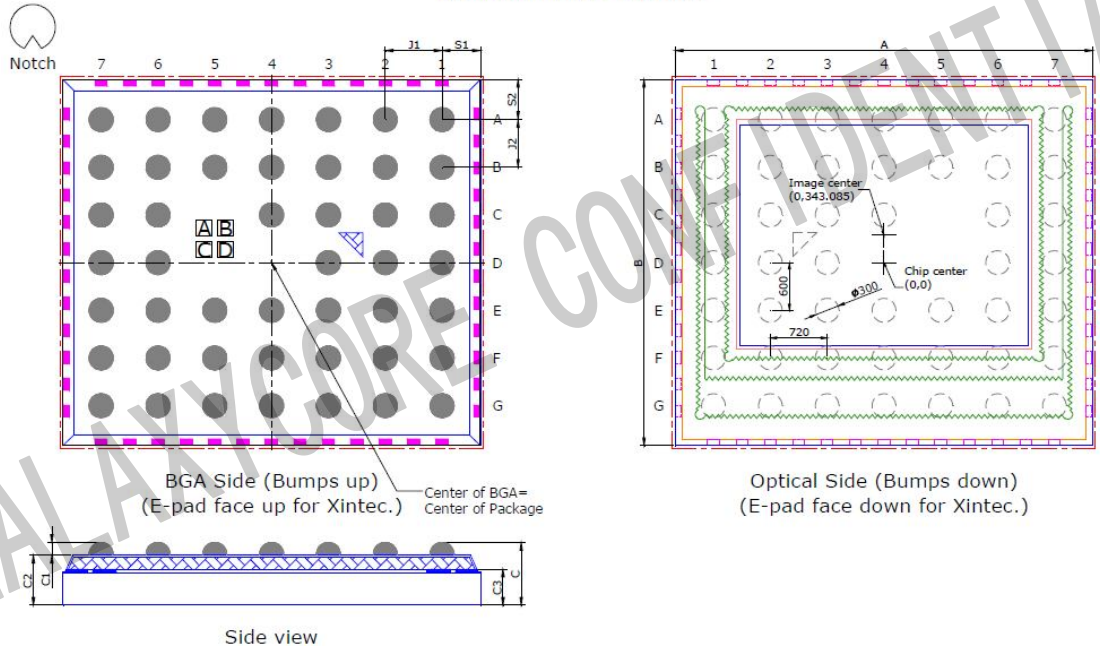
- **Recommended power on/off sequence is above.**
- **If you have special requirements in application, please contact with us to confirm.**

5.4 DC Parameters

Symbol		Parameter	Min	Typ	Max	Unit
Supply						
V_{AVDD28}		Power supply	2.7	2.8	3.0	V
V_{DVDD15}		Supply voltage(digital core)	1.425	1.5	1.575	V
V_{IOVDD}		Supply voltage(digital I/O)	1.7	1.8	3.0	V
I_{AVDD28}		Active(operating) current		TBD	TBD	mA
I_{DVDD15}				TBD	TBD	mA
I_{IOVDD}	1.8V			TBD	TBD	mA
	2.8V			TBD	TBD	mA
I_{DDS_PWD}		Standby Current		TBD	TBD	uA
Digital Input(Typical conditions: AVDD28 = 2.8V，DVDD = 1.5V，IOVDD = 1.8V)						
V_{IH}		Input voltage HIGH	TBD			V
V_{IL}		Input voltage LOW			TBD	V
Digital Output(AVDD28 = 2.8V，standard Loading 25PF，IOVDD = 1.8V)						
V_{OH}		Output voltage HIGH	TBD			V
V_{OL}		Output voltage LOW			TBD	V

6. Package Specification

Mechanical Diagram



Parameter	Symbol	Nominal	Min.	Max.
		μ m		
Package Body Dimension X	A	5290	5265	5315
Package Body Dimension Y	B	4610	4585	4635
Package Height	C	790	730	850
Ball Height	C1	160	130	190
Package Body Thickness	C2	630	585	675
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	300	270	330
Total Pin Count	N	46		
Pins Count X axis	N1	7		
Pins Count Y axis	N2	7		
Pins Pitch X axis	J1	720		
Pins Pitch Y axis	J2	600		
Edge to Pin Center Distance along X	S1	485	455	515
Edge to Pin Center Distance along Y	S2	505	474	535

7. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	**Sensor_ID_highbit**	**8**	**0x50**	**RO**	**Sensor_ID**
0xf1	**Sensor_ID_low**	**8**	**0x04**	**RO**	**Sensor_ID**
0xf2	pad_vb_hiz_mode data_pad_io sync_pad_io	5	0x00	RW	[7:5] NA [4] pad_vb_hiz_mode [3] data_pad_io [2:0] sync_pad_io
0xf3	I2C_open_en	1	0x00	RW	[7:1] NA [0] I2C_open_en
0xf6	Up_down Pwd_dn	6	0x00	RW	[7:6] NA [5:4] up_dn 00: not pull 01: pull down 10: pull up 11: illegal [3:1] NA [0] PWD dn 0: pull down 1: not pull
0xf7	PLL_mode1	8	0x10	RW	[7] DVP mode [6:4] serial_clk_double [3] clk_double [2] Mode 32X 1: MCLK x32(MCLK 24MHz) 0: MCLK x48(MCLK 12MHz) [1] div2en 1: divider MCLK 1/2 0: not divider [0] PLL_en 1: enable 0: disable
0xf8	PLL_mode2	8	0x00	RW	[7] PLL dgdiv enable [6] NA [5:0] div MIPI:MCLK*(div+1)*4 DVP: MCLK*(div+1)/4

0xf9	Cm_mode	8	0x00	RW	[7] regf clk enable [6] 2pclk enable [5] pclk enable [4] hpclk enable [3] ISP all clock enable [2] serial clock enable [1] re_lock PLL [0] not use PLL
0xfa	clk_div_mode	8	0x00	RW	[7:4] +1 represent the frequency division number [3:0] represent the high level in one pulse after frequency division MCLK by Div duty 0x11 2 1:1 0x21 3 1:2 0x22 3 2:1 0x31 4 1:3 0x32 4 2:2 0x33 4 3:1 …
0xfb	i2c_device_id	8	0x6c	RW	[7:1] I2C device ID, can write once [0] NA
0xfc	analog_pwc	3	0x01	RW	[7:3] NA [2] vpix_en [1] NA [0] apwd
0xfe	Reset related	8	0x00	RW	[7] soft_reset [6] cm_reset [5] mipi_reset [4] CISCTL_restart_n, restart CISCTL, effective low [3] spi_reset [2:0] page_select

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x00	Reserved	8	0x10	RW	Reserved
P0:0x01	Exposure2[12:8]	5	0x00	RW	[7:5] NA [4:0] exposure[12:8], use line processing time as the unit.

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P0:0x02	Exposure2[7:0]	8	0x04	RW	Exposure[7:0]
P0:0x03	Exposure[12:8]	5	0x00	RW	[7:5] NA [4:0] exposure[12:8], use line processing time as the unit.
P0:0x04	Exposure[7:0]	8	0x10	RW	Exposure[7:0]
P0:0x05	HB[11:8]	4	0x00	RW	H Blanking
P0:0x06	HB[7:0]	8	0xa4	RW	
P0:0x07	VB[12:8]	5	0x00	RW	Vertical blanking, if current exposure < (Vb + window Height) , frame rate will be (Vb + window Height); otherwise frame rate will be determined by exposure
P0:0x08	VB[7:0]	8	0x04	RW	
P0:0x09	Row_start[10:8]	3	0x00	RW	Row Start
P0:0x0a	Row_start[7:0]	8	0x00	RW	
P0:0x0b	Col_start[11:8]	4	0x00	RW	Col start
P0:0x0c	Col_start[7:2]	8	0x00	RW	
P0:0x0d	win_height[10:8]	3	0x07	RW	[7:3] NA [2:0] Window height[10:8]
P0:0x0e	win_height[7:0]	8	0xa8	RW	Window height[7:0]
P0:0x0f	win_width[11:8]	4	0x02	RW	[7:4] NA [3:0] Window width[11:8]
P0:0x10	win_width[7:2]	8	0x8c	RW	window width[7:2]
P0:0x11	Sh_delay[9:8]	2	0x00	RW	Sh_delay[9:8]
P0:0x12	Sh_delay[7:0]	8	0x1e	RW	Sh_delay[7:0]
P0:0x13	Vs_st	8	0x11	RW	Vs_st
P0:0x14	Vs_et	8	0x02	RW	Vs_et
P0:0x15	Reserved	8	0x00	RW	Reserved
P0:0x16	Reserved	8	0xc1	RW	Reserved
P0:0x17	Mirror & Flip	8	0X00	RW	[7:2] Reserved [1] Flip [0] mirror
P0:0x18	Reserved	8	0x0a	RW	Reserved
P0:0x19	Reserved	8	0x05	RW	Reserved
P0:0x1a	Reserved	8	0x18	RW	Reserved
P0:0x1b	Reserved	8	0x44	RW	Reserved
P0:0x1c	Reserved	8	0x10	RW	Reserved
P0:0x1d	Reserved	8	0x00	RW	Reserved

P0:0x1e	Reserved	8	0x93	RW	Reserved
P0:0x1f	Reserved	8	0x18	RW	Reserved
P0:0x20	Reserved	8	0x00	RW	Reserved
P0:0x21	Reserved	8	0x40	RW	Reserved
P0:0x22	Reserved	8	0xb2	RW	Reserved
P0:0x23	Reserved	8	0x01	RW	Reserved
P0:0x24	Analog_PAD_drv	8	0x15	RW	[7:6] col test u/d [5:4] sync_drv 00: 4mA 01: 8mA 10: 12mA 11: 16mA [3:2] data_drv 00: 2mA 01: 4mA 10: 8mA 11: 10mA [1:0] pclk_drv 00:2mA 01:4mA 10:8mA 11:10mA
P0:0x25	Reserved	3	0x00	RW	Reserved
P0:0x26	Reserved	8	0x10	RW	Reserved
P0:0x27	Reserved	8	0x32	RW	Reserved
P0:0x28	Reserved	8	0xb7	RW	Reserved
P0:0x29	Reserved	4	0x0f	RW	Reserved
P0:0x2a	Reserved	8	0x06	RW	Reserved
P0:0x2b	Reserved	8	0x00	RW	Reserved
P0:0x2c	Reserved	7	0x58	RW	Reserved
P0:0x2d	Reserved	8	0x13	RW	Reserved
P0:0x2e	Reserved	8	0x04	RW	Reserved
P0:0x2f	Reserved	8	0x11	RW	Reserved
P0:0x30	Reserved	8	0x00	RW	Reserved
P0:0x31	Reserved	8	0x00	RW	Reserved
P0:0x32	Reserved	3	0x00	RW	Reserved
P0:0x33	Reserved	8	0x00	RW	Reserved
P0:0x34	Reserved	4	0x00	RW	Reserved
P0:0x35	Reserved	8	0x00	RW	Reserved
P0:0x36	Reserved	3	0x00	RW	Reserved
P0:0x37	Reserved	8	0x00	RW	Reserved

P0:0x38	Reserved	3	0x00	RW	Reserved
P0:0x39	Reserved	8	0x00	RW	Reserved
P0:0x3a	Reserved	2	0x00	RW	Reserved
P0:0x3b	Reserved	8	0x00	RW	Reserved
P0:0x3c	Reserved	3	0x00	RW	Reserved
P0:0x3d	Reserved	8	0x00	RW	Reserved
P0:0x3e	Reserved	2	0x00	RW	Reserved
P0:0x3f	Reserved	8	0x00	RW	Reserved

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x00	RW	[6] CTD_lane1 [5] CTD_lane0 [4] CTD_clk [2] PHY_lane1_en [1] PHY_lane0_en [0] PHY_clk_en
P3:0x02	DPHY_analog_mode2	8	0x00	RW	[6:4] lane0_diff [2:0] clk_diff
P3:0x03	DPHY_analog_mode3	8	0x00	RW	[7] LP low voltage enable [6] lane1_delay [5] lane0_delay [4] clk_delay [3] NA [2:0] lane1_diff
P3:0x04	FIFO_prog_full_level[7:0]	8	0xa0	RW	FIFO_prog_full_level[7:0]
P3:0x05	FIFO_prog_full_level[11:8]	4	0x00	RW	[7:4] NA [3:0] FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	8	0x00	RW	[7] MIPI_clk_Module [6] manual CSI2_up_mode [5] fix when output buf [4] FIFO_rst_mode [3] use_SRAM1_mode [2] NA [1] FIFO switch read [0] FIFO switch write
P3:0x10	buf_CSI2_mode	8	0x00	RW	[7] lane_en [6] four lane

					[5] ULP_mode [4] MIPI_en [3] bit10_switch [2] RAW8 [1] line_sync_mode [0] double_lane
P3:0x11	LDI_set	8	0x2b	RW	RAW10
P3:0x12	LWC_set[7:0]	8	0xd0	RW	Long packet WC set
P3:0x13	LWC_set[15:8]	8	0x07	RW	Long packet WC set
P3:0x14	SYNC_set	8	0xb8	RW	SYNC
P3:0x15	DPHY_mode	8	0x00	RW	[7] not split sram 672 [6:4] trigger mode [6] half [5] full [4] prog [3:2] switch msb mode [1:0] clklane_mode 1X: frames keep 01: clock lane sync with data lane 00: every frame stop clk lane mode
P3:0x16	LP_set	8	0x09	RW	[7:6] HIGH-Z [3:2] 1 [1:0] 0
P3:0x17	Ffio_gate_mode MIPI_wdiv_set	8	0x80	RW	[7] empty trigger [6] counter reach trigger [5] write gate mode [4] read gate mode [3:0] MIPI_wdiv_set, default 1/2
P3:0x18	DPHY_analog_mode4	8	0x00	RW	[6] CTD_lane3 [5] CTD_lane2 [4:3] NA [2] PHY_lane3_en [1] PHY_lane2_en [0] NA
P3:0x19	DPHY_analog_mode5	8	0x00	RW	[6:4] lane2_diff [3:0] NA
P3:0x1a	DPHY_analog_mode6	8	0x00	RW	[7] NA [6] lane3_delay [5] lane2_delay [4:3] NA [2:0] lane3_diff
P3:0x1b	Fifo2_prog_full	6	0x10	RW	Fifo2_prog_full_level

	_level				
P3:0x1c	Fifo2_push_prog_full_level	6	0x10	RW	Fifo2_push_prog_full_level
P3:0x1d	Sram_test_mode	4	0x02	RW	[7:4] NA [3] pause disable when div output buf [2] fifo2 frog full mode [1] sram gate [0] sram test
P3:0x20	T_init_set	8	0x80	RW	Timing of initial setting, more than 100 us
P3:0x21	T_LPX_set	8	0x10	RW	Timing of LP setting, more than 50ns
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	Timing of COCLK HS PREPARE setting, 38ns~95ns LP00
P3:0x23	T_CLK_zero_set	8	0x30	RW	Timing of COCLK HS zero setting, more than 300ns
P3:0x24	T_CLK_PRE_set	8	0x02	RW	Timing of COCLK HS PRE of Data setting, more than 8UI
P3:0x25	T_CLK_POST_set	8	0x10	RW	Timing of COCLK HS Post of Data setting, 60ns +52UI
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	Timing of COCLK tail setting, 60ns
P3:0x27	T_HS_exit_set	8	0x10	RW	Timing of HS exit setting, more than 100ns
P3:0x28	T_wakeup_set	8	0xa0	RW	Timing of wakeup setting, 1ms
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	Timing of data HS PREPARE setting, 45+4UI~85+5UI
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	Timing of data HS zero setting, 140ns
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	Timing of data HS trail setting, 60ns
P3:0x30	MIPI_test	2	0x00	RW	[7:2] NA [1:0] MIPI_test
P3:0x31	MIPI_test_data0	8	0x96	RW	MIPI_test_data0
P3:0x32	MIPI_test_data1	8	0x3a	RW	MIPI_test_data1
P3:0x33	MIPI_test_data2	8	0x87	RW	MIPI_test_data2
P3:0x34	MIPI_test_data3	8	0xb5	RW	MIPI_test_data3
P3:0x35	hsync_in_start_4_5_cnt_num	8	0x40	RW	hsync_in_start_4_5_cnt_num[7:0]

	[7:0]				
P3:0x36	hsync_in_start_4_5_cnt_num[9:8]	2	0x00	RW	[7:2] NA [1:0] hsync_in_start_4_5_cnt_num[9:8]
P3:0x3f	FIFO_error_log	2		RO	[7:2] NA [1] Fifo1_error_valid [0] Fifo_error_valid
P3:0x40	Output_buf_mode1	8	0x00	RW	[7:4] start mode [3] NA [2:1] delay half [0] NA
P3:0x41	Output_buf_mode2	8	0x00	RW	[7:6] NA [5:4] full mode for 4_5 [2] clk gating [1] pclk polarity [0] hsync polarity
P3:0x42	Buf_win_width[7:0]	8	0x40	RW	Buf_win_width[7:0]
P3:0x43	Buf_win_width[11:8]	4	0x06	RW	[7:4] NA [3:0] Buf_win_width[11:8]

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x80	Block_enable1	8	0x00	RW	[7] test mode for analog sim [6] NA [5] first_dn_en [4] first_dd_en [3] scaler_en [2:1] NA [0] output_buf_en
P0:0x81	Pad_test_valid[11:8] Pad_test_data[11:8]	8	0x00	RW	[7:4] Pad_test_valid[11:8] [3:0] Pad_test_data[11:8]
P0:0x82	Pad_test_valid[7:0]	8	0x00	RW	Pad_test_valid[7:0]
P0:0x83	Pad_test_data[7:0]	8	0x00	RW	Pad_test_data[7:0]
P0:0x84	Output_format	8	0x01	RW	[7:6] AD sequence

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					[5] auto DD en [4] auto DN en [3:2] scaler_DN_ratio [1:0] scaler_out_CFA
P0:0x85	Frame_start_num_thd	8	0x60	RW	Frame start delay frame thd
P0:0x86	Sync_mode	8	0x0f	RW	[7] data_delay_half [6] hsync_delay_half [5] aec valid for 2235 for FPGA [4] OUT gate en [3] NA [2] opclk polarity [1] hsync polarity [0] vsync polarity
P0:0x87	Scaler_x_ratio_a, Scaler_x_ratio_b	8	0x34	RW	[7:4] Scaler_x_ratio_a, [3:0] Scaler_x_ratio_b
P0:0x88	AEC_outdoor_th	8	0x20	RW	
P0:0x89	Bypass_mode	8	0x03	RW	[7] output 8bit [6] output 8bit round [5] dndd bypass [4] pregain bypass [3] is 8bit bypass [2] output dark sun [1:0] bypass which 8bit from 11bit, in is 8bit bypass mode
P0:0x8a	Reserved	8	0xb3	RW	Reserved
P0:0x8b	debug_mode1	8	0xad	RW	[7:6] BFF gate mode [5] BLK switch gain lasts one frame more [4] protect exp [3:2] pipe gate mode, 4 type check in CTL [1] not split sram [0] dark current update all allowed
P0:0x8c	debug_mode2	8	0x10	RW	[7] frame counter disable [6] GRAB round [5] exp2 1: 1/8 0: 1/4 [4] not smooth when exp change

					[3] test image when in VGA,UXGA 1: UXGA 0: VGA [2] input test image [1] LSC test image [0] OUT test image
P0:0x8d	Debug_mode3	8	0x01	RW	[7:4] test image fix value, [3] test image fix value mode [2] INBF_clock_gate [1] INBF_en [0] update gain mode
P0:0x8e	ACC_mode1	8	0x00	RW	[7] ACC_en [1] skip mode 1 is 1/16 [0] use buf parameter cal exp_gain
P0:0x8f	ACC_mode2	6	0x16	RW	[5] 4 FIR [4] 2 FIR [5:4]=00, no filter for Y [3:0] luma select
P0:0x90	Crop_win_mode	1	0x00	RW	[7:1] NA [0] Crop out Window mode
P0:0x91	Crop_win_y1[10:8]	3	0x00	RW	[7:3] NA [2:0] Crop _win_y1[10:8]
P0:0x92	Crop_win_y1[7:0]	8	0x00	RW	Crop _win_y1[7:0]
P0:0x93	Crop_win_x1[11:8]	4	0x00	RW	[7:4] NA [3:0] Crop _win_x1[11:8]
P0:0x94	Crop_win_x1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P0:0x95	out_win_height[10:8]	3	0x04	RW	[7:3] NA [2:0] Out window height[10:8]
P0:0x96	out_win_height[7:0]	8	0xb0	RW	Out window height[7:0]
P0:0x97	out_win_width[11:8]	4	0x06	RW	[7:4] NA [3:0] Out window width[11:8]
P0:0x98	out_win_width[7:0]	8	0x40	RW	Out window width[7:0]
P0:0xab	Y_avg_filter			RO	Y_avg_filter
P0:0xac	Luma_value[15:8]	8		RO	Luma_value[15:8]
P0:0xad	Luma_value[7:0]	8		RO	Luma_value[7:0]

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Blk_mode1	8	0x2b	RW	[7] not smooth [6:4] BLK_smooth_speed [3] BLK after GAIN [2] dark_current_mode [1] dark_current_en [0] offset_en
P0:0x41	BLK_mode2	8	0x80	RW	[7] sdark ndark in one frame [6] various th mode [5] blooming value limit en [4] blooming value limit [3] blooming number limie [2] FIR for 4 frame [1] enable dark current when all stat sdark [0] disable BLK DD
P0:0x42	BLK_limit_value	8	0xff	RW	When Dark data big than it, while get this to replace it for protect dark data. low align 11bits
P0:0x43	global_offset	8	0x00	RW	[7:0] global offset
P0:0x44	exp_rate_darkc	8	0x04	RW	low8 of 0.12; 4 means when exp=1024, dark_current_portion=4(align to low 7bits)
P0:0x46	Reserved	8	0xf2	RW	Reserved
P0:0x47	Reserved	8	0x10	RW	Reserved
P0:0x48	Reserved	8	0x10	RW	Reserved
P0:0x49	Reserved	8	0x00	RW	Reserved
P0:0x4a	Reserved	5	0x00	RW	Reserved
P0:0x4b	Reserved	8	0xff	RW	Reserved
P0:0x4c	dark_current_exp_rated_flop[10:8]	3		RO	[7:3] NA [2:0] dark_current_exp_rated_flop[10:8]
P0:0x4d	dark_current_exp_rated_flop[7:0]	8		RO	dark_current_exp_rated_flop[7:0]
P0:0x4e	BLK_select_row_bits[15:8]	8	0x00	RW	
P0:0x4f	BLK_select_row_bits[7:0]	8	0x3c	RW	

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P0:0x50 -0x5f	current_offset [7:0]	8		RO	current_ offset [7:0]
P0:0x60 -0x6f	current_dark_current[7:0]	8		RO	currentt_dark_current[7:0]
P0:0x70	offset_ratio_G1	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G1
P0:0x71	offset_ratio_R1	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_R1
P0:0x72	offset_ratio_B2	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_B2
P0:0x73	offset_ratio_G2	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G2
P0:0x74	Dark_current_ratio_G1	6	0x20	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_G1
P0:0x75	Dark_current_ratio_R1	6	0x20	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_R1
P0:0x76	Dark_current_ratio_B2	6	0x20	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_B2
P0:0x77	Dark_current_ratio_G2	6	0x20	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_G2
P0:0x78	manual_G1_odd_offset1	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x79	manual_G1_even_offset1	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x7a	manual_R1_odd_offset1	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x7b	manual_R1_even_offset1	6	0x00	RW	[7:6] NA [5:0]S5, aligned to lower 8 of 11 bits data
P0:0x7c	manual_B2_odd_offset1	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x7d	manual_B2_even_offset1	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x7e	manual_G2_odd_offset1	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x7f	manual_G2_even_offset1	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits

					data
P0:0xc8	manual_G1_odd_offset2	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0xc9	manual_G1_even_offset2	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0xca	manual_R1_odd_offset2	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0xcb	manual_R1_even_offset2	6	0x00	RW	[7:6] NA [5:0]S5, aligned to lower 8 of 11 bits data
P0:0xcc	manual_B2_odd_offset2	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0xcd	manual_B2_even_offset2	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0xce	manual_G2_odd_offset2	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0xcf	manual_G2_even_offset2	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0xd0 -0xdf	current _offset [10:8]	3		RO	[7:3] NA [2:0] current_ offset [10:8]
P0:0xe0 -0xef	current_dark_current[10:8]	3		RO	[7:3] NA [2:0]current__dark_current[10:8]

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0x9b	channel_gain1_G1_odd	8	0x80	RW	G1 odd Channel gain1
P0:0x9c	channel_gain1_G1_even	8	0x80	RW	G1 even Channel gain1
P0:0x9d	channel_gain1_R1_odd	8	0x80	RW	R1 odd Channel gain1
P0:0x9e	channel_gain1_R1_even	8	0x80	RW	R1 even Channel gain1
P0:0x9f	channel_gain1	8	0x80	RW	B2 odd channel gain1

	_B2_odd				
P0:0xa0	channel_gain1_B2_even	8	0x80	RW	B2 even channel gain1
P0:0xa1	channel_gain1_G2_odd	8	0x80	RW	G2 odd channel gain1
P0:0xa2	channel_gain1_G2_even	8	0x80	RW	G2 even channel gain1
P0:0xa3	channel_gain_G1_odd	8	0x80	RW	G1 odd Channel gain
P0:0xa4	channel_gain_G1_even	8	0x80	RW	G1 even Channel gain
P0:0xa5	channel_gain_R1_odd	8	0x80	RW	R1 odd Channel gain
P0:0xa6	channel_gain_R1_even	8	0x80	RW	R1 even Channel gain
P0:0xa7	channel_gain_B2_odd	8	0x80	RW	B2 odd channel gain
P0:0xa8	channel_gain_B2_even	8	0x80	RW	B2 even channel gain
P0:0xa9	channel_gain_G2_odd	8	0x80	RW	G2 odd channel gain
P0:0xaa	channel_gain_G2_even	8	0x80	RW	G2 even channel gain
P0:0xb0	Global_gain	8	0x40	RW	Global gain
P0:0xb1	Auto_pregain_sync[9:6]	4	0x01	RW	[7:4] NA [3:0] Auto_pregain_sync[9:6]
P0:0xb2	Auto_pregain[5:0]	8	0x00	RW	[7:2] Auto_pregain[5:0] [1:0] NA
P0:0xb3	AWB_R_gain	8	0x40	RW	AWB_R_gain
P0:0xb4	AWB_G_gain	8	0x40	RW	AWB_G_gain
P0:0xb5	AWB_B_gain	8	0x40	RW	AWB_B_gain
P0:0xb6	Again	3	0x00	RW	[2:0] Again
P0:0xb7	PRC_mode	8	0x11	RW	[7:2] RC_P [1] NA [0] PRC_mode_en

DNDD

Address	Name	Width	Default Value	R/W	Description
P2:0x83	Y_value_dd_th2	8	0xa0	RW	Y_value_dd_th2

P2:0x84	Y_value_dd_th3	8	0x90	RW	Y_value_dd_th3
P2:0x85	Y_value_dd_th4	8	0x80	RW	Y_value_dd_th4
P2:0x86	DN_mode_en	8	0x80	RW	DN_mode_en
P2:0x87	DN_mode_ratio	8	0x22	RW	DN_mode_ratio
P2:0x88	DN_auto_disable DNDD_denoise_mode DN_bilat_b_base	8	0x15	RW	[7] DN auto disable [6] DNDD_denoise_mode [5:0]Fixed bilateral b value
P2:0x89	DD_mode_en DN_C_weight	8	0x05	RW	[7:4] DD_mode_en [3:0] C_base
P2:0x8a	DD_dark_bright_TH	8	0x05	RW	DD_dark_bright_TH
P2:0x8b	DD_flat_TH	8	0x86	RW	dd th subtract
P2:0x8c	DD_limit DN_b_in_dark_inc_or_dec DD_ratio	8	0xf2	RW	[7:4] DD limit [3] NA [2] DN b in dark inc or dec [1:0] DD ratio
P2:0x8d	DN_b_in_dark_en DD_thr_en DD_mm_TH	8	0x8a	RW	[7] DN b in dark enable [6:4] en three defect [3:0] DD mm TH
P2:0x8e	DN_b_in_dark_th	8	0x0f	RW	DN bin dark th
P2:0x9d	DN_b_in_dark_slope	8	0x0f	RW	DN_b_in_dark_slope
P2:0x9e	noise_level_th1	8	0x03	RW	noise_level_th1
P2:0x9f	noise_level_th2	8	0x06	RW	noise_level_th2
P2:0xa0	noise_level_th3	8	0x0a	RW	noise_level_th3
P2:0xa1	noise_level_th4	8	0x10	RW	noise_level_th4

ASDE

Address	Name	Width	Default Value	R/W	Description
P2:0xaa	ASDE_low_luma_value_DD_th	8	0x20	RW	ASDE_low_luma_value_DD_th
P2:0xab	ASDE_low_luma_value_OT_th	8	0x20	RW	ASDE_low_luma_value_OT_th
P2:0xac	ASDE_DN_b_slope	8	0x66	RW	ASDE_DN_b_slope
P2:0xad	ASDE_DN_c_slope	8	0xaa	RW	ASDE_DN_c_slope
P2:0xb1	ASDE_DD_bright_th_slope ASDE_DD_limit_slope	8	0x5f	RW	[7:4] ASDE_DD_bright_th_slope [3:0] ASDE_DD_limit_slope
P2:0xb8	ASDE_DD_mm_th_slope	8	0x0a	RW	[3:0] ASDE_DD_mm_th_slope
P2:0xb3	b inc or dec	8	0x00	RW	b inc or dec

Revision History

Version V1.0 2013.07.29

- Document Release

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