

REV	Description	DATE	BY
A4A	Initial production Release.	11/19/2012	GC
A5	On the initial production release the processors were to be found incorrect as supplied by TI. Parts while marked AM3359 were actually AM3352. This revision uses the correct parts.	1/2/2013	GC
A5A	<ol style="list-style-type: none"> <li>Deleted R29-R44 from the LCD lines.</li> <li>Added 47pf capacitors C156-C173 to LCD data lines to ground.</li> <li>Changed schematic revision to A5A.</li> <li>Changed a few footprints after PCB update for above changes.</li> <li>Added access point for the battery function of the TPS65217C.</li> <li>Added Ferrite beads in series with LED power and 5V power rail of the USB host connector. Required to pass FCC/CE testing due to noise emissions on that pin.</li> <li>Added power button to enable sleep, wakeup, power down and power up features on the system.</li> <li>Added Modification to add 100K ohm resistor to ground to prevent crosstalk when serial cable is not plugged in.</li> </ol>	2/8/2013	GC
A5B	<ol style="list-style-type: none"> <li>Added 100K pulldown on J1 pin 4 to prevent crosstalk when serial cable is not connected into PCB layout.</li> <li>Changed the LED resistors to 4.75K to lower the brightness.</li> </ol>	5/21/2013	GC
A5C	<ol style="list-style-type: none"> <li>Changed R46, R47, R48 to 0 ohms.</li> <li>Changed R45 to 22 Ohms.</li> </ol> Change was made due to production failures on some boards due to differences in impedances.	6/12/2013	GC
A6	<ol style="list-style-type: none"> <li>Moved the enable for the VDD_3V3B regulator to VDD_3V3A rail. Change was made to reduce the delay between the ramp up of the 3.3V rails.</li> <li>Added a AND gate to the SYS_RESETh circuitry. There is a small chance that on power up the nRESETOUT signal on the processor may go high, causing the SYS_RESETh signal to go HI before it should. This change reenforces the reset with the PORZn reset signal.</li> <li>Added optional zero ohm resistor to tie GND_OSC0 to system ground.</li> </ol>	7/25/2013	GC
A6A	<ol style="list-style-type: none"> <li>Added optional zero ohm resistor to tie GND_OSC1 to system ground.</li> <li>Changed C106 to a 1uF capacitor.</li> <li>Changed C24 to a 2.2uF capacitor.</li> <li>Made R8 installed and R9 not installed.</li> </ol>	12/13/2013	GC
B	1.Changed the processor to the AM3358BZCZ100.	1/20/2014	GC
C	1.Increased the eMMC from 2GB to 4GB.	3/21/2014	GC

PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, UAB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	eMMC FLASH
9	10/100 ETHERNET
10	HDMI FRAMER
11	EXP CONN, uSD

NOTE: PCB Revision for this board is Rev B6

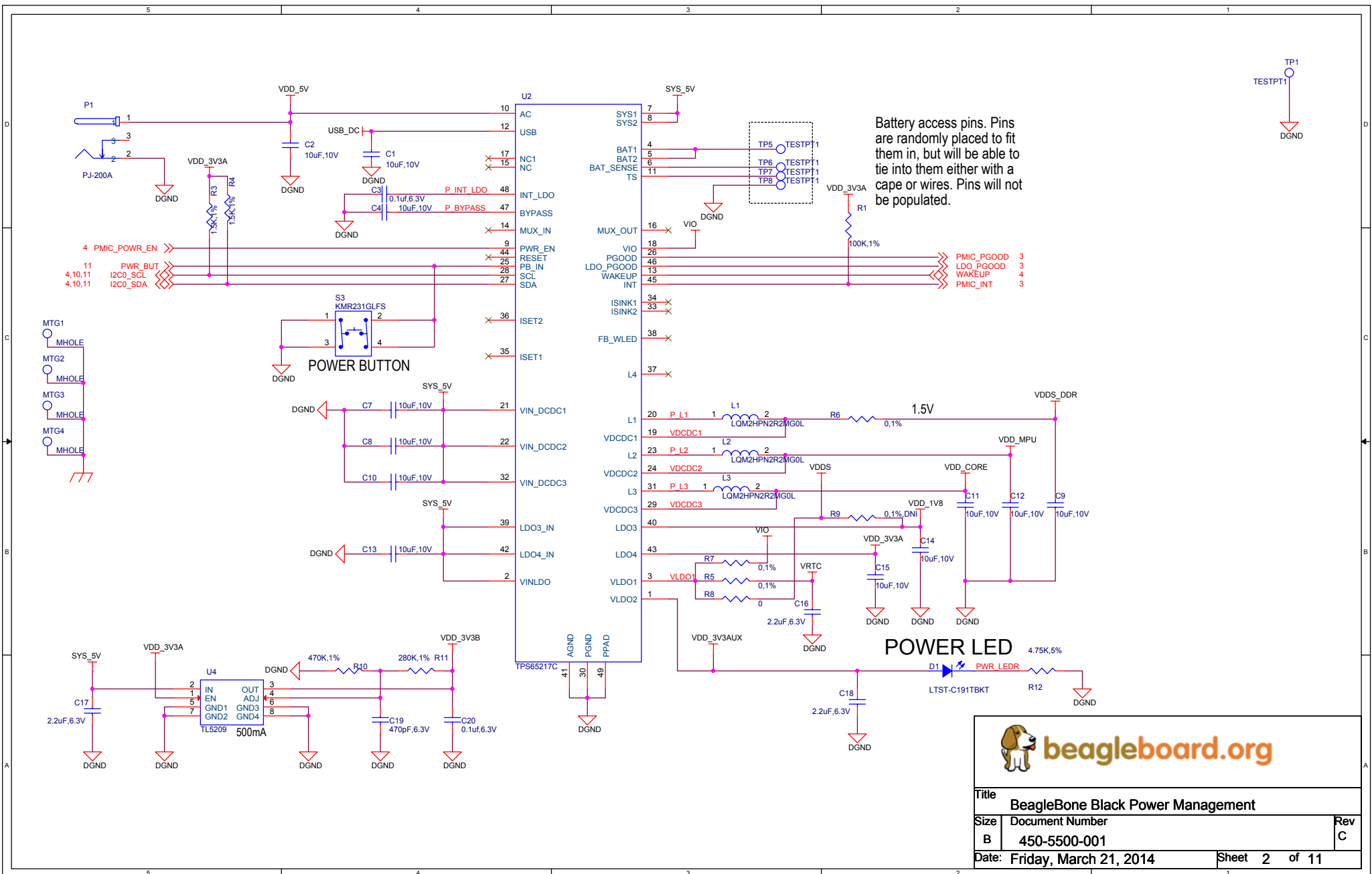
This schematic is **\*NOT SUPPORTED\*** and DOES NOT constitute a reference design. Only "community" support is allowed via resources at [BeagleBoard.org/discuss](http://BeagleBoard.org/discuss).

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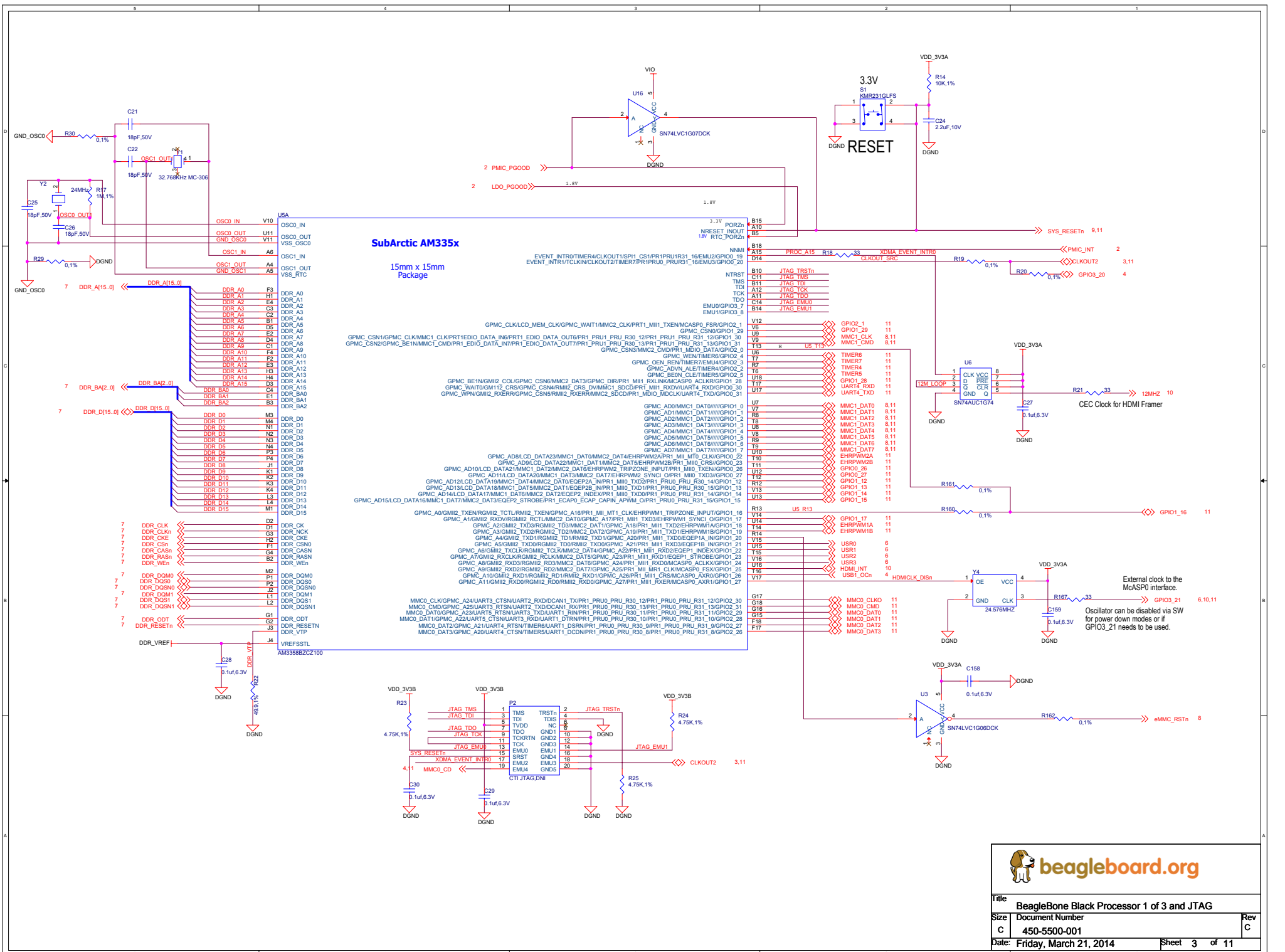


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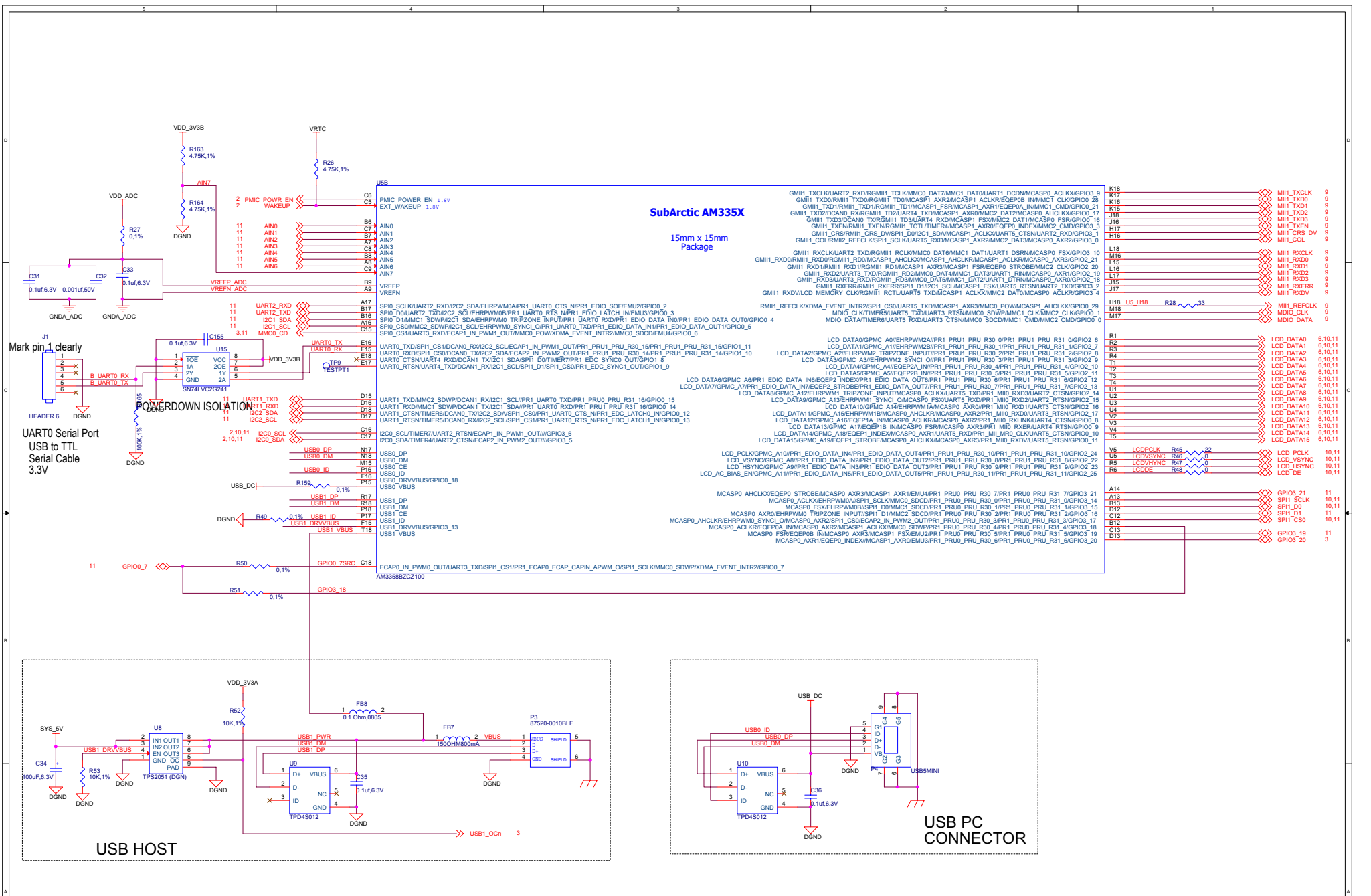
Title		BeagleBone Black Cover Page	
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B	450-5500-001	C	
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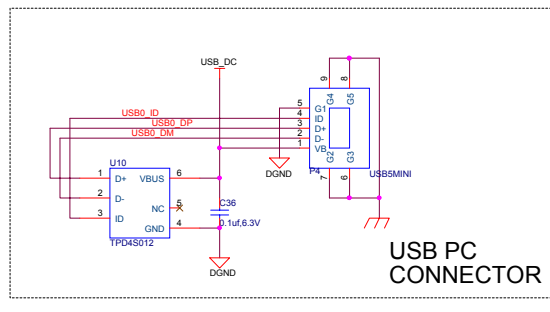
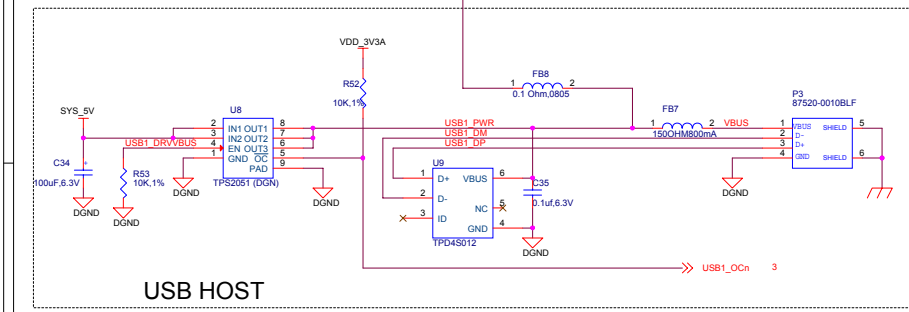
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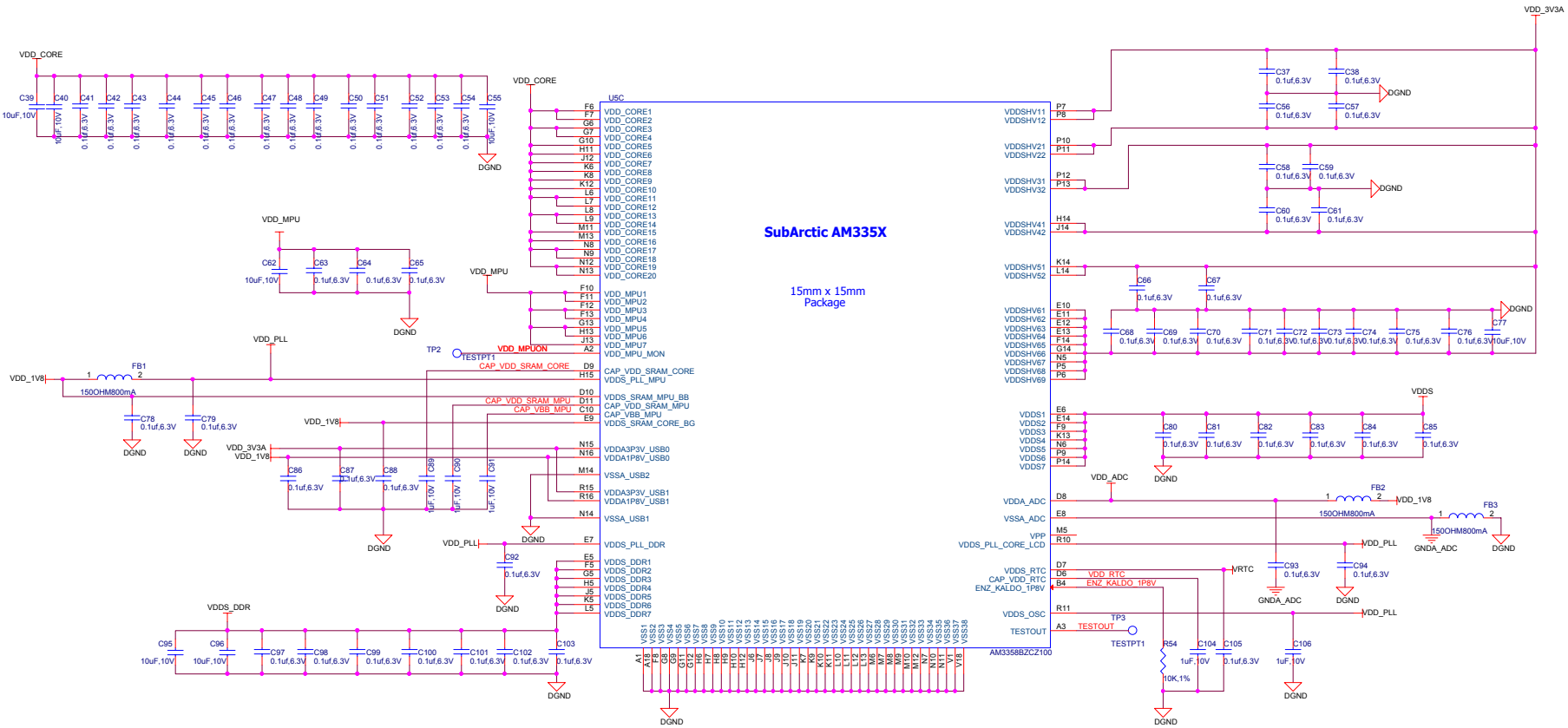


Title	BeagleBone Black Processor 1 of 3 and JTAG	
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Mark pin 1 clearly  
 UART0 Serial Port  
 USB to TTL  
 Serial Cable  
 3.3V





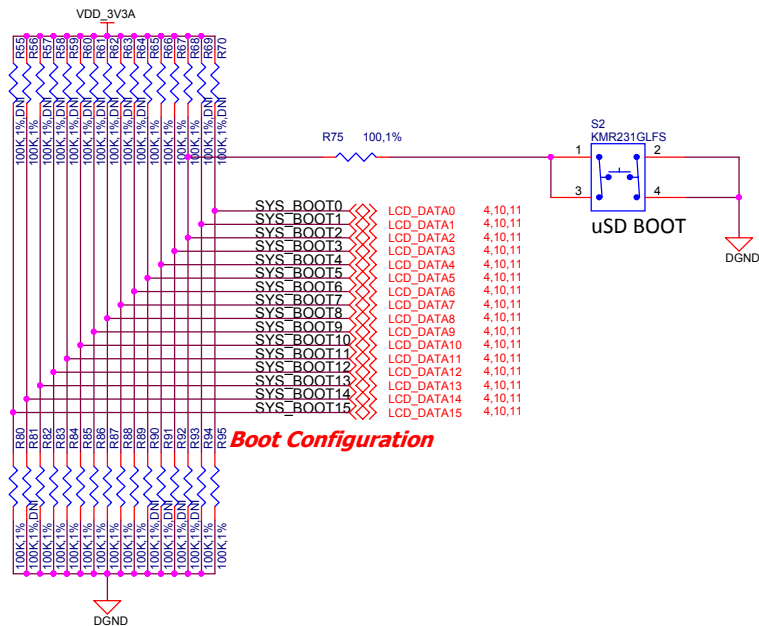
**SubArctic AM335X**

15mm x 15mm Package



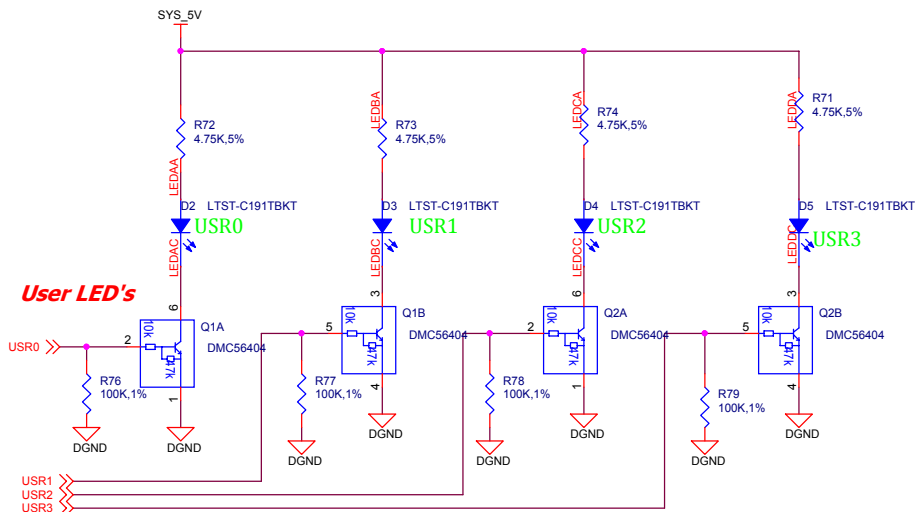
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Title	BeagleBone Black Process 3 of 3	
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SYS_BOOT0	LCD_DATA0	4,10,11
SYS_BOOT1	LCD_DATA1	4,10,11
SYS_BOOT2	LCD_DATA2	4,10,11
SYS_BOOT3	LCD_DATA3	4,10,11
SYS_BOOT4	LCD_DATA4	4,10,11
SYS_BOOT5	LCD_DATA5	4,10,11
SYS_BOOT6	LCD_DATA6	4,10,11
SYS_BOOT7	LCD_DATA7	4,10,11
SYS_BOOT8	LCD_DATA8	4,10,11
SYS_BOOT9	LCD_DATA9	4,10,11
SYS_BOOT10	LCD_DATA10	4,10,11
SYS_BOOT11	LCD_DATA11	4,10,11
SYS_BOOT12	LCD_DATA12	4,10,11
SYS_BOOT13	LCD_DATA13	4,10,11
SYS_BOOT14	LCD_DATA14	4,10,11
SYS_BOOT15	LCD_DATA15	4,10,11

**Boot Configuration**



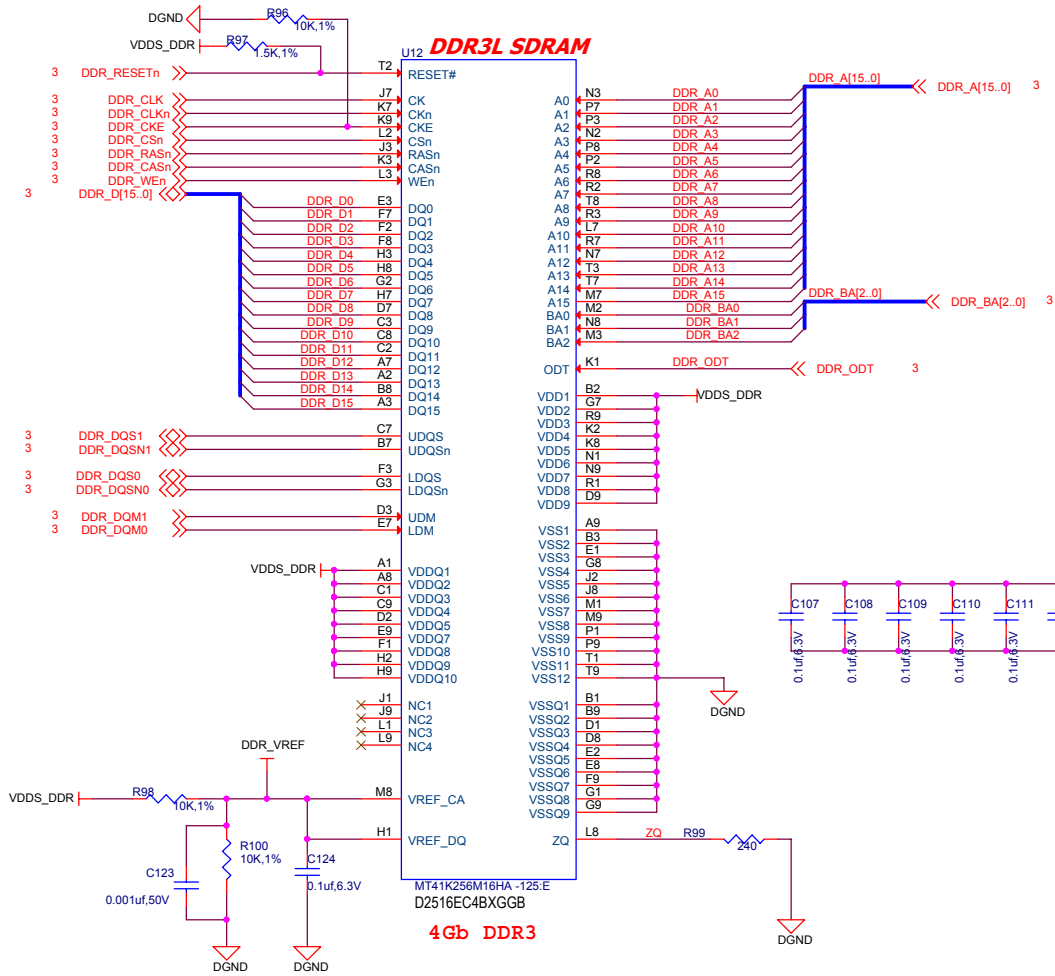
**User LED's**

SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5]	UART0

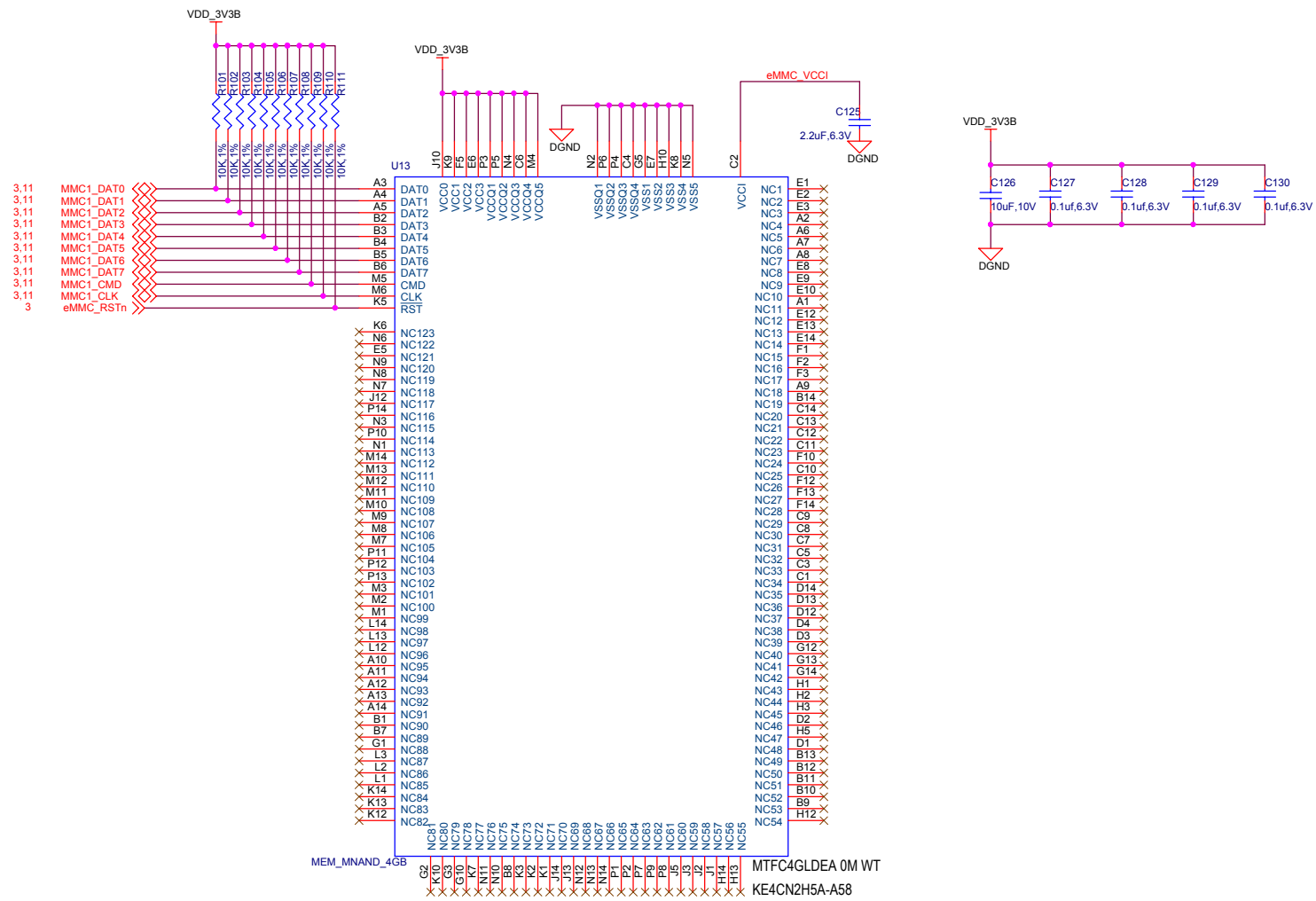


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Title		BeagleBone Black LED, Configuration, and Reset	
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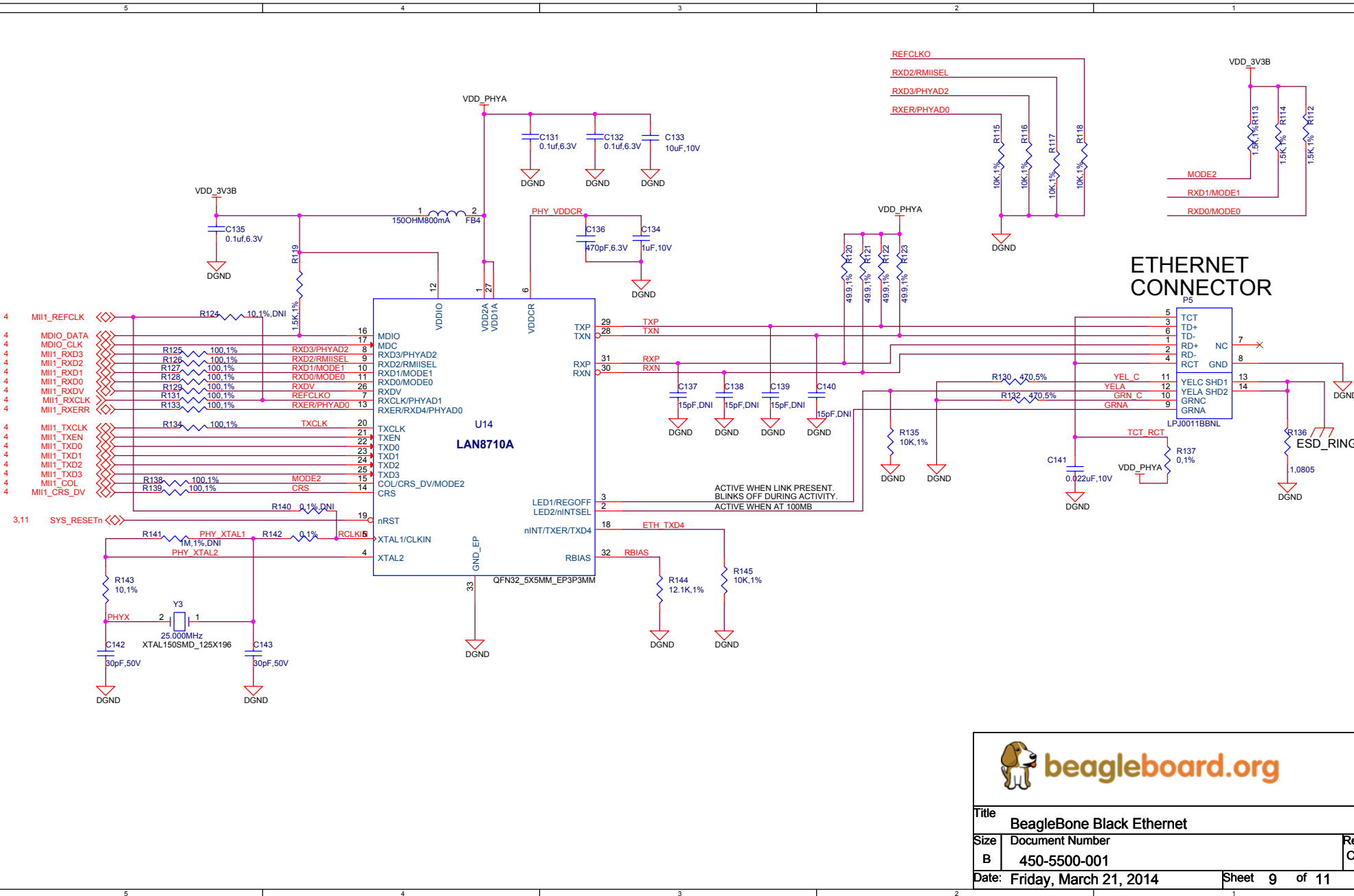


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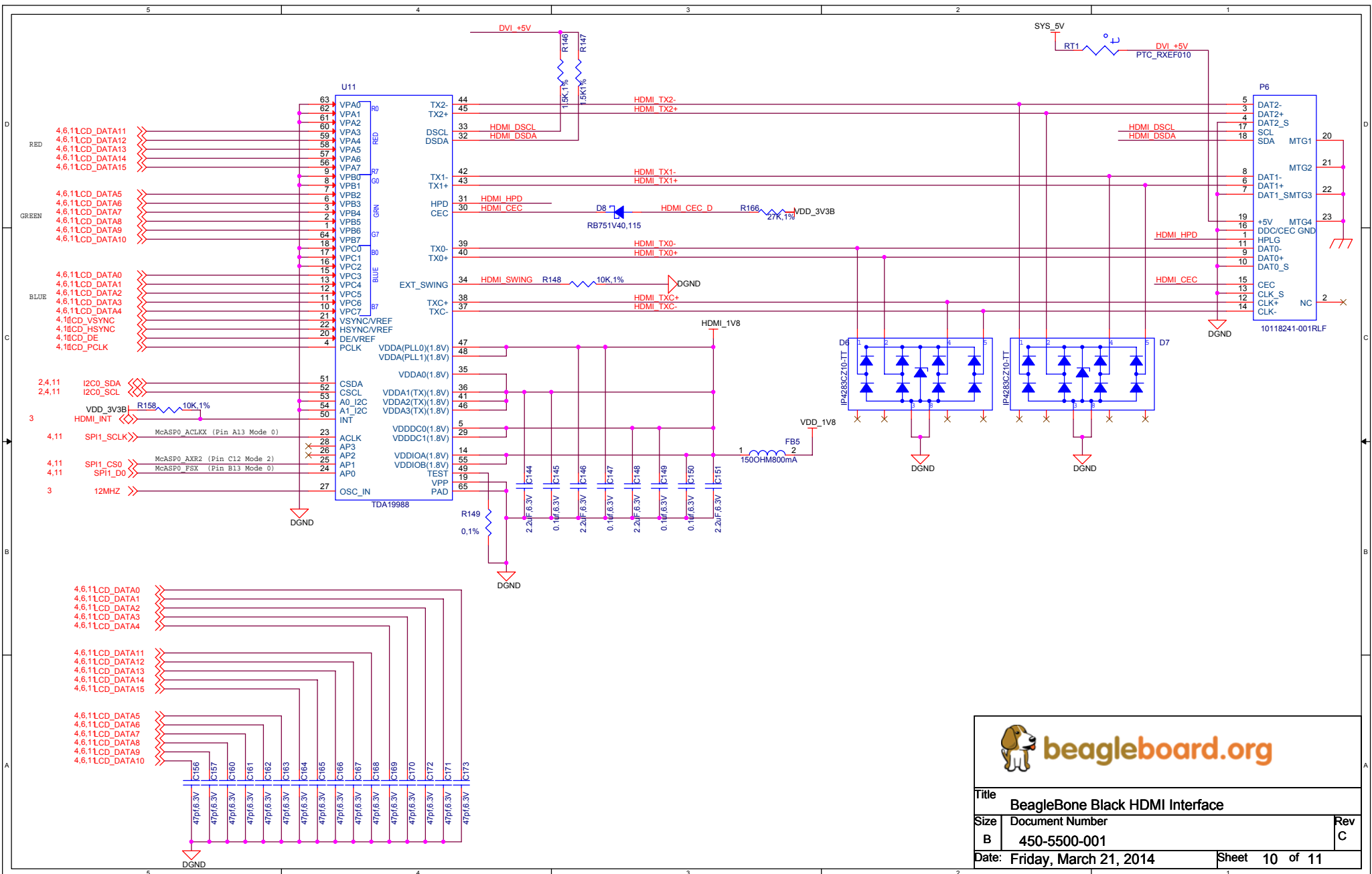


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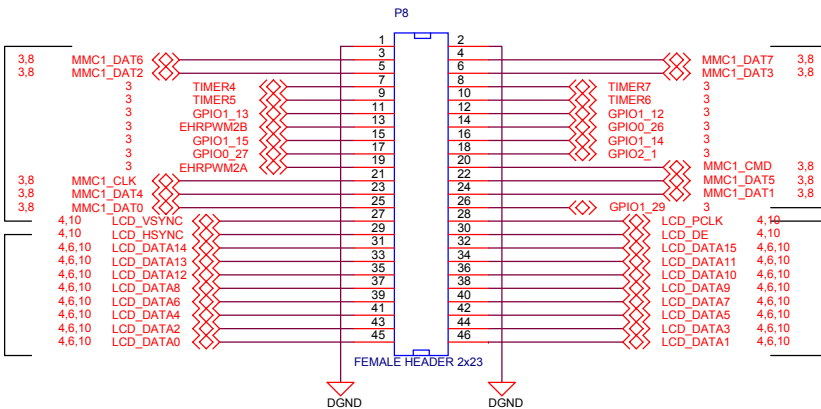


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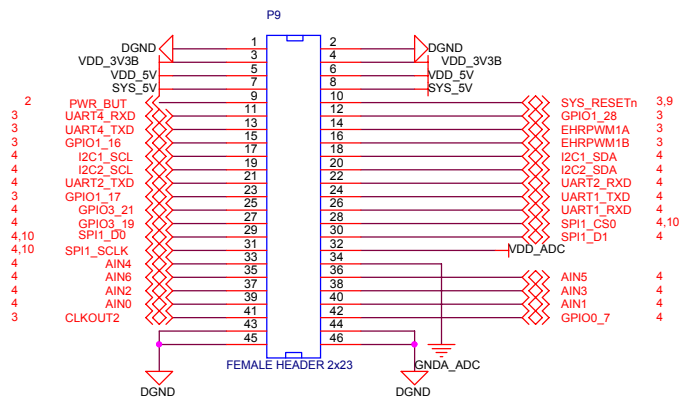
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BeagleBone Black HDMI Interface		
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CAUTION: USED ON BOARD

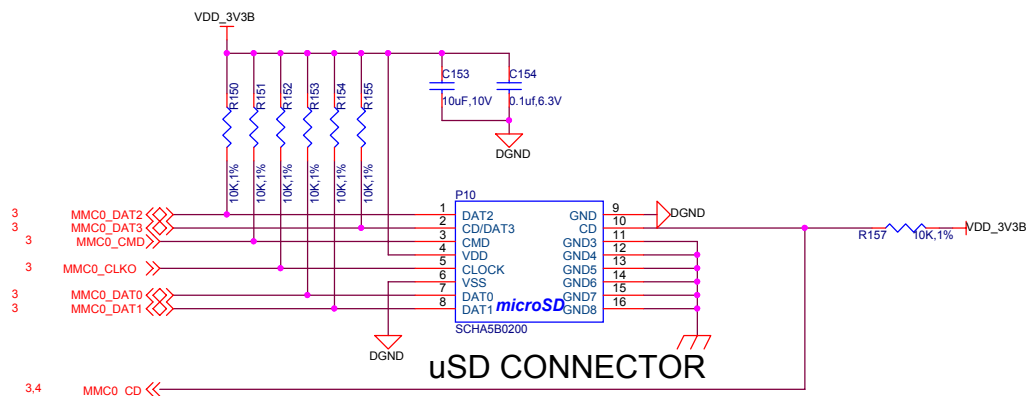


EXPANSION HEADER

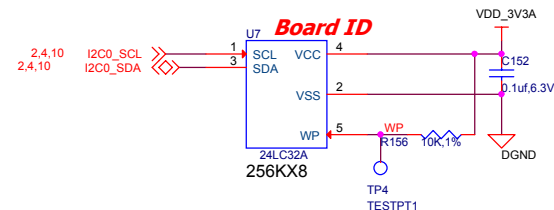
CAUTION: USED ON BOARD



EXPANSION HEADER



uSD CONNECTOR



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BeagleBone Black Expansion Headers, uSD and EEPROM		
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