DATA SHEET

(DOC No. HX8357-A01(T)-DS)

HX8357-A01(T)

320RGB x 480 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

Preliminary version 01 , October 2008

Himax Technologies, Inc.
http://www.himax.com.tw

List of Contents

List of Contents

List of Contents

List of Figures

List of Figures

List of Figures

List of Figures

List of Figures

List of Tables

List of Tables

1. General Description

This document describes HX8357-A is 320RGBx480 dots resolution driving controller. The HX8357-A is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 320RGBx480 dots at maximum.

The HX8357-A can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8357-A also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8357-A supports two interface groups: Command-Parameter interface group, Register-Content interface group. The interface groups are selected by the external pin IFSEL setting. This manual description focuses on Register-Content interface group. About the Command-Parameter interface group, please refer to the HX8357-A(N) datasheet for detail.

The HX8357-A is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

2. Features

2.1 Display

- Resolution:
  - 320(H) x RGB(H) x 240(V)
  - 320(H) x RGB(H) x 320(V)
  - 320(H) x RGB(H) x 400(V)
  - 320(H) x RGB(H) x 426(V)
  - 320(H) x RGB(H) x 432(V)
  - 320(H) x RGB(H) x 480(V)
- Display Color modes
  - Normal Display Mode On
    1. System Interface Circuit
       a. 4096(R(4),G(4),B(4)) colors
       b. 65,536(R(5),G(6),B(5)) colors
       c. 262,144(R(6),G(6),B(6)) colors
    2. RGB Interface Circuit
       a. 65,536(R(5),G(6),B(5)) colors
       b. 262,144(R(6),G(6),B(6)) colors
  - Idle Mode On
    - 8 (R(1),G(1),B(1)) colors.

2.2 Display module

- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)
- On module DC/DC converter
  - DDVDH = 4.6 to 6.0V (Source output voltage range)
  - VGH = +9.0 to +16.5V (Positive Gate output voltage range)
  - VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- Frame Memory area 320 (H) x 480 (V) x 18 bit

2.3 Display/control interface

- Display Interface types supported
  - System interface:
    a. 8-/9-/16-/18-bit parallel bus system interface
    b. 3-/4-wire serial bus system interface
  - RGB interface:
    a. 6-/16-/18-bit RGB interface
  - MDDI (Mobile Display Digital Interface) interface
- Color modes
  - 12 bit/pixel: R(4), G(4), B(4)
  - 16 bit/pixel: R(5), G(6), B(5)
  - 18 bit/pixel: R(6), G(6), B(6)

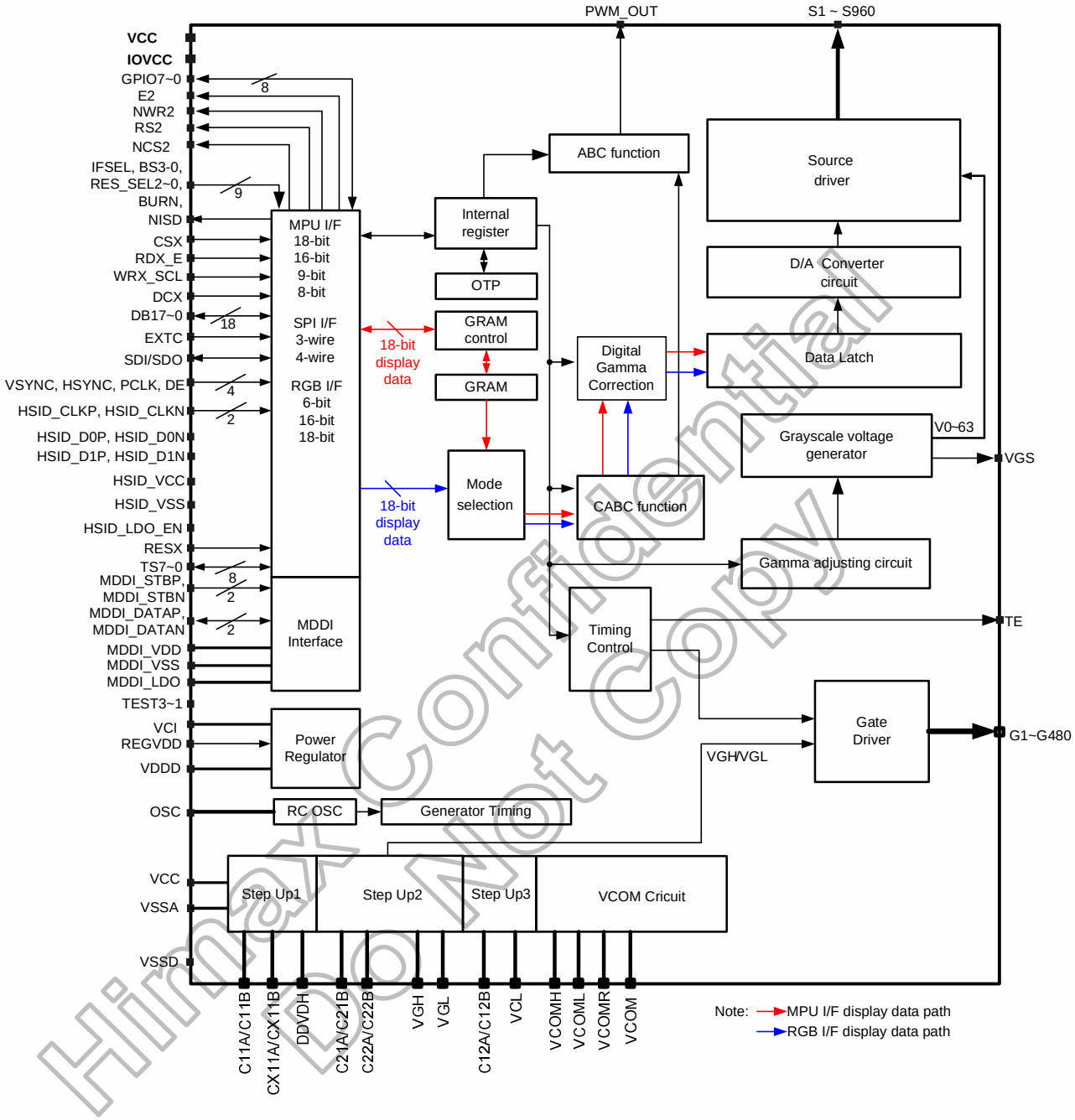
2.4 Display module

- Logic voltage (IOVCC): 1.65V ~ 3.3V
- Analog voltage (VCC): 2.3V ~ 3.3V
- Analog voltage (VCI): 2.3V ~ 3.3V
- MDDI power supply (MDDI_VDD): 2.3V ~ 3.3V
- OTP programming voltage (VPP): 7.5V ± 0.2

2.5 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -40 ~ +85 °C
- Proprietary multi phase driving for lower power consumption
- Support external VDDD for lower power consumption (such as 1.8 volts input)
- Support 1~7 Line inversion or Farme inversion
- Support Digital gamme correction
- Support Area scrolling
- Support Partial display mode
- Support normal black/normal white LCD
- Support wide view angle display
- Support burn-in mode for efficient test in module production
- On-chip OTP (One-time-programming) and MTP(three-time-programming for some register) non-volatile memory
- Support Content Adaptive Brightness Control(CABC) function
- Support Deep Standby mode or Standby mode

3. Block Diagram



4. Pin Description

4.1 Pin description

<table>
<tr><th colspan="5">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>BS3, BS2, BS1, BS0</td><td>I</td><td>4</td><td>VSSD/ IOVCC</td><td>System interface select.
<table>
<tr><th>BS3</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 16-bits Parallel type I</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 8-bits Parallel type I</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-bits Parallel type II</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 8-bits Parallel type II</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>3-wire Serial interface</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>-</td><td>4-wire Serial interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 18-bits Paralle type I</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 9-bits Parallel type I</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bits Parallel type II</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-bits Parallel type II</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>MDDI Interface</td></tr>
</table>
If not used, please fix this pin to IOVCC or VSSD level.</td></tr>
<tr><td>IFSEL</td><td>I</td><td>1</td><td>MPU</td><td>Interface format select pin
<table>
<tr><th>IFSEL</th><th>Interface Format Selection</th></tr>
<tr><td>1</td><td>Command-Parameter interface mode</td></tr>
<tr><td>0</td><td>Register-content interface mode</td></tr>
</table></td></tr>
<tr><td>EXTC</td><td>I</td><td>1</td><td>MPU</td><td>When operate in Register-content interface mode, the EXTC has to be connected to IOVCC or VSSD.</td></tr>
<tr><td>RES_SEL2~0</td><td>I</td><td>3</td><td>MPU</td><td>Panel Resolution select pin.
<table>
<tr><th>RES_SEL2</th><th>RES_SEL1</th><th>RES_SEL0</th><th>Panel Resolution</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>320RGB x 480 dot</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>320RGB x 432 dot</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>320RGB x 426 dot</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>320RGB x 400 dot</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>320RGB x 320 dot</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>320RGB x 240 dot</td></tr>
</table></td></tr>
<tr><td>CSX</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>RESX</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>WRX_DCX</td><td>I</td><td>1</td><td>MPU</td><td>I80 I/F mode: Serves as a write signal and write data at the low level.
M68 I/F mode: 0: Read/Write disable, 1: Read/Write enable.
When under 4-wire SPI interface, it servers as DCX(Data / Command Selection)
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>RDX_E</td><td>I</td><td>1</td><td>MPU</td><td>I80 I/F mode: Serves as a read signal and read data at the low level.
M68 I/F mode: Read/Write disable, 1: Read/Write enable.
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>DCX_SCL</td><td>I</td><td>1</td><td>MPU</td><td>Data / Command Selection pin
When under SPI interface, it servers as SCL (Serial Clock)
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>BURN</td><td>I</td><td>1</td><td>MPU</td><td>Free Running mode
If BURN=Hi, this can enable free running mode for burn in test.
The display data alternates between full black and full white independent of input data in free running mode. (weak pull low)</td></tr>
<tr><td>VS</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal for RGB I/F mode..
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>HS</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal for RGB I/F mode..
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>PCLK</td><td>I</td><td>1</td><td>MPU</td><td>Pixel clock signal for RGB I/F mode..
Must be connected to VSSD or IOVCC.</td></tr>
</table>

<table>
<tr><th colspan="5">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal for RGB I/F mode.
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>OSC</td><td>I</td><td>1</td><td>Oscillation Resistor</td><td>Oscillator input for test purpose.
If not used, please let it open or connected to VSSD.</td></tr>
<tr><td>VCOMR</td><td>I</td><td>1</td><td>Resistor or open</td><td>A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VREG1 and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8357-A.</td></tr>
<tr><td>VGS</td><td>I</td><td>1</td><td>VSSD or external resistor</td><td>Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used or connected to VSSA</td></tr>
<tr><td>RCM1, RCM0</td><td>I</td><td>2</td><td>MCU</td><td>RGB and System interface mode selection pin.
<table>
<tr><th>RCM1, RCM0</th><th>MCU and RGB Interface Mode Select</th></tr>
<tr><td>0x</td><td>System Interface (1)</td></tr>
<tr><td>10</td><td>RGB Interface (1) (VS+HS+DE)</td></tr>
<tr><td>11</td><td>RGB Interface (2) (VS+HS)</td></tr>
</table>
As internal RCM[1:0] bits are written, the external pin RCM[1:0] control is invalid, and RGB and System interface mode selection is controlled by internal RCM[1:0] bits.
If not used, please fix this pin to GND.</td></tr>
<tr><td>SRGB</td><td>I</td><td>1</td><td>MCU</td><td>RGB direction select H/W pin for Color filter default setting.
<table>
<tr><th>SRGB</th><th>RGB Filter Order for Color Filter Default Setting</th></tr>
<tr><td>0</td><td>S1, S2, S3 filter order = ’B’, ‘G’, ‘R’</td></tr>
<tr><td>1</td><td>S1, S2, S3 filter order = ’R’, ‘G’, ‘B’</td></tr>
</table>
As internal BRG bits are written, the external pin SRGB control is invalid and the color filter setting will be controlled by BRG bit.
If not used, please fix this pin to GND.</td></tr>
<tr><td>SMX</td><td>I</td><td>1</td><td>MCU</td><td>Module source output direction H/W select pin.
<table>
<tr><th>SMX</th><th>Module Source Output Direction</th></tr>
<tr><td>0</td><td>S960 -> S1</td></tr>
<tr><td>1</td><td>S1 -> S960</td></tr>
</table>
If not used, please fix this pin to GND.</td></tr>
<tr><td>SMY</td><td>I</td><td>1</td><td>MCU</td><td>Module Gate output direction H/W select pin.
<table>
<tr><th>SMY</th><th>Module Gate Output Direction</th></tr>
<tr><td>0</td><td>G1 -> G480</td></tr>
<tr><td>1</td><td>G480 -> G1</td></tr>
</table>
If not used, please fix this pin to GND.</td></tr>
</table>

<table>
<tr><th colspan="5">Output Part</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>S1~S960</td><td>O</td><td>960</td><td>LCD</td><td>Output voltages applied to the liquid crystal.</td></tr>
<tr><td>G1~G480</td><td>O</td><td>480</td><td>LCD</td><td>Gate driver output pins. These pins output VGH, VGL.
(If not used, should be open)
<table>
<tr><th rowspan="2">RES_SEL2~0</th><th rowspan="2">Panel Resolution</th><th colspan="2">Gate pin state</th></tr>
<tr><th>Connect to Panel</th><th>Open</th></tr>
<tr><td>111</td><td>320RGB x 480 dot</td><td>G1 ~ G480</td><td>-</td></tr>
<tr><td>110</td><td>320RGB x 432 dot</td><td>G1 ~ G432</td><td>G433 ~ G480</td></tr>
<tr><td>101</td><td>320RGB x 426 dot</td><td>G1 ~ G426</td><td>G427 ~ G480</td></tr>
<tr><td>100</td><td>320RGB x 400 dot</td><td>G1 ~ G400</td><td>G401 ~ G480</td></tr>
<tr><td>011</td><td>320RGB x 320 dot</td><td>G1 ~ G320</td><td>G321 ~ G480</td></tr>
<tr><td>010</td><td>320RGB x 240 dot</td><td>G1 ~ G240</td><td>G241 ~ G480</td></tr>
</table></td></tr>
<tr><td>VCOM</td><td>O</td><td>1</td><td>TFT common electrode</td><td>The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.</td></tr>
<tr><td>TE</td><td>O</td><td>1</td><td>MPU</td><td>Tearing effect output. If not used, please open this pin.</td></tr>
</table>

NISD	O	1	Open	Image Sticking Discharge signal. This pin is used for monitoring image sticking discharge phenomena. When the NISD goes low, the VGL, Source and VCOM would be discharged to VSSA. When the NISD goes high, the VGL, Source and VCOM are normal operation.
PWM_OUT	O	1	LED driver IC	Backlight On/Off control pin. If use ABC function, the pin can connect to external LED driver IC. The output voltage rage = VSSD~ IOVCC.
NWR2	O	1	Sub Panel	80-interface NWR signal output pin for Sub Panel. **If not use, let it open.**
E2	O	1	Sub Panel	68-interface Enable signal output pin for Sub Panel. **If not use, let it open.**
NCS2	O	1	Sub Panel	The signal is Chip select for Sub Panel. **If not use, let it open.**
RS2	O	1	Sub Panel	The signal is register index or register parameter select for Sub Panel. **If not use, let it open**

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B CX11A,CX11B	I/O	4	Step-up Capacitor	Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	I/O	4	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
DB17~0 (DBS17~0)	I/O	18	MPU	When Operates in MPU interface mode, it is used liked an 18-bit bi-directional data bus. About data bus format, please refer "Table 5. 1 Input Bus Format Selection of System Interface Circuit". When Operation in RGB interface mode, it is an 18-bit bus RGB data bus. About RGB data bus format, please refer "Table 5. 20 RGB interface Bus Width Set Table" If use MDDI interface, these pins are sub panel data bus (DBS17~DBS0). **Let unused pins to the open.**
SDA	I/O	1	MPU	Serial data input pin and output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal. **If not used, please open this pin.**
GPIO7~0	I/O	8	-	Standard Input/Output pin As for GPIO7 to 0 terminal, setting of an input and output direction is possible. **If not use, let it open.**

Hihg Speed Interface Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
HSID_CLKP, HSID_CLKN	-	2	High speed Host	High Speed Interface clock differential signal input pins. **If not used, please fix this pin to GND.**
HSID_D0P, HSID_D0N, HSID_D1P, HSID_D1N	-	4	High speed Host	High Speed Interface Data differential signal input pins. **If not used, please fix this pin to GND.**
HSID _VCC	P	1	Power supply or Capacitor	Power supply for the High Speed Interface analog power.HSID_VCC = 1.2V ~ 1.3V **If not used, please open this pin.**
HSID _VSS	P	1	Ground	High Speed Interface analog ground. HSID_VSS = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
HSID _LDO_EN	I	1	VSSD/ IOVCC	If HSID _LDO_EN = high, the internal HSID _VCC regulator will be turned on. If HSID _LDO_EN = low, the internal HSID _VCC regulator will be turned off, HSID _VCC should connect to external power supply, the voltage range 1.2V~1.3V. Must be connected to IOVCC or VSSD. **(weak pull low)**

MDDI Interface Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
MDDI_STBP, MDDI_STBN	-	2	MDDI Host	MDDI Strobe differential signal input pins. STBP pin for Strobe+, STBN pin for Strobe-. Connect to a terminal resistance (100Ω) between STBP and STBN. **If not used, please let it connected to VSSD.**
MDDI_DATAP MDDI_DATAN	-	2	MDDI Host	MDDI Data differential signal input pins. DATAP pin for Data+, DATAN pin for Data-. Connect to a terminal resistance (100Ω) between DATAP and DATAN. **If not used, please let it connected to VSSD.**
MDDI_VDD	P	1	Power Supply	MDDI I/O power supply pin, 2.3V~3.3V.
MDDI_VSS	P	1	Ground	MDDI I/O ground pin.
MDDI_LDO	O	1	Capacitor	MDDI regulator output pin. Connect to a stabilizing capacitor between MDDI_VSS and MDDI_LDO If not used, please open these pins.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	1	Power Supply	IO Pad and Digital power supply, 1.65V~3.3V
VCC	P	1	Power Supply	Analog power supply, 2.3V~3.3V
VCI	P	1	Power Supply	Analog power supply, 2.3V~3.3V
VPP	P	1	Power Supply	Power supply pin used in OTP program mode and operates at 7.5V ± 0.2. If not in OTP program mode, please let it open.
VSSD	P	1	Ground	Digital ground
VSSA	P	1	Ground	Analog ground
VDDD	O	1	Stabilizing Capacitor	Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor
REGVDD	I	1	VSSD/ IOVCC	If REGVDD = high, the internal VDDD regulator will be turned on. If REGVDD = low, the internal VDDD regulator will be turned off, VDDD should connect to external power supply, the voltage range 1.65~1.95V. Must be connected to IOVCC or VSSD. **(weak pull high)**
VREG1	P	1	Stabilizing Capacitor	Internal generated stable power for source driver unit.
VREF	O	1	Open	Internal reference voltage output pin, please open this pin.
VCOMH	P	1	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	P	1	Stabilizing capacitor	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.
VCL	P	1	Stabilizing capacitor	A negative voltage for VCOML circuit, VCL=-VCI
DDVDH	P	1	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH.
VGH	P	1	Stabilizing capacitor	An output from the step-up circuit2.or 4 ~ 6 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGH.
VGL	P	1	Stabilizing capacitor	An output from the step-up circuit2.or –3~ -5 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGL. Place a schottkey barrier diode between VSSD and VGL. Place a schottkey barrier diode (see “configuration of the power supply”).

Test Pin and Others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST3-1	I	3	GND	Test pin input (Internal pull low)
HSID_TEST3-1	O	3	Open	A test pin. Disconnect it.
TS7~0	O	8	Open	A test pin. Disconnect it.
VTEST	O	1	Open	A test pin. Disconnect it.
TVCOMHI	O	8	Open	A test pin. Disconnect it.
PADB0	I	2	Open	A test pin. Available for measuring the COG contact resistance. PADB0 are short-circuited within the chip.
PADB2	I	2	Open	A test pin. Available for measuring the COG contact resistance. PADB2 are short-circuited within the chip.

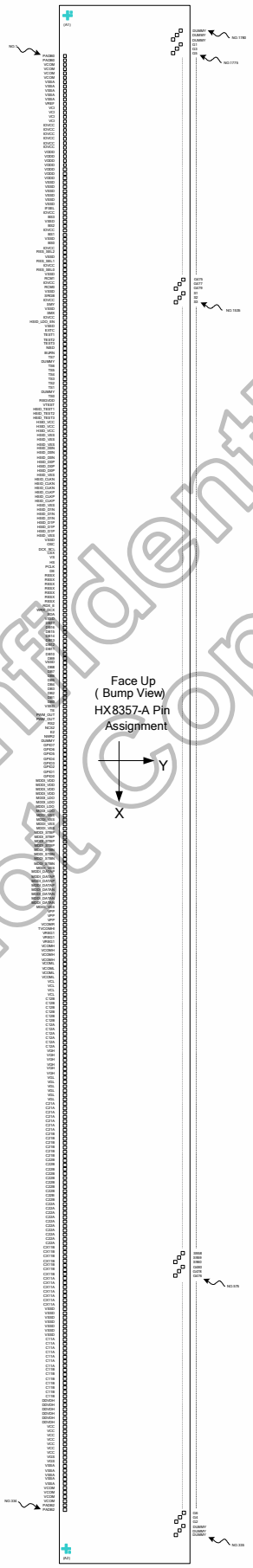
4.2 Pin assignment

- Chip Size: 21000 x 900 um
  Include seal ring: 15 x 2um
  Include scribe line: 40 x 2um
- Chip thickness: 300 um ± 25 um
- Pad Location: PAD Center
- Coordinate Origin: Chip Center
- Au Bump Size:

  1. 40 um x 56 um
     Input:
     No. 1 to No. 334

  2. 18 um x 80 um
     Staggered LCD output side
     No.335 to No.1780

- The chip size includes the core size seal ring size, and scribe line size
- Au bump pitch: Refer to Pad Coordinate
- Au bump height:15 um ± 3 um
- Numbers in the figure corresponds to pad coordinate numbers



4.3 PAD coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	PADB0	-10240	-365	61	IOVCC	-6640	-365	121	RESX	-3040	-365	181	MDDI_STBP	1060	-365
2	PADB0	-10180	-365	62	HSID_LDO_EN	-6580	-365	122	RESX	-2980	-365	182	MDDI_STBP	1120	-365
3	VCOM	-10120	-365	63	VSSD	-6520	-365	123	RESX	-2920	-365	183	MDDI_STBN	1180	-365
4	VCOM	-10060	-365	64	EXTC	-6460	-365	124	RESX	-2860	-365	184	MDDI_STBN	1240	-365
5	VCOM	-10000	-365	65	TEST1	-6400	-365	125	RESX	-2800	-365	185	MDDI_STBN	1300	-365
6	VCOM	-9940	-365	66	TEST2	-6340	-365	126	RESX	-2740	-365	186	MDDI_STBN	1360	-365
7	VSSA	-9880	-365	67	TEST3	-6280	-365	127	RDX_E	-2680	-365	187	MDDI_VSS	1420	-365
8	VSSA	-9820	-365	68	NISD	-6220	-365	128	WRX_DCX	-2620	-365	188	MDDI_DATAP	1480	-365
9	VSSA	-9760	-365	69	BURN	-6160	-365	129	SDA	-2560	-365	189	MDDI_DATAP	1540	-365
10	VSSA	-9700	-365	70	TS7	-6100	-365	130	VSSD	-2500	-365	190	MDDI_DATAP	1600	-365
11	VSSA	-9640	-365	71	DUMMY	-6040	-365	131	DB17	-2415	-365	191	MDDI_DATAP	1660	-365
12	VREF	-9580	-365	72	TS6	-5980	-365	132	DB16	-2330	-365	192	MDDI_DATAN	1720	-365
13	VCI	-9520	-365	73	TS5	-5920	-365	133	DB15	-2245	-365	193	MDDI_DATAN	1780	-365
14	VCI	-9460	-365	74	TS4	-5860	-365	134	DB14	-2160	-365	194	MDDI_DATAN	1840	-365
15	VCI	-9400	-365	75	TS3	-5800	-365	135	DB13	-2075	-365	195	MDDI_DATAN	1900	-365
16	VCI	-9340	-365	76	TS2	-5740	-365	136	DB12	-1990	-365	196	MDDI_VSS	1960	-365
17	IOVCC	-9280	-365	77	TS1	-5680	-365	137	DB11	-1905	-365	197	VPP	2020	-365
18	IOVCC	-9220	-365	78	DUMMY	-5620	-365	138	DB10	-1820	-365	198	VPP	2080	-365
19	IOVCC	-9160	-365	79	TS0	-5560	-365	139	DB9	-1735	-365	199	VPP	2140	-365
20	IOVCC	-9100	-365	80	REGVDD	-5500	-365	140	VSSD	-1650	-365	200	VCOMR	2200	-365
21	IOVCC	-9040	-365	81	VTEST	-5440	-365	141	DB8	-1565	-365	201	TVCOMHI	2260	-365
22	IOVCC	-8980	-365	82	HSID_TEST1	-5380	-365	142	DB7	-1480	-365	202	VREG1	2320	-365
23	VDDD	-8920	-365	83	HSID_TEST2	-5320	-365	143	DB6	-1395	-365	203	VREG1	2380	-365
24	VDDD	-8860	-365	84	HSID_TEST3	-5260	-365	144	DB5	-1310	-365	204	VREG1	2440	-365
25	VDDD	-8800	-365	85	HSID_VCC	-5200	-365	145	DB4	-1225	-365	205	VCOMH	2500	-365
26	VDDD	-8740	-365	86	HSID_VCC	-5140	-365	146	DB3	-1140	-365	206	VCOMH	2560	-365
27	VDDD	-8680	-365	87	HSID_VCC	-5080	-365	147	DB2	-1055	-365	207	VCOMH	2620	-365
28	VDDD	-8620	-365	88	HSID_VSS	-5020	-365	148	DB1	-970	-365	208	VCOMH	2680	-365
29	VDDD	-8560	-365	89	HSID_VSS	-4960	-365	149	DB0	-885	-365	209	VCOML	2740	-365
30	VSSD	-8500	-365	90	HSID_VSS	-4900	-365	150	VSSD	-800	-365	210	VCOML	2800	-365
31	VSSD	-8440	-365	91	HSID_D0N	-4840	-365	151	TE	-740	-365	211	VCOML	2860	-365
32	VSSD	-8380	-365	92	HSID_D0N	-4780	-365	152	PWM_OUT	-680	-365	212	VCOML	2920	-365
33	VSSD	-8320	-365	93	HSID_D0N	-4720	-365	153	PWM_OUT	-620	-365	213	VCL	2980	-365
34	VSSD	-8260	-365	94	HSID_D0P	-4660	-365	154	RS2	-560	-365	214	VCL	3040	-365
35	VSSD	-8200	-365	95	HSID_D0P	-4600	-365	155	NCS2	-500	-365	215	VCL	3100	-365
36	IFSEL	-8140	-365	96	HSID_D0P	-4540	-365	156	E2	-440	-365	216	VCL	3160	-365
37	IOVCC	-8080	-365	97	HSID_VSS	-4480	-365	157	NWR2	-380	-365	217	C12B	3220	-365
38	BS3	-8020	-365	98	HSID_CLKN	-4420	-365	158	DUMMY	-320	-365	218	C12B	3280	-365
39	VSSD	-7960	-365	99	HSID_CLKN	-4360	-365	159	GPIO7	-260	-365	219	C12B	3340	-365
40	BS2	-7900	-365	100	HSID_CLKN	-4300	-365	160	GPIO6	-200	-365	220	C12B	3400	-365
41	IOVCC	-7840	-365	101	HSID_CLKP	-4240	-365	161	GPIO5	-140	-365	221	C12B	3460	-365
42	BS1	-7780	-365	102	HSID_CLKP	-4180	-365	162	GPIO4	-80	-365	222	C12B	3520	-365
43	VSSD	-7720	-365	103	HSID_CLKP	-4120	-365	163	GPIO3	-20	-365	223	C12A	3580	-365
44	BS0	-7660	-365	104	HSID_VSS	-4060	-365	164	GPIO2	40	-365	224	C12A	3640	-365
45	IOVCC	-7600	-365	105	HSID_D1N	-4000	-365	165	GPIO1	100	-365	225	C12A	3700	-365
46	RES_SEL2	-7540	-365	106	HSID_D1N	-3940	-365	166	GPIO0	160	-365	226	C12A	3760	-365
47	VSSD	-7480	-365	107	HSID_D1N	-3880	-365	167	MDDI_VDD	220	-365	227	C12A	3820	-365
48	RES_SEL1	-7420	-365	108	HSID_D1P	-3820	-365	168	MDDI_VDD	280	-365	228	C12A	3880	-365
49	IOVCC	-7360	-365	109	HSID_D1P	-3760	-365	169	MDDI_VDD	340	-365	229	VGH	3940	-365
50	RES_SEL0	-7300	-365	110	HSID_D1P	-3700	-365	170	MDDI_VDD	400	-365	230	VGH	4000	-365
51	VSSD	-7240	-365	111	HSID_VSS	-3640	-365	171	MDDI_LDO	460	-365	231	VGH	4060	-365
52	RCM1	-7180	-365	112	VSSD	-3580	-365	172	MDDI_LDO	520	-365	232	VGH	4120	-365
53	IOVCC	-7120	-365	113	OSC	-3520	-365	173	MDDI_LDO	580	-365	233	VGH	4180	-365
54	RCM0	-7060	-365	114	DCX_SCL	-3460	-365	174	MDDI_LDO	640	-365	234	VGH	4240	-365
55	VSSD	-7000	-365	115	CSX	-3400	-365	175	MDDI_VSS	700	-365	235	VGL	4300	-365
56	SRGB	-6940	-365	116	VS	-3340	-365	176	MDDI_VSS	760	-365	236	VGL	4360	-365
57	IOVCC	-6880	-365	117	HS	-3280	-365	177	MDDI_VSS	820	-365	237	VGL	4420	-365
58	SMY	-6820	-365	118	PCLK	-3220	-365	178	MDDI_VSS	880	-365	238	VGL	4480	-365
59	VSSD	-6760	-365	119	DE	-3160	-365	179	MDDI_STBP	940	-365	239	VGL	4540	-365
60	SMX	-6700	-365	120	RESX	-3100	-365	180	MDDI_STBP	1000	-365	240	VGL	4600	-365

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
241	C21A	4660	-365	301	C11A	8260	-365	361	G48	9959	353	421	G168	9119	353
242	C21A	4720	-365	302	C11B	8320	-365	362	G50	9945	161	422	G170	9105	161
243	C21A	4780	-365	303	C11B	8380	-365	363	G52	9931	257	423	G172	9091	257
244	C21A	4840	-365	304	C11B	8440	-365	364	G54	9917	353	424	G174	9077	353
245	C21A	4900	-365	305	C11B	8500	-365	365	G56	9903	161	425	G176	9063	161
246	C21A	4960	-365	306	C11B	8560	-365	366	G58	9889	257	426	G178	9049	257
247	C21A	5020	-365	307	C11B	8620	-365	367	G60	9875	353	427	G180	9035	353
248	C21B	5080	-365	308	C11B	8680	-365	368	G62	9861	161	428	G182	9021	161
249	C21B	5140	-365	309	DDVDH	8740	-365	369	G64	9847	257	429	G184	9007	257
250	C21B	5200	-365	310	DDVDH	8800	-365	370	G66	9833	353	430	G186	8993	353
251	C21B	5260	-365	311	DDVDH	8860	-365	371	G68	9819	161	431	G188	8979	161
252	C21B	5320	-365	312	DDVDH	8920	-365	372	G70	9805	257	432	G190	8965	257
253	C21B	5380	-365	313	DDVDH	8980	-365	373	G72	9791	353	433	G192	8951	353
254	C22B	5440	-365	314	DDVDH	9040	-365	374	G74	9777	161	434	G194	8937	161
255	C22B	5500	-365	315	VCC	9100	-365	375	G76	9763	257	435	G196	8923	257
256	C22B	5560	-365	316	VCC	9160	-365	376	G78	9749	353	436	G198	8909	353
257	C22B	5620	-365	317	VCC	9220	-365	377	G80	9735	161	437	G200	8895	161
258	C22B	5680	-365	318	VCC	9280	-365	378	G82	9721	257	438	G202	8881	257
259	C22B	5740	-365	319	VCC	9340	-365	379	G84	9707	353	439	G204	8867	353
260	C22B	5800	-365	320	VCC	9400	-365	380	G86	9693	161	440	G206	8853	161
261	C22B	5860	-365	321	VCC	9460	-365	381	G88	9679	257	441	G208	8839	257
262	C22B	5920	-365	322	VGS	9520	-365	382	G90	9665	353	442	G210	8825	353
263	C22B	5980	-365	323	VGS	9580	-365	383	G92	9651	161	443	G212	8811	161
264	C22A	6040	-365	324	VSSA	9640	-365	384	G94	9637	257	444	G214	8797	257
265	C22A	6100	-365	325	VSSA	9700	-365	385	G96	9623	353	445	G216	8783	353
266	C22A	6160	-365	326	VSSA	9760	-365	386	G98	9609	161	446	G218	8769	161
267	C22A	6220	-365	327	VSSA	9820	-365	387	G100	9595	257	447	G220	8755	257
268	C22A	6280	-365	328	VSSA	9880	-365	388	G102	9581	353	448	G222	8741	353
269	C22A	6340	-365	329	VCOM	9940	-365	389	G104	9567	161	449	G224	8727	161
270	C22A	6400	-365	330	VCOM	10000	-365	390	G106	9553	257	450	G226	8713	257
271	C22A	6460	-365	331	VCOM	10060	-365	391	G108	9539	353	451	G228	8699	353
272	C22A	6520	-365	332	VCOM	10120	-365	392	G110	9525	161	452	G230	8685	161
273	C22A	6580	-365	333	PADB2	10180	-365	393	G112	9511	257	453	G232	8671	257
274	CX11B	6640	-365	334	PADB2	10240	-365	394	G114	9497	353	454	G234	8657	353
275	CX11B	6700	-365	335	DUMMY	10323	161	395	G116	9483	161	455	G236	8643	161
276	CX11B	6760	-365	336	DUMMY	10309	257	396	G118	9469	257	456	G238	8629	257
277	CX11B	6820	-365	337	DUMMY	10295	353	397	G120	9455	353	457	G240	8615	353
278	CX11B	6880	-365	338	G2	10281	161	398	G122	9441	161	458	G242	8601	161
279	CX11B	6940	-365	339	G4	10267	257	399	G124	9427	257	459	G244	8587	257
280	CX11B	7000	-365	340	G6	10253	353	400	G126	9413	353	460	G246	8573	353
281	CX11A	7060	-365	341	G8	10239	161	401	G128	9399	161	461	G248	8559	161
282	CX11A	7120	-365	342	G10	10225	257	402	G130	9385	257	462	G250	8545	257
283	CX11A	7180	-365	343	G12	10211	353	403	G132	9371	353	463	G252	8531	353
284	CX11A	7240	-365	344	G14	10197	161	404	G134	9357	161	464	G254	8517	161
285	CX11A	7300	-365	345	G16	10183	257	405	G136	9343	257	465	G256	8503	257
286	CX11A	7360	-365	346	G18	10169	353	406	G138	9329	353	466	G258	8489	353
287	CX11A	7420	-365	347	G20	10155	161	407	G140	9315	161	467	G260	8475	161
288	VSSD	7480	-365	348	G22	10141	257	408	G142	9301	257	468	G262	8461	257
289	VSSD	7540	-365	349	G24	10127	353	409	G144	9287	353	469	G264	8447	353
290	VSSD	7600	-365	350	G26	10113	161	410	G146	9273	161	470	G266	8433	161
291	VSSD	7660	-365	351	G28	10099	257	411	G148	9259	257	471	G268	8419	257
292	VSSD	7720	-365	352	G30	10085	353	412	G150	9245	353	472	G270	8405	353
293	VSSD	7780	-365	353	G32	10071	161	413	G152	9231	161	473	G272	8391	161
294	VSSD	7840	-365	354	G34	10057	257	414	G154	9217	257	474	G274	8377	257
295	C11A	7900	-365	355	G36	10043	353	415	G156	9203	353	475	G276	8363	353
296	C11A	7960	-365	356	G38	10029	161	416	G158	9189	161	476	G278	8349	161
297	C11A	8020	-365	357	G40	10015	257	417	G160	9175	257	477	G280	8335	257
298	C11A	8080	-365	358	G42	10001	353	418	G162	9161	353	478	G282	8321	353
299	C11A	8140	-365	359	G44	9987	161	419	G164	9147	161	479	G284	8307	161
300	C11A	8200	-365	360	G46	9973	257	420	G166	9133	257	480	G286	8293	257

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
481	G288	8279	353	541	G408	7439	353	601	S937	6557	353	661	S877	5717	353
482	G290	8265	161	542	G410	7425	161	602	S936	6543	161	662	S876	5703	161
483	G292	8251	257	543	G412	7411	257	603	S935	6529	257	663	S875	5689	257
484	G294	8237	353	544	G414	7397	353	604	S934	6515	353	664	S874	5675	353
485	G296	8223	161	545	G416	7383	161	605	S933	6501	161	665	S873	5661	161
486	G298	8209	257	546	G418	7369	257	606	S932	6487	257	666	S872	5647	257
487	G300	8195	353	547	G420	7355	353	607	S931	6473	353	667	S871	5633	353
488	G302	8181	161	548	G422	7341	161	608	S930	6459	161	668	S870	5619	161
489	G304	8167	257	549	G424	7327	257	609	S929	6445	257	669	S869	5605	257
490	G306	8153	353	550	G426	7313	353	610	S928	6431	353	670	S868	5591	353
491	G308	8139	161	551	G428	7299	161	611	S927	6417	161	671	S867	5577	161
492	G310	8125	257	552	G430	7285	257	612	S926	6403	257	672	S866	5563	257
493	G312	8111	353	553	G432	7271	353	613	S925	6389	353	673	S865	5549	353
494	G314	8097	161	554	G434	7257	161	614	S924	6375	161	674	S864	5535	161
495	G316	8083	257	555	G436	7243	257	615	S923	6361	257	675	S863	5521	257
496	G318	8069	353	556	G438	7229	353	616	S922	6347	353	676	S862	5507	353
497	G320	8055	161	557	G440	7215	161	617	S921	6333	161	677	S861	5493	161
498	G322	8041	257	558	G442	7201	257	618	S920	6319	257	678	S860	5479	257
499	G324	8027	353	559	G444	7187	353	619	S919	6305	353	679	S859	5465	353
500	G326	8013	161	560	G446	7173	161	620	S918	6291	161	680	S858	5451	161
501	G328	7999	257	561	G448	7159	257	621	S917	6277	257	681	S857	5437	257
502	G330	7985	353	562	G450	7145	353	622	S916	6263	353	682	S856	5423	353
503	G332	7971	161	563	G452	7131	161	623	S915	6249	161	683	S855	5409	161
504	G334	7957	257	564	G454	7117	257	624	S914	6235	257	684	S854	5395	257
505	G336	7943	353	565	G456	7103	353	625	S913	6221	353	685	S853	5381	353
506	G338	7929	161	566	G458	7089	161	626	S912	6207	161	686	S852	5367	161
507	G340	7915	257	567	G460	7075	257	627	S911	6193	257	687	S851	5353	257
508	G342	7901	353	568	G462	7061	353	628	S910	6179	353	688	S850	5339	353
509	G344	7887	161	569	G464	7047	161	629	S909	6165	161	689	S849	5325	161
510	G346	7873	257	570	G466	7033	257	630	S908	6151	257	690	S848	5311	257
511	G348	7859	353	571	G468	7019	353	631	S907	6137	353	691	S847	5297	353
512	G350	7845	161	572	G470	7005	161	632	S906	6123	161	692	S846	5283	161
513	G352	7831	257	573	G472	6991	257	633	S905	6109	257	693	S845	5269	257
514	G354	7817	353	574	G474	6977	353	634	S904	6095	353	694	S844	5255	353
515	G356	7803	161	575	G476	6963	161	635	S903	6081	161	695	S843	5241	161
516	G358	7789	257	576	G478	6949	257	636	S902	6067	257	696	S842	5227	257
517	G360	7775	353	577	G480	6935	353	637	S901	6053	353	697	S841	5213	353
518	G362	7761	161	578	S960	6879	161	638	S900	6039	161	698	S840	5199	161
519	G364	7747	257	579	S959	6865	257	639	S899	6025	257	699	S839	5185	257
520	G366	7733	353	580	S958	6851	353	640	S898	6011	353	700	S838	5171	353
521	G368	7719	161	581	S957	6837	161	641	S897	5997	161	701	S837	5157	161
522	G370	7705	257	582	S956	6823	257	642	S896	5983	257	702	S836	5143	257
523	G372	7691	353	583	S955	6809	353	643	S895	5969	353	703	S835	5129	353
524	G374	7677	161	584	S954	6795	161	644	S894	5955	161	704	S834	5115	161
525	G376	7663	257	585	S953	6781	257	645	S893	5941	257	705	S833	5101	257
526	G378	7649	353	586	S952	6767	353	646	S892	5927	353	706	S832	5087	353
527	G380	7635	161	587	S951	6753	161	647	S891	5913	161	707	S831	5073	161
528	G382	7621	257	588	S950	6739	257	648	S890	5899	257	708	S830	5059	257
529	G384	7607	353	589	S949	6725	353	649	S889	5885	353	709	S829	5045	353
530	G386	7593	161	590	S948	6711	161	650	S888	5871	161	710	S828	5031	161
531	G388	7579	257	591	S947	6697	257	651	S887	5857	257	711	S827	5017	257
532	G390	7565	353	592	S946	6683	353	652	S886	5843	353	712	S826	5003	353
533	G392	7551	161	593	S945	6669	161	653	S885	5829	161	713	S825	4989	161
534	G394	7537	257	594	S944	6655	257	654	S884	5815	257	714	S824	4975	257
535	G396	7523	353	595	S943	6641	353	655	S883	5801	353	715	S823	4961	353
536	G398	7509	161	596	S942	6627	161	656	S882	5787	161	716	S822	4947	161
537	G400	7495	257	597	S941	6613	257	657	S881	5773	257	717	S821	4933	257
538	G402	7481	353	598	S940	6599	353	658	S880	5759	353	718	S820	4919	353
539	G404	7467	161	599	S939	6585	161	659	S879	5745	161	719	S819	4905	161
540	G406	7453	257	600	S938	6571	257	660	S878	5731	257	720	S818	4891	257

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
721	S817	4877	353	781	S757	4037	353	841	S697	3197	353	901	S637	2357	353
722	S816	4863	161	782	S756	4023	161	842	S696	3183	161	902	S636	2343	161
723	S815	4849	257	783	S755	4009	257	843	S695	3169	257	903	S635	2329	257
724	S814	4835	353	784	S754	3995	353	844	S694	3155	353	904	S634	2315	353
725	S813	4821	161	785	S753	3981	161	845	S693	3141	161	905	S633	2301	161
726	S812	4807	257	786	S752	3967	257	846	S692	3127	257	906	S632	2287	257
727	S811	4793	353	787	S751	3953	353	847	S691	3113	353	907	S631	2273	353
728	S810	4779	161	788	S750	3939	161	848	S690	3099	161	908	S630	2259	161
729	S809	4765	257	789	S749	3925	257	849	S689	3085	257	909	S629	2245	257
730	S808	4751	353	790	S748	3911	353	850	S688	3071	353	910	S628	2231	353
731	S807	4737	161	791	S747	3897	161	851	S687	3057	161	911	S627	2217	161
732	S806	4723	257	792	S746	3883	257	852	S686	3043	257	912	S626	2203	257
733	S805	4709	353	793	S745	3869	353	853	S685	3029	353	913	S625	2189	353
734	S804	4695	161	794	S744	3855	161	854	S684	3015	161	914	S624	2175	161
735	S803	4681	257	795	S743	3841	257	855	S683	3001	257	915	S623	2161	257
736	S802	4667	353	796	S742	3827	353	856	S682	2987	353	916	S622	2147	353
737	S801	4653	161	797	S741	3813	161	857	S681	2973	161	917	S621	2133	161
738	S800	4639	257	798	S740	3799	257	858	S680	2959	257	918	S620	2119	257
739	S799	4625	353	799	S739	3785	353	859	S679	2945	353	919	S619	2105	353
740	S798	4611	161	800	S738	3771	161	860	S678	2931	161	920	S618	2091	161
741	S797	4597	257	801	S737	3757	257	861	S677	2917	257	921	S617	2077	257
742	S796	4583	353	802	S736	3743	353	862	S676	2903	353	922	S616	2063	353
743	S795	4569	161	803	S735	3729	161	863	S675	2889	161	923	S615	2049	161
744	S794	4555	257	804	S734	3715	257	864	S674	2875	257	924	S614	2035	257
745	S793	4541	353	805	S733	3701	353	865	S673	2861	353	925	S613	2021	353
746	S792	4527	161	806	S732	3687	161	866	S672	2847	161	926	S612	2007	161
747	S791	4513	257	807	S731	3673	257	867	S671	2833	257	927	S611	1993	257
748	S790	4499	353	808	S730	3659	353	868	S670	2819	353	928	S610	1979	353
749	S789	4485	161	809	S729	3645	161	869	S669	2805	161	929	S609	1965	161
750	S788	4471	257	810	S728	3631	257	870	S668	2791	257	930	S608	1951	257
751	S787	4457	353	811	S727	3617	353	871	S667	2777	353	931	S607	1937	353
752	S786	4443	161	812	S726	3603	161	872	S666	2763	161	932	S606	1923	161
753	S785	4429	257	813	S725	3589	257	873	S665	2749	257	933	S605	1909	257
754	S784	4415	353	814	S724	3575	353	874	S664	2735	353	934	S604	1895	353
755	S783	4401	161	815	S723	3561	161	875	S663	2721	161	935	S603	1881	161
756	S782	4387	257	816	S722	3547	257	876	S662	2707	257	936	S602	1867	257
757	S781	4373	353	817	S721	3533	353	877	S661	2693	353	937	S601	1853	353
758	S780	4359	161	818	S720	3519	161	878	S660	2679	161	938	S600	1839	161
759	S779	4345	257	819	S719	3505	257	879	S659	2665	257	939	S599	1825	257
760	S778	4331	353	820	S718	3491	353	880	S658	2651	353	940	S598	1811	353
761	S777	4317	161	821	S717	3477	161	881	S657	2637	161	941	S597	1797	161
762	S776	4303	257	822	S716	3463	257	882	S656	2623	257	942	S596	1783	257
763	S775	4289	353	823	S715	3449	353	883	S655	2609	353	943	S595	1769	353
764	S774	4275	161	824	S714	3435	161	884	S654	2595	161	944	S594	1755	161
765	S773	4261	257	825	S713	3421	257	885	S653	2581	257	945	S593	1741	257
766	S772	4247	353	826	S712	3407	353	886	S652	2567	353	946	S592	1727	353
767	S771	4233	161	827	S711	3393	161	887	S651	2553	161	947	S591	1713	161
768	S770	4219	257	828	S710	3379	257	888	S650	2539	257	948	S590	1699	257
769	S769	4205	353	829	S709	3365	353	889	S649	2525	353	949	S589	1685	353
770	S768	4191	161	830	S708	3351	161	890	S648	2511	161	950	S588	1671	161
771	S767	4177	257	831	S707	3337	257	891	S647	2497	257	951	S587	1657	257
772	S766	4163	353	832	S706	3323	353	892	S646	2483	353	952	S586	1643	353
773	S765	4149	161	833	S705	3309	161	893	S645	2469	161	953	S585	1629	161
774	S764	4135	257	834	S704	3295	257	894	S644	2455	257	954	S584	1615	257
775	S763	4121	353	835	S703	3281	353	895	S643	2441	353	955	S583	1601	353
776	S762	4107	161	836	S702	3267	161	896	S642	2427	161	956	S582	1587	161
777	S761	4093	257	837	S701	3253	257	897	S641	2413	257	957	S581	1573	257
778	S760	4079	353	838	S700	3239	353	898	S640	2399	353	958	S580	1559	353
779	S759	4065	161	839	S699	3225	161	899	S639	2385	161	959	S579	1545	161
780	S758	4051	257	840	S698	3211	257	900	S638	2371	257	960	S578	1531	257

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
961	S577	1517	353	1021	S517	677	353	1081	S457	-495	353	1141	S397	-1335	353
962	S576	1503	161	1022	S516	663	161	1082	S456	-509	161	1142	S396	-1349	161
963	S575	1489	257	1023	S515	649	257	1083	S455	-523	257	1143	S395	-1363	257
964	S574	1475	353	1024	S514	635	353	1084	S454	-537	353	1144	S394	-1377	353
965	S573	1461	161	1025	S513	621	161	1085	S453	-551	161	1145	S393	-1391	161
966	S572	1447	257	1026	S512	607	257	1086	S452	-565	257	1146	S392	-1405	257
967	S571	1433	353	1027	S511	593	353	1087	S451	-579	353	1147	S391	-1419	353
968	S570	1419	161	1028	S510	579	161	1088	S450	-593	161	1148	S390	-1433	161
969	S569	1405	257	1029	S509	565	257	1089	S449	-607	257	1149	S389	-1447	257
970	S568	1391	353	1030	S508	551	353	1090	S448	-621	353	1150	S388	-1461	353
971	S567	1377	161	1031	S507	537	161	1091	S447	-635	161	1151	S387	-1475	161
972	S566	1363	257	1032	S506	523	257	1092	S446	-649	257	1152	S386	-1489	257
973	S565	1349	353	1033	S505	509	353	1093	S445	-663	353	1153	S385	-1503	353
974	S564	1335	161	1034	S504	495	161	1094	S444	-677	161	1154	S384	-1517	161
975	S563	1321	257	1035	S503	481	257	1095	S443	-691	257	1155	S383	-1531	257
976	S562	1307	353	1036	S502	467	353	1096	S442	-705	353	1156	S382	-1545	353
977	S561	1293	161	1037	S501	453	161	1097	S441	-719	161	1157	S381	-1559	161
978	S560	1279	257	1038	S500	439	257	1098	S440	-733	257	1158	S380	-1573	257
979	S559	1265	353	1039	S499	425	353	1099	S439	-747	353	1159	S379	-1587	353
980	S558	1251	161	1040	S498	411	161	1100	S438	-761	161	1160	S378	-1601	161
981	S557	1237	257	1041	S497	397	257	1101	S437	-775	257	1161	S377	-1615	257
982	S556	1223	353	1042	S496	383	353	1102	S436	-789	353	1162	S376	-1629	353
983	S555	1209	161	1043	S495	369	161	1103	S435	-803	161	1163	S375	-1643	161
984	S554	1195	257	1044	S494	355	257	1104	S434	-817	257	1164	S374	-1657	257
985	S553	1181	353	1045	S493	341	353	1105	S433	-831	353	1165	S373	-1671	353
986	S552	1167	161	1046	S492	327	161	1106	S432	-845	161	1166	S372	-1685	161
987	S551	1153	257	1047	S491	313	257	1107	S431	-859	257	1167	S371	-1699	257
988	S550	1139	353	1048	S490	299	353	1108	S430	-873	353	1168	S370	-1713	353
989	S549	1125	161	1049	S489	285	161	1109	S429	-887	161	1169	S369	-1727	161
990	S548	1111	257	1050	S488	271	257	1110	S428	-901	257	1170	S368	-1741	257
991	S547	1097	353	1051	S487	257	353	1111	S427	-915	353	1171	S367	-1755	353
992	S546	1083	161	1052	S486	243	161	1112	S426	-929	161	1172	S366	-1769	161
993	S545	1069	257	1053	S485	229	257	1113	S425	-943	257	1173	S365	-1783	257
994	S544	1055	353	1054	S484	215	353	1114	S424	-957	353	1174	S364	-1797	353
995	S543	1041	161	1055	S483	201	161	1115	S423	-971	161	1175	S363	-1811	161
996	S542	1027	257	1056	S482	187	257	1116	S422	-985	257	1176	S362	-1825	257
997	S541	1013	353	1057	S481	173	353	1117	S421	-999	353	1177	S361	-1839	353
998	S540	999	161	1058	S480	-173	161	1118	S420	-1013	161	1178	S360	-1853	161
999	S539	985	257	1059	S479	-187	257	1119	S419	-1027	257	1179	S359	-1867	257
1000	S538	971	353	1060	S478	-201	353	1120	S418	-1041	353	1180	S358	-1881	353
1001	S537	957	161	1061	S477	-215	161	1121	S417	-1055	161	1181	S357	-1895	161
1002	S536	943	257	1062	S476	-229	257	1122	S416	-1069	257	1182	S356	-1909	257
1003	S535	929	353	1063	S475	-243	353	1123	S415	-1083	353	1183	S355	-1923	353
1004	S534	915	161	1064	S474	-257	161	1124	S414	-1097	161	1184	S354	-1937	161
1005	S533	901	257	1065	S473	-271	257	1125	S413	-1111	257	1185	S353	-1951	257
1006	S532	887	353	1066	S472	-285	353	1126	S412	-1125	353	1186	S352	-1965	353
1007	S531	873	161	1067	S471	-299	161	1127	S411	-1139	161	1187	S351	-1979	161
1008	S530	859	257	1068	S470	-313	257	1128	S410	-1153	257	1188	S350	-1993	257
1009	S529	845	353	1069	S469	-327	353	1129	S409	-1167	353	1189	S349	-2007	353
1010	S528	831	161	1070	S468	-341	161	1130	S408	-1181	161	1190	S348	-2021	161
1011	S527	817	257	1071	S467	-355	257	1131	S407	-1195	257	1191	S347	-2035	257
1012	S526	803	353	1072	S466	-369	353	1132	S406	-1209	353	1192	S346	-2049	353
1013	S525	789	161	1073	S465	-383	161	1133	S405	-1223	161	1193	S345	-2063	161
1014	S524	775	257	1074	S464	-397	257	1134	S404	-1237	257	1194	S344	-2077	257
1015	S523	761	353	1075	S463	-411	353	1135	S403	-1251	353	1195	S343	-2091	353
1016	S522	747	161	1076	S462	-425	161	1136	S402	-1265	161	1196	S342	-2105	161
1017	S521	733	257	1077	S461	-439	257	1137	S401	-1279	257	1197	S341	-2119	257
1018	S520	719	353	1078	S460	-453	353	1138	S400	-1293	353	1198	S340	-2133	353
1019	S519	705	161	1079	S459	-467	161	1139	S399	-1307	161	1199	S339	-2147	161
1020	S518	691	257	1080	S458	-481	257	1140	S398	-1321	257	1200	S338	-2161	257

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1201	S337	-2175	353	1261	S277	-3015	353	1321	S217	-3855	353	1381	S157	-4695	353
1202	S336	-2189	161	1262	S276	-3029	161	1322	S216	-3869	161	1382	S156	-4709	161
1203	S335	-2203	257	1263	S275	-3043	257	1323	S215	-3883	257	1383	S155	-4723	257
1204	S334	-2217	353	1264	S274	-3057	353	1324	S214	-3897	353	1384	S154	-4737	353
1205	S333	-2231	161	1265	S273	-3071	161	1325	S213	-3911	161	1385	S153	-4751	161
1206	S332	-2245	257	1266	S272	-3085	257	1326	S212	-3925	257	1386	S152	-4765	257
1207	S331	-2259	353	1267	S271	-3099	353	1327	S211	-3939	353	1387	S151	-4779	353
1208	S330	-2273	161	1268	S270	-3113	161	1328	S210	-3953	161	1388	S150	-4793	161
1209	S329	-2287	257	1269	S269	-3127	257	1329	S209	-3967	257	1389	S149	-4807	257
1210	S328	-2301	353	1270	S268	-3141	353	1330	S208	-3981	353	1390	S148	-4821	353
1211	S327	-2315	161	1271	S267	-3155	161	1331	S207	-3995	161	1391	S147	-4835	161
1212	S326	-2329	257	1272	S266	-3169	257	1332	S206	-4009	257	1392	S146	-4849	257
1213	S325	-2343	353	1273	S265	-3183	353	1333	S205	-4023	353	1393	S145	-4863	353
1214	S324	-2357	161	1274	S264	-3197	161	1334	S204	-4037	161	1394	S144	-4877	161
1215	S323	-2371	257	1275	S263	-3211	257	1335	S203	-4051	257	1395	S143	-4891	257
1216	S322	-2385	353	1276	S262	-3225	353	1336	S202	-4065	353	1396	S142	-4905	353
1217	S321	-2399	161	1277	S261	-3239	161	1337	S201	-4079	161	1397	S141	-4919	161
1218	S320	-2413	257	1278	S260	-3253	257	1338	S200	-4093	257	1398	S140	-4933	257
1219	S319	-2427	353	1279	S259	-3267	353	1339	S199	-4107	353	1399	S139	-4947	353
1220	S318	-2441	161	1280	S258	-3281	161	1340	S198	-4121	161	1400	S138	-4961	161
1221	S317	-2455	257	1281	S257	-3295	257	1341	S197	-4135	257	1401	S137	-4975	257
1222	S316	-2469	353	1282	S256	-3309	353	1342	S196	-4149	353	1402	S136	-4989	353
1223	S315	-2483	161	1283	S255	-3323	161	1343	S195	-4163	161	1403	S135	-5003	161
1224	S314	-2497	257	1284	S254	-3337	257	1344	S194	-4177	257	1404	S134	-5017	257
1225	S313	-2511	353	1285	S253	-3351	353	1345	S193	-4191	353	1405	S133	-5031	353
1226	S312	-2525	161	1286	S252	-3365	161	1346	S192	-4205	161	1406	S132	-5045	161
1227	S311	-2539	257	1287	S251	-3379	257	1347	S191	-4219	257	1407	S131	-5059	257
1228	S310	-2553	353	1288	S250	-3393	353	1348	S190	-4233	353	1408	S130	-5073	353
1229	S309	-2567	161	1289	S249	-3407	161	1349	S189	-4247	161	1409	S129	-5087	161
1230	S308	-2581	257	1290	S248	-3421	257	1350	S188	-4261	257	1410	S128	-5101	257
1231	S307	-2595	353	1291	S247	-3435	353	1351	S187	-4275	353	1411	S127	-5115	353
1232	S306	-2609	161	1292	S246	-3449	161	1352	S186	-4289	161	1412	S126	-5129	161
1233	S305	-2623	257	1293	S245	-3463	257	1353	S185	-4303	257	1413	S125	-5143	257
1234	S304	-2637	353	1294	S244	-3477	353	1354	S184	-4317	353	1414	S124	-5157	353
1235	S303	-2651	161	1295	S243	-3491	161	1355	S183	-4331	161	1415	S123	-5171	161
1236	S302	-2665	257	1296	S242	-3505	257	1356	S182	-4345	257	1416	S122	-5185	257
1237	S301	-2679	353	1297	S241	-3519	353	1357	S181	-4359	353	1417	S121	-5199	353
1238	S300	-2693	161	1298	S240	-3533	161	1358	S180	-4373	161	1418	S120	-5213	161
1239	S299	-2707	257	1299	S239	-3547	257	1359	S179	-4387	257	1419	S119	-5227	257
1240	S298	-2721	353	1300	S238	-3561	353	1360	S178	-4401	353	1420	S118	-5241	353
1241	S297	-2735	161	1301	S237	-3575	161	1361	S177	-4415	161	1421	S117	-5255	161
1242	S296	-2749	257	1302	S236	-3589	257	1362	S176	-4429	257	1422	S116	-5269	257
1243	S295	-2763	353	1303	S235	-3603	353	1363	S175	-4443	353	1423	S115	-5283	353
1244	S294	-2777	161	1304	S234	-3617	161	1364	S174	-4457	161	1424	S114	-5297	161
1245	S293	-2791	257	1305	S233	-3631	257	1365	S173	-4471	257	1425	S113	-5311	257
1246	S292	-2805	353	1306	S232	-3645	353	1366	S172	-4485	353	1426	S112	-5325	353
1247	S291	-2819	161	1307	S231	-3659	161	1367	S171	-4499	161	1427	S111	-5339	161
1248	S290	-2833	257	1308	S230	-3673	257	1368	S170	-4513	257	1428	S110	-5353	257
1249	S289	-2847	353	1309	S229	-3687	353	1369	S169	-4527	353	1429	S109	-5367	353
1250	S288	-2861	161	1310	S228	-3701	161	1370	S168	-4541	161	1430	S108	-5381	161
1251	S287	-2875	257	1311	S227	-3715	257	1371	S167	-4555	257	1431	S107	-5395	257
1252	S286	-2889	353	1312	S226	-3729	353	1372	S166	-4569	353	1432	S106	-5409	353
1253	S285	-2903	161	1313	S225	-3743	161	1373	S165	-4583	161	1433	S105	-5423	161
1254	S284	-2917	257	1314	S224	-3757	257	1374	S164	-4597	257	1434	S104	-5437	257
1255	S283	-2931	353	1315	S223	-3771	353	1375	S163	-4611	353	1435	S103	-5451	353
1256	S282	-2945	161	1316	S222	-3785	161	1376	S162	-4625	161	1436	S102	-5465	161
1257	S281	-2959	257	1317	S221	-3799	257	1377	S161	-4639	257	1437	S101	-5479	257
1258	S280	-2973	353	1318	S220	-3813	353	1378	S160	-4653	353	1438	S100	-5493	353
1259	S279	-2987	161	1319	S219	-3827	161	1379	S159	-4667	161	1439	S99	-5507	161
1260	S278	-3001	257	1320	S218	-3841	257	1380	S158	-4681	257	1440	S98	-5521	257

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1441	S97	-5535	353	1501	S37	-6375	353	1561	G433	-7257	353	1621	G313	-8097	353
1442	S96	-5549	161	1502	S36	-6389	161	1562	G431	-7271	161	1622	G311	-8111	161
1443	S95	-5563	257	1503	S35	-6403	257	1563	G429	-7285	257	1623	G309	-8125	257
1444	S94	-5577	353	1504	S34	-6417	353	1564	G427	-7299	353	1624	G307	-8139	353
1445	S93	-5591	161	1505	S33	-6431	161	1565	G425	-7313	161	1625	G305	-8153	161
1446	S92	-5605	257	1506	S32	-6445	257	1566	G423	-7327	257	1626	G303	-8167	257
1447	S91	-5619	353	1507	S31	-6459	353	1567	G421	-7341	353	1627	G301	-8181	353
1448	S90	-5633	161	1508	S30	-6473	161	1568	G419	-7355	161	1628	G299	-8195	161
1449	S89	-5647	257	1509	S29	-6487	257	1669	G417	-7369	257	1629	G297	-8209	257
1450	S88	-5661	353	1510	S28	-6501	353	1570	G415	-7383	353	1630	G295	-8223	353
1451	S87	-5675	161	1511	S27	-6515	161	1571	G413	-7397	161	1631	G293	-8237	161
1452	S86	-5689	257	1512	S26	-6529	257	1572	G411	-7411	257	1632	G291	-8251	257
1453	S85	-5703	353	1513	S25	-6543	353	1573	G409	-7425	353	1633	G289	-8265	353
1454	S84	-5717	161	1514	S24	-6557	161	1574	G407	-7439	161	1634	G287	-8279	161
1455	S83	-5731	257	1515	S23	-6571	257	1575	G405	-7453	257	1635	G285	-8293	257
1456	S82	-5745	353	1516	S22	-6585	353	1576	G403	-7467	353	1636	G283	-8307	353
1457	S81	-5759	161	1517	S21	-6599	161	1577	G401	-7481	161	1637	G281	-8321	161
1458	S80	-5773	257	1518	S20	-6613	257	1578	G399	-7495	257	1638	G279	-8335	257
1459	S79	-5787	353	1519	S19	-6627	353	1579	G397	-7509	353	1639	G277	-8349	353
1460	S78	-5801	161	1520	S18	-6641	161	1580	G395	-7523	161	1640	G275	-8363	161
1461	S77	-5815	257	1521	S17	-6655	257	1581	G393	-7537	257	1641	G273	-8377	257
1462	S76	-5829	353	1522	S16	-6669	353	1582	G391	-7551	353	1642	G271	-8391	353
1463	S75	-5843	161	1523	S15	-6683	161	1583	G389	-7565	161	1643	G269	-8405	161
1464	S74	-5857	257	1524	S14	-6697	257	1584	G387	-7579	257	1644	G267	-8419	257
1465	S73	-5871	353	1525	S13	-6711	353	1585	G385	-7593	353	1645	G265	-8433	353
1466	S72	-5885	161	1526	S12	-6725	161	1586	G383	-7607	161	1646	G263	-8447	161
1467	S71	-5899	257	1527	S11	-6739	257	1587	G381	-7621	257	1647	G261	-8461	257
1468	S70	-5913	353	1528	S10	-6753	353	1588	G379	-7635	353	1648	G259	-8475	353
1469	S69	-5927	161	1529	S9	-6767	161	1589	G377	-7649	161	1649	G257	-8489	161
1470	S68	-5941	257	1530	S8	-6781	257	1590	G375	-7663	257	1650	G255	-8503	257
1471	S67	-5955	353	1531	S7	-6795	353	1591	G373	-7677	353	1651	G253	-8517	353
1472	S66	-5969	161	1532	S6	-6809	161	1592	G371	-7691	161	1652	G251	-8531	161
1473	S65	-5983	257	1533	S5	-6823	257	1593	G369	-7705	257	1653	G249	-8545	257
1474	S64	-5997	353	1534	S4	-6837	353	1594	G367	-7719	353	1654	G247	-8559	353
1475	S63	-6011	161	1535	S3	-6851	161	1595	G365	-7733	161	1655	G245	-8573	161
1476	S62	-6025	257	1536	S2	-6865	257	1596	G363	-7747	257	1656	G243	-8587	257
1477	S61	-6039	353	1537	S1	-6879	353	1597	G361	-7761	353	1657	G241	-8601	353
1478	S60	-6053	161	1538	G479	-6935	161	1598	G359	-7775	161	1658	G239	-8615	161
1479	S59	-6067	257	1539	G477	-6949	257	1599	G357	-7789	257	1659	G237	-8629	257
1480	S58	-6081	353	1540	G475	-6963	353	1600	G355	-7803	353	1660	G235	-8643	353
1481	S57	-6095	161	1541	G473	-6977	161	1601	G353	-7817	161	1661	G233	-8657	161
1482	S56	-6109	257	1542	G471	-6991	257	1602	G351	-7831	257	1662	G231	-8671	257
1483	S55	-6123	353	1543	G469	-7005	353	1603	G349	-7845	353	1663	G229	-8685	353
1484	S54	-6137	161	1544	G467	-7019	161	1604	G347	-7859	161	1664	G227	-8699	161
1485	S53	-6151	257	1545	G465	-7033	257	1605	G345	-7873	257	1665	G225	-8713	257
1486	S52	-6165	353	1546	G463	-7047	353	1606	G343	-7887	353	1666	G223	-8727	353
1487	S51	-6179	161	1547	G461	-7061	161	1607	G341	-7901	161	1667	G221	-8741	161
1488	S50	-6193	257	1548	G459	-7075	257	1608	G339	-7915	257	1668	G219	-8755	257
1489	S49	-6207	353	1549	G457	-7089	353	1609	G337	-7929	353	1669	G217	-8769	353
1490	S48	-6221	161	1550	G455	-7103	161	1610	G335	-7943	161	1670	G215	-8783	161
1491	S47	-6235	257	1551	G453	-7117	257	1611	G333	-7957	257	1671	G213	-8797	257
1492	S46	-6249	353	1552	G451	-7131	353	1612	G331	-7971	353	1672	G211	-8811	353
1493	S45	-6263	161	1553	G449	-7145	161	1613	G329	-7985	161	1673	G209	-8825	161
1494	S44	-6277	257	1554	G447	-7159	257	1614	G327	-7999	257	1674	G207	-8839	257
1495	S43	-6291	353	1555	G445	-7173	353	1615	G325	-8013	353	1675	G205	-8853	353
1496	S42	-6305	161	1556	G443	-7187	161	1616	G323	-8027	161	1676	G203	-8867	161
1497	S41	-6319	257	1557	G441	-7201	257	1617	G321	-8041	257	1677	G201	-8881	257
1498	S40	-6333	353	1558	G439	-7215	353	1618	G319	-8055	353	1678	G199	-8895	353
1499	S39	-6347	161	1559	G437	-7229	161	1619	G317	-8069	161	1679	G197	-8909	161
1500	S38	-6361	257	1560	G435	-7243	257	1620	G315	-8083	257	1680	G195	-8923	257

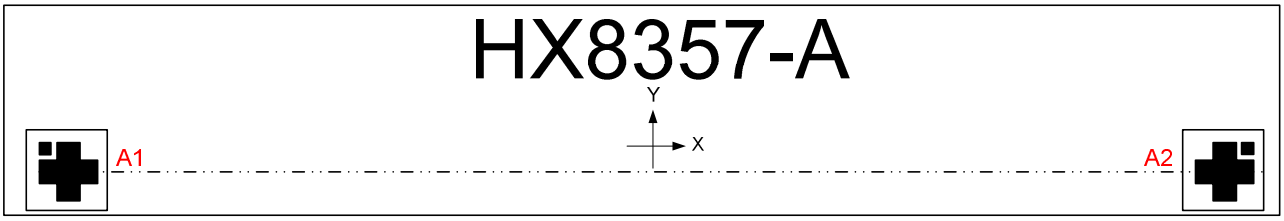
No.	Name	X	Y
1681	G193	-8937	353
1682	G191	-8951	161
1683	G189	-8965	257
1684	G187	-8979	353
1685	G185	-8993	161
1686	G183	-9007	257
1687	G181	-9021	353
1688	G179	-9035	161
1689	G177	-9049	257
1690	G175	-9063	353
1691	G173	-9077	161
1692	G171	-9091	257
1693	G169	-9105	353
1694	G167	-9119	161
1695	G165	-9133	257
1696	G163	-9147	353
1697	G161	-9161	161
1698	G159	-9175	257
1699	G157	-9189	353
1700	G155	-9203	161
1701	G153	-9217	257
1702	G151	-9231	353
1703	G149	-9245	161
1704	G147	-9259	257
1705	G145	-9273	353
1706	G143	-9287	161
1707	G141	-9301	257
1708	G139	-9315	353
1709	G137	-9329	161
1710	G135	-9343	257
1711	G133	-9357	353
1712	G131	-9371	161
1713	G129	-9385	257
1714	G127	-9399	353
1715	G125	-9413	161
1716	G123	-9427	257
1717	G121	-9441	353
1718	G119	-9455	161
1719	G117	-9469	257
1720	G115	-9483	353
1721	G113	-9497	161
1722	G111	-9511	257
1723	G109	-9525	353
1724	G107	-9539	161
1725	G105	-9553	257
1726	G103	-9567	353
1727	G101	-9581	161
1728	G99	-9595	257
1729	G97	-9609	353
1730	G95	-9623	161
1731	G93	-9637	257
1732	G91	-9651	353
1733	G89	-9665	161
1734	G87	-9679	257
1735	G85	-9693	353
1736	G83	-9707	161
1737	G81	-9721	257
1738	G79	-9735	353
1739	G77	-9749	161
1740	G75	-9763	257

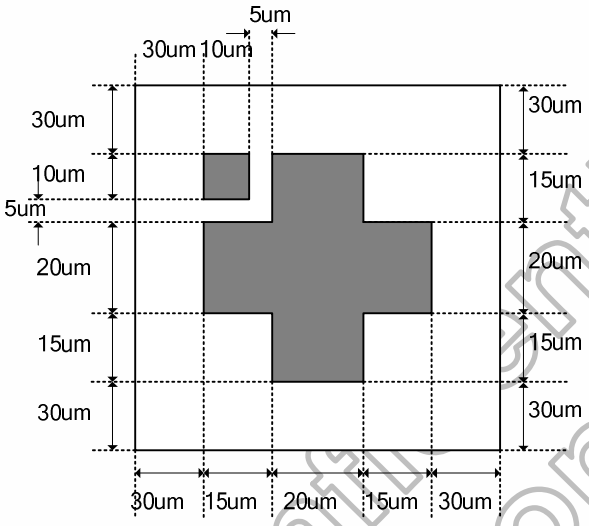
No.	Name	X	Y
1741	G73	-9777	353
1742	G71	-9791	161
1743	G69	-9805	257
1744	G67	-9819	353
1745	G65	-9833	161
1746	G63	-9847	257
1747	G61	-9861	353
1748	G59	-9875	161
1749	G57	-9889	257
1750	G55	-9903	353
1751	G53	-9917	161
1752	G51	-9931	257
1753	G49	-9945	353
1754	G47	-9959	161
1755	G45	-9973	257
1756	G43	-9987	353
1757	G41	-10001	161
1758	G39	-10015	257
1759	G37	-10029	353
1760	G35	-10043	161
1761	G33	-10057	257
1762	G31	-10071	353
1763	G29	-10085	161
1764	G27	-10099	257
1765	G25	-10113	353
1766	G23	-10127	161
1767	G21	-10141	257
1768	G19	-10155	353
1769	G17	-10169	161
1770	G15	-10183	257
1771	G13	-10197	353
1772	G11	-10211	161
1773	G9	-10225	257
1774	G7	-10239	353
1775	G5	-10253	161
1776	G3	-10267	257
1777	G1	-10281	353
1778	DUMMY	-10295	161
1779	DUMMY	-10309	257
1780	DUMMY	-10323	353

No.	name	X	Y

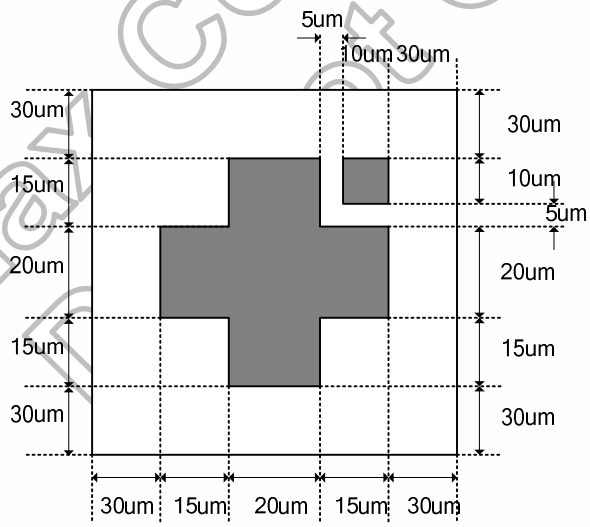
No.	name	X	Y

4.4 Alignment mark





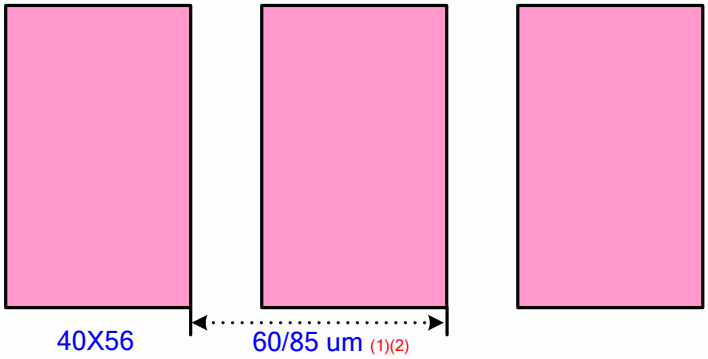
A1(-10390,-340)



A2 (10390,-340)

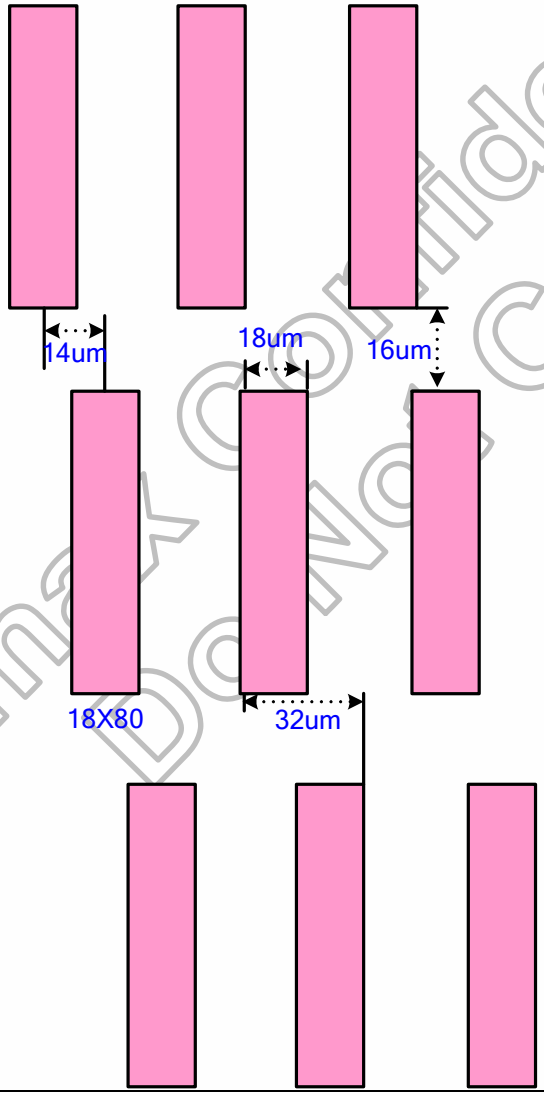
4.5 Bump size

Input PAD
(No.1 ~0 No.334)



Note:
(1) No.1~No.129 and No.151~No.334 are 60um
(2) No.130~No.150 are 85um

Output PAD
(No.335 ~ No.1780)



5. Interface

The HX8357-A supports two-type interface group: Command-Parameter interface group, Register-Content interface group.

This manual description focuses on Register-Content interface group. About the Command-Parameter interface mode, please refer to the HX8357-A(N) datasheet for detail.

In Register-Content interface group (IFSEL = 'L'), the HX8357-A has a system interface circuit for register command/GRAM data transferring, and a RGB interface circuit for display data transferring during animated display. The system interface circuit uses data bus pins (DB17-0). Since the data bus pins (DB17-0) can be used as input in RGB interface circuit, the HX8357-A shows animated display with less wiring.

System interface can be used to access internal command and internal 18-bit/pixel GRAM. The RGB interface is only used to access display data. Please make sure that in RGB interface mode, the input display data is not written to GRAM and is displayed directly.

5.1 System interface circuit

The system interface circuit in HX8357-A supports, 18-/16-/9-/8-bit bus width parallel bus system interface for I80 series CPU, and 4-/3-wire serial bus system interface for serial data input. When CSX = “L”, the parallel and serial bus system interface of the HX8357-A become active and data transfer through the interface circuit is available. The DCX_SCL pin specifies whether the system interface circuit access is to the register command or to the display data RAM. The input bus format of system interface circuit is selected by external pins setting. For selecting the input bus format, please refer to Table 5.1.

BS3	BS2	BS1	BS0	Interface	WRX_DCX	DCX_SCL	Data Bus use	
							Register/ Content	GRAM
0	0	0	0	8080 MCU 16-bits Parallel type I	WRX	DCX	DB7-DB0	DB15-DB0: 16-bit data
0	0	0	1	8080 MCU 8-bits Parallel type I	WRX	DCX	DB7-DB0	DB7-DB0: 8-bits Data
0	0	1	0	8080 MCU 16-bits Parallel type II	WRX	DCX	DB8-DB1	DB17-DB10, DB8-DB1: 16-bit data
0	0	1	1	8080 MCU 8-bits Parallel type II	WRX	DCX	DB17-DB10	DB17-DB10: 8-bits Data
0	1	0	ID	3-wire Serial interface	x	SCL	SDA	
1	1	0	-	4-wire Serial interface	DCX	SCL	SDA	
1	0	0	0	8080 MCU 18-bits Paralle type I	WRX	DCX	DB7-DB0	DB17-DB0: 18-bits Data
1	0	0	1	8080 MCU 9-bits Parallel type I	WRX	DCX	DB7-DB0	DB8-DB0: 9-bits Data
1	0	1	0	8080 MCU 18-bits Parallel type II	WRX	DCX	DB8-DB1	DB17-DB0: 18-bits Data
1	0	1	1	8080 MCU 9-bits Parallel type II	WRX	DCX	DB17-DB10	DB17-DB9: 9-bits Data
1	1	1	1	MDDI Interface	x	x	MDDI	MDDI
Other Setting				Setting Invalid				

Table 5. 1 Input Bus Format Selection of System Interface Circuit

It has an Index Register (IR) in HX8357-A to store index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DCX=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DCX=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

5.1.1 Parallel bus system interface

The input / output data from data pins (DB17-0) and signal operation of the I80 series parallel bus interface are listed in Table 5.2.

Operations	WRX_DCX	RDX_E	DCX_SCL
Writes Indexes into IR	0	1	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 5. 2 Data Pin Function for I80 Series CPU

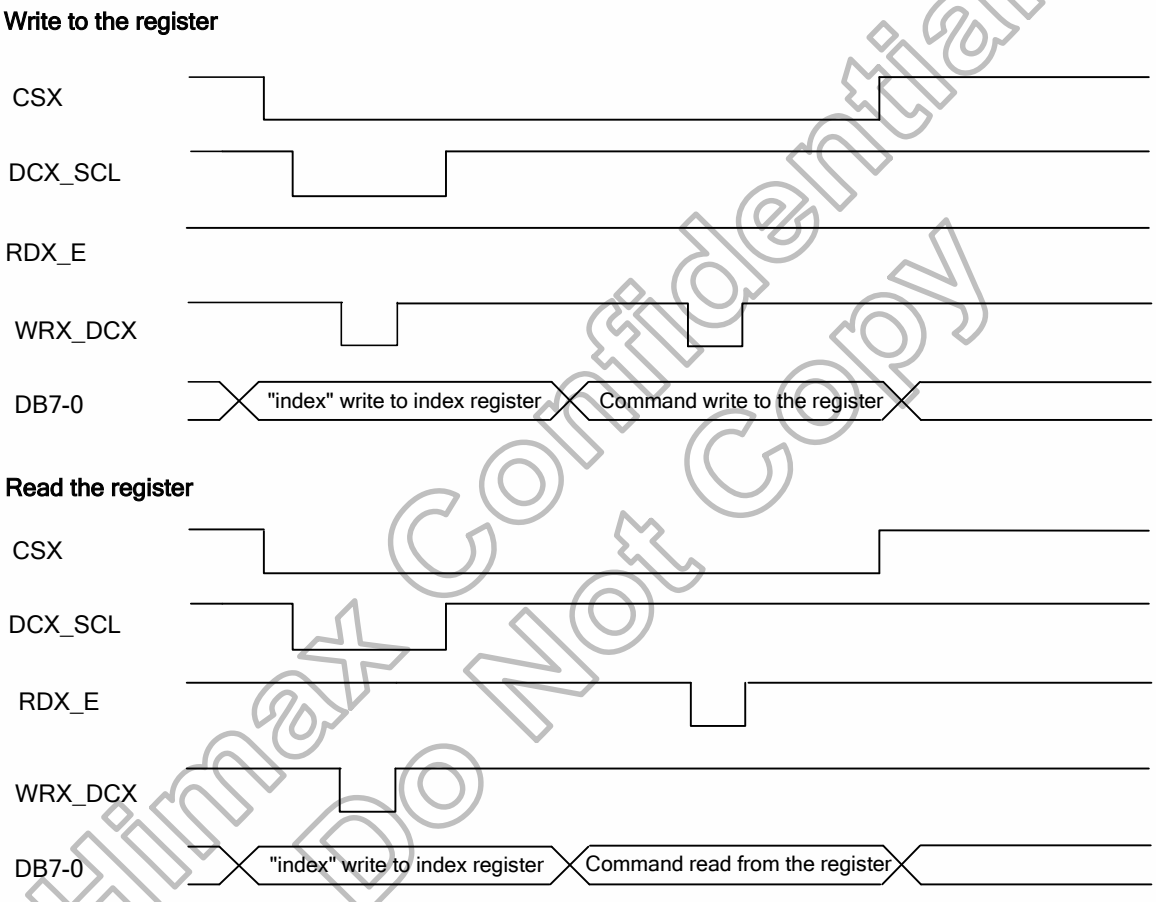


Figure 5. 1 Register Read/Write Timing in Parallel Bus System Interface (for I80 Series MPU)

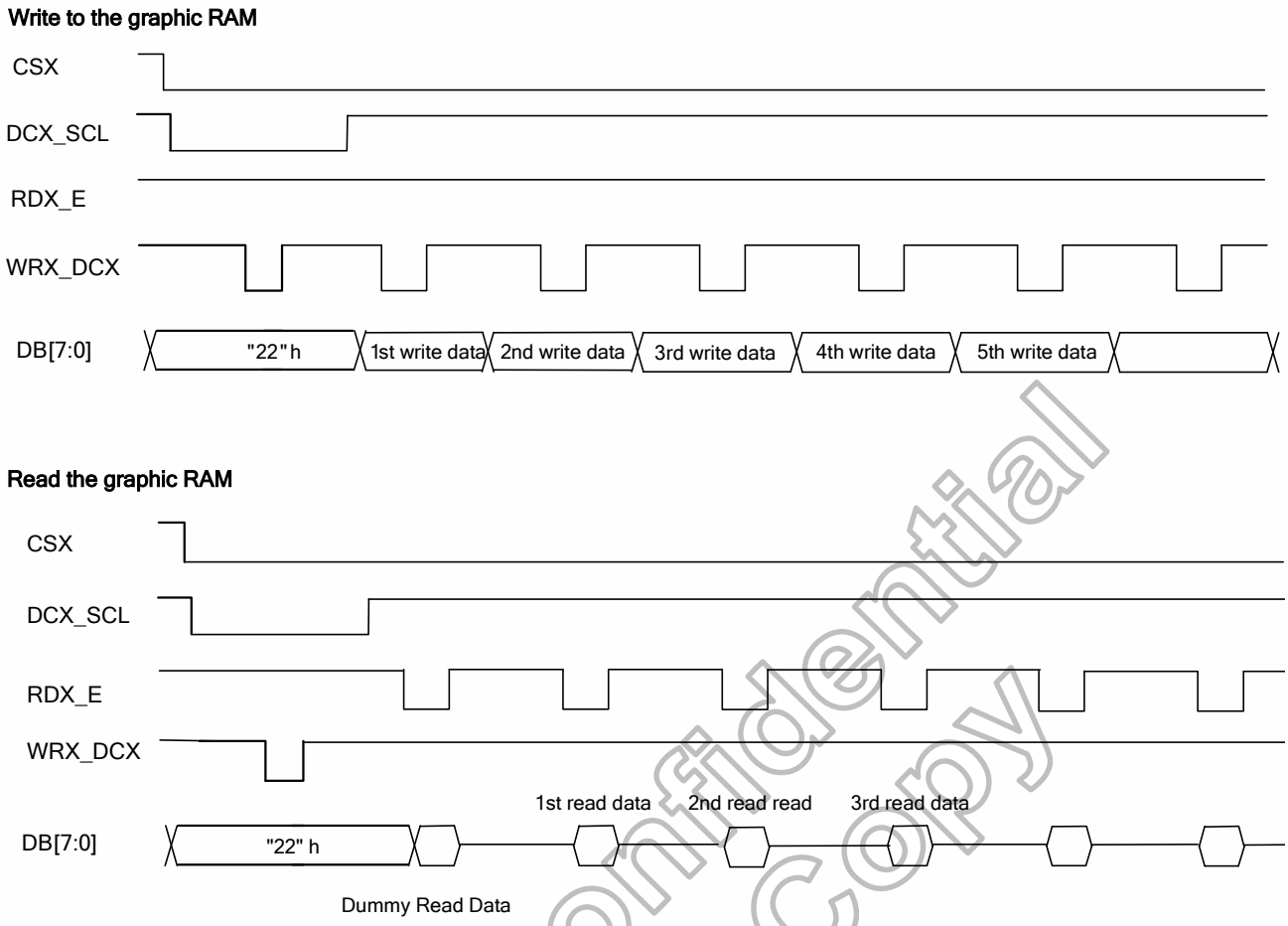


Figure 5. 2 GRAM Read/Write Timing in Parallel Bus System Interface (for I80 Series MPU)

5.1.2 MCU data color coding

MCU Data Color Coding for RAM data ***Write***

- Parallel 8-Bits Bus Interface typeI (BS3,BS2,BS1,BS0="0001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	x	x	x	x	x	x	R3	R2	R1	R0	G3	G2	G1	G0	4K-Color (2-pixels/ 3-bytes)
	x	x	x	x	x	x	x	x	x	x	B3	B2	B1	B0	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	x	x	G3	G2	G1	G0	B3	B2	B1	B0	
05h	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixels/ 2-bytes)
	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixels/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5. 3 8-Bits Parallel Interface Type I GRAM Write Table

- Parallel 16-Bits Bus Interface typeI (BS3,BS2,BS1,BS0="0000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h							R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Color
05h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	65K-Color
06h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	
07h	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	262K-Color (16+2)
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B1	B0	

Table 5. 4 16-Bits Parallel Interface Type I GRAM Write Table

- Parallel 9-Bits Bus Interface typeI (BS3,BS2,BS1,BS0="1001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixels/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5. 5 9-Bits Parallel Interface Type I GRAM Write Table

- Parallel 18-Bits Bus Interface typeI (BS3,BS2,BS1,BS0="1000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 5. 6 18-Bits Parallel Interface Type I GRAM Write Table

- Parallel 8-Bits Bus Interface typeII (BS3,BS2,BS1,BS0=”0011”)

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	R3	R2	R1	R0	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	4K-Color (2-pixels/ 3-bytes)
	B3	B2	B1	B0	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	
	G3	G2	G1	G0	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	x	65K-Color (1-pixels/ 2-bytes)
	G2	G1	G0	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
06h	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5. 7 8-Bits Parallel Interface Type II GRAM Write Table

- Parallel 16-Bits Bus Interface typeII (BS3,BS2,BS1,BS0=”0010”)

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
									x	0	0	1	0	0	0	1	0	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
03h	x	x	x	x	R3	R2	R1	R0	x	G3	G2	G1	G0	B3	B2	B1	B0	x	4K-Color
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	G2	G1	G0	B4	B3	B2	B1	B0	x	65K-Color
06h	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixels/ 3bytes)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	
07h	R5	R4	R3	R2	R1	R0	G5	G4	x	G3	G2	G1	G0	B5	B4	B3	B2	x	262K-Color (16+2)
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B1	B0	x	

Table 5. 8 16-Bits Parallel Interface Type II GRAM Write Set Table

- Parallel 9-Bits Bus Interface typeII (BS3,BS2,BS1,BS0=”1011”)

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	1	1	0	0	x	x	x	x	x	x	x	x	x	x	**22H**
17H	D8	D7	D6	D5	D4	D3	D2	D1	D0	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5. 9 9-Bits Parallel Interface Set Type II GRAM Write Table

- Parallel 18-Bits Bus Interface typeII (BS3,BS2,BS1,BS0=”1010”)

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
17H	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	**262K-Color**

Table 5. 10 18-Bits Parallel Interface Type II GRAM Write Set Table

18-bit Parallel bus system interface

The I80-system 18-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “BS3, BS2, BS1, BS0” pins to “1000”. And the I80-system 18-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “BS3, BS2, BS1, BS0” pins to “1010”. Figure 5.9 is the example of interface with I80 microcomputer system interface.

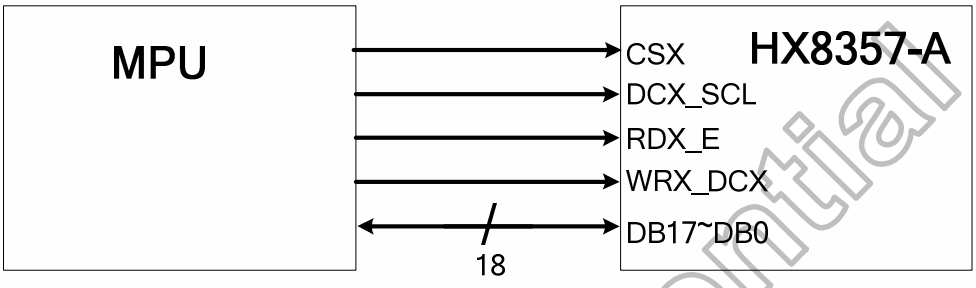


Figure 5. 3 Example of I80- System 18-bit Parallel Bus Interface

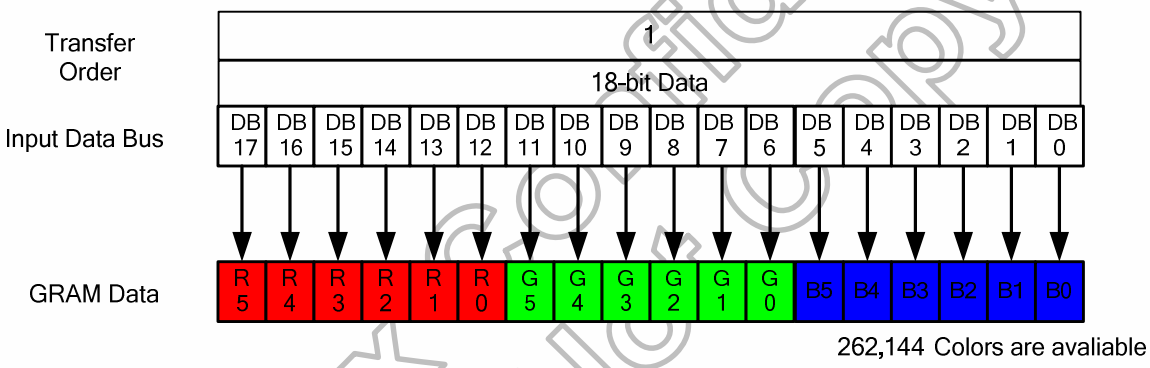


Figure 5. 4 Input Data Bus and GRAM Data Mapping in 18-Bit Bus System Interface with 18 Bit-Data Input (“BS3, BS2, BS1, BS0”=”1010” or “1000”)

16-bit Parallel bus system interface

The I80-system 16-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “BS3, BS2, BS1, BS0” pins to “0000”. And I80-system 16-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “BS3, BS2, BS1, BS0” pins to “0010”. Figure 5.5 is the example of type I interface with I80 microcomputer system interface. And Figure 5.6 is the example of type II interface with I80 microcomputer system interface.

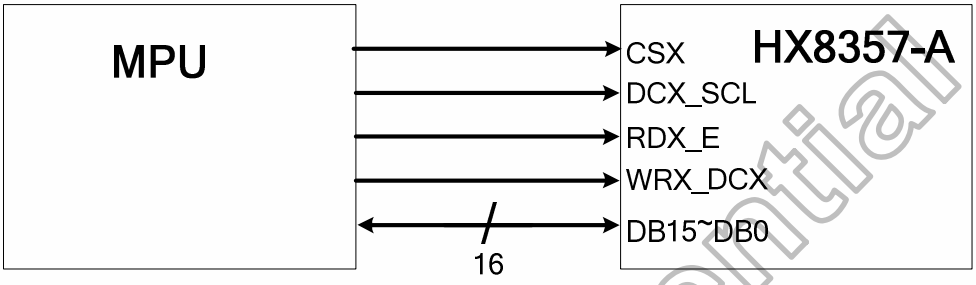


Figure 5. 5 Example of I80 System 16-bit Parallel Bus Interface type I

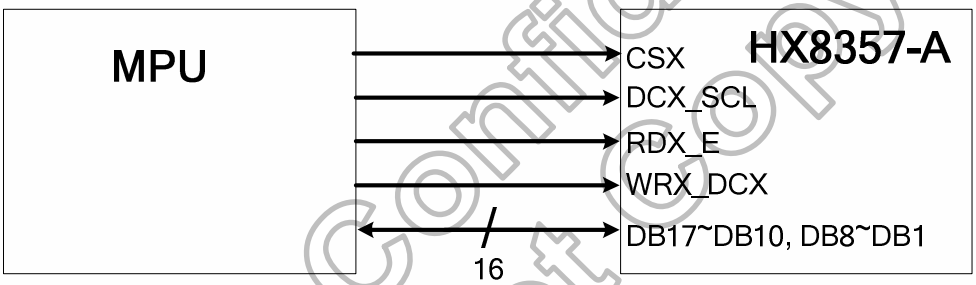


Figure 5. 6 Example of I80 System 16-bit Parallel Bus Interface type II

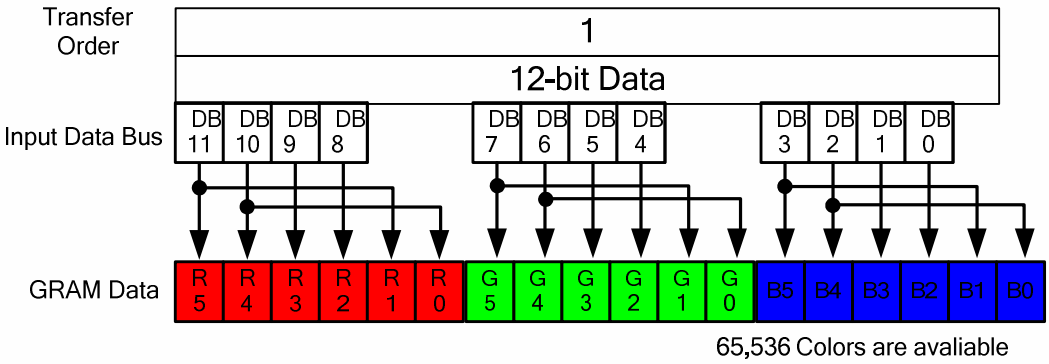


Figure 5. 7 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 12 Bit-Data Input (R17H=03h and "BS3, BS2, BS1, BS0"="0000")

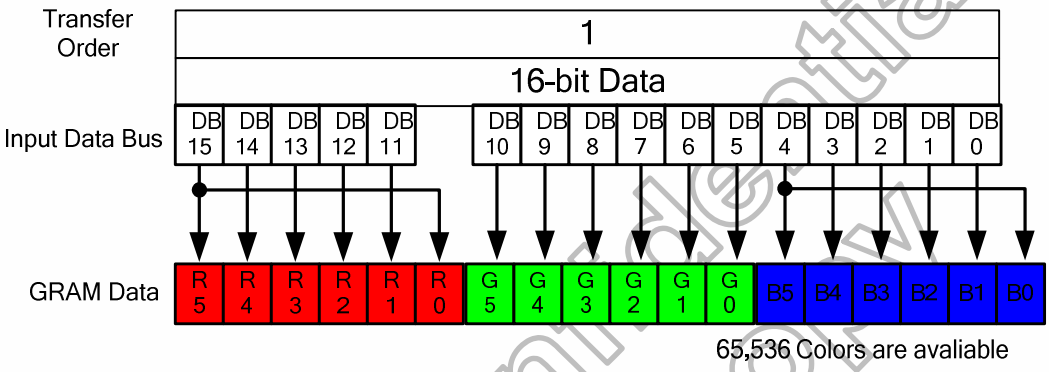


Figure 5. 8 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 16 Bit-Data Input (R17H=05h and "BS3, BS2, BS1, BS0"="0000")

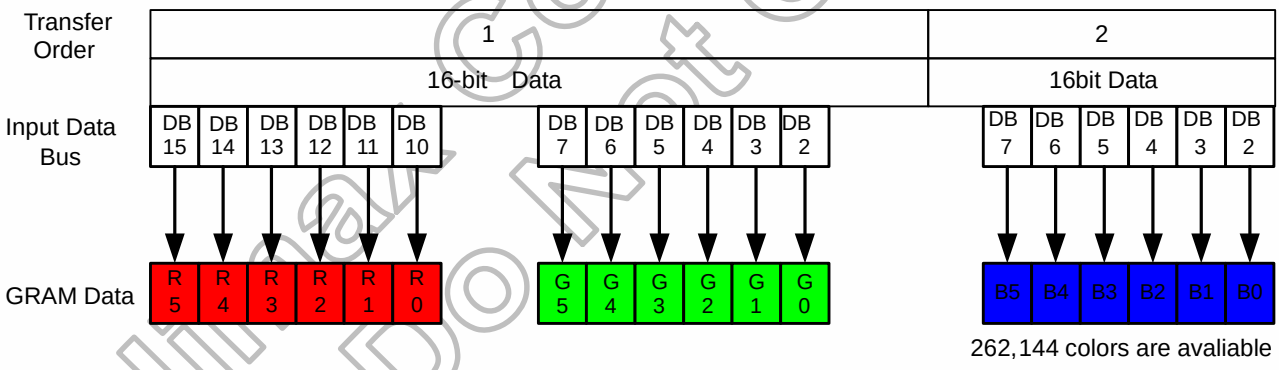


Figure 5. 9 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(12+6) Bit-Data Input (R17H=06h and "BS3, BS2, BS1, BS0"="0000")

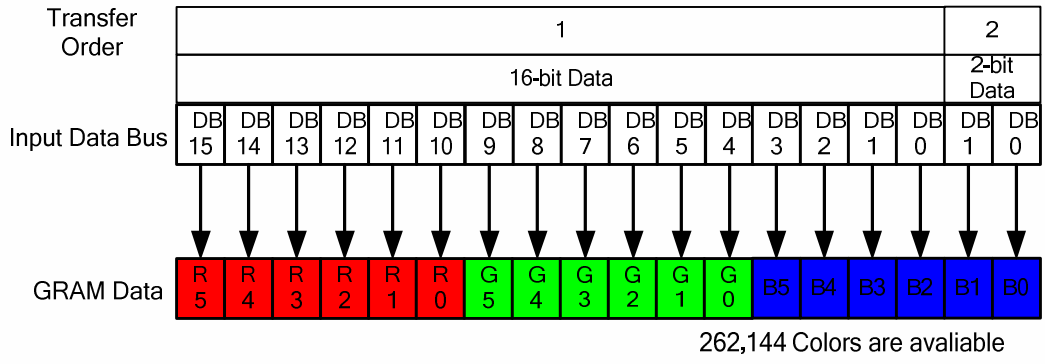


Figure 5. 10 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(16+2) Bit-Data Input (R17H=07h and "BS3,BS2, BS1, BS0"="0000")

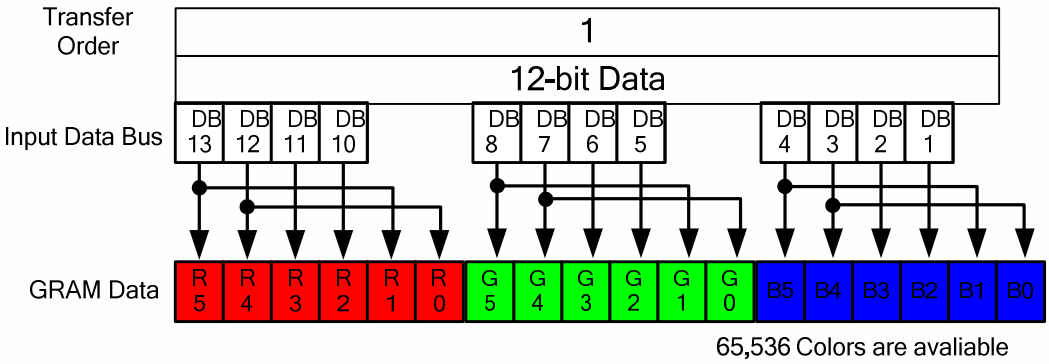


Figure 5. 11 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 12 Bit-Data Input (R17H=03h and "BS3, BS2, BS1, BS0"="0010")

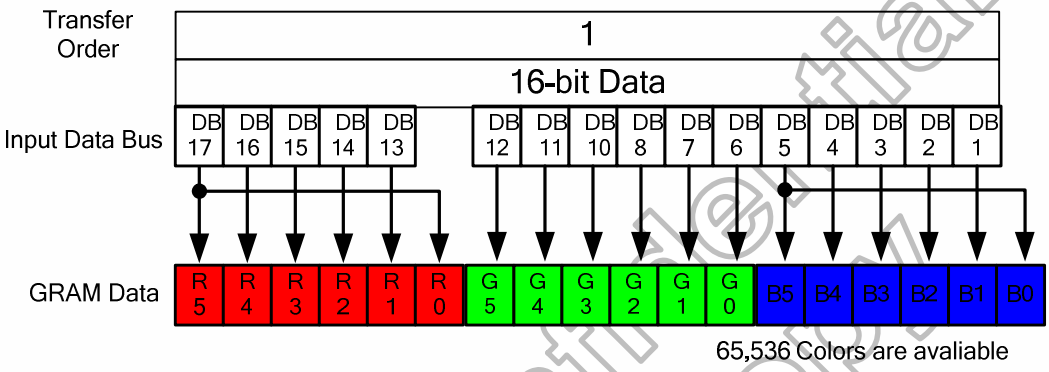


Figure 5. 12 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 16 Bit-Data Input (R17H=05h and "BS3, BS2, BS1, BS0"="0010")

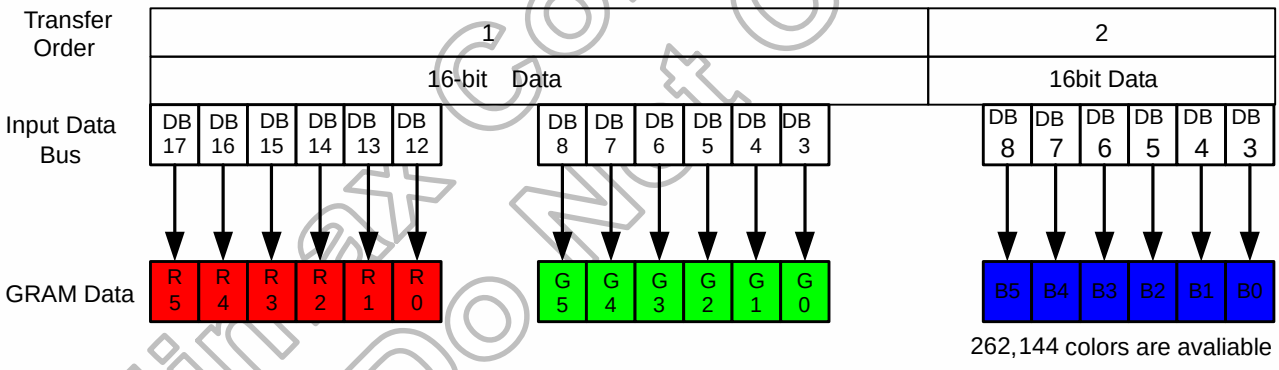


Figure 5. 13 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(12+6) Bit-Data Input (R17H=06h and "BS3, BS2, BS1, BS0"="0010")

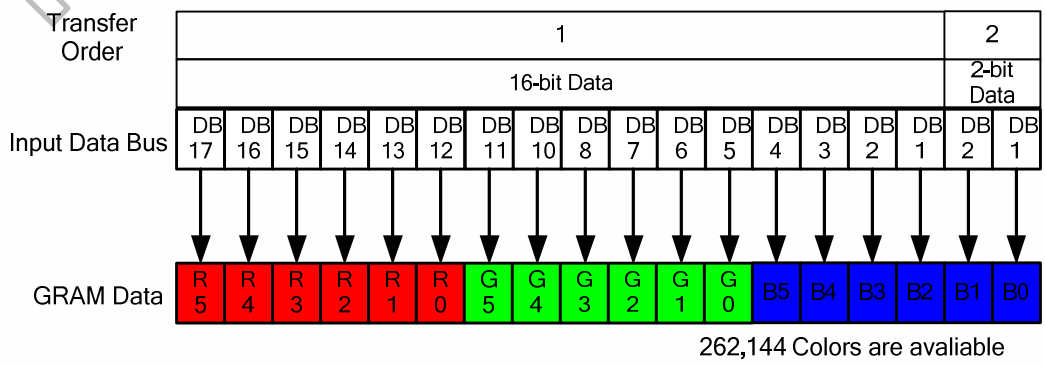


Figure 5. 14 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(16+2) Bit-Data Input (R17H=07h and "BS3, BS2, BS1, BS0"="0010")

9-bit Parallel bus system interface

The I80-system 9-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins “BS3, BS2, BS1, BS0” pins to “1001”. And I80-system 9-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting “BS3, BS2, BS1, BS0” pins to “1011”. Figure 5.5 is the example of type I interface with I80 microcomputer system interface. And Figure 5.6 is the example of type II interface with I80 microcomputer system interface.

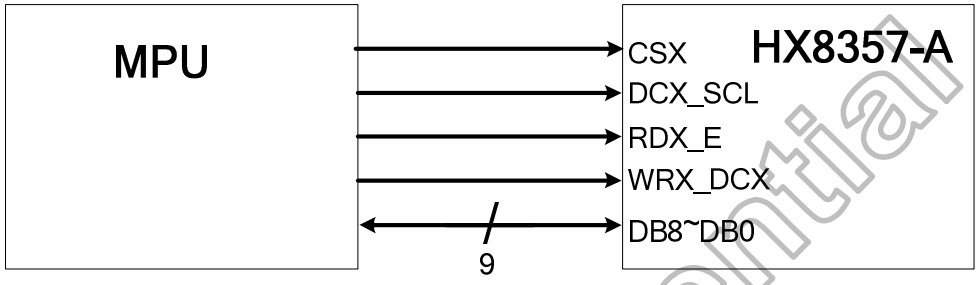


Figure 5. 15 Example of I80 System 9-bit Parallel Bus Interface type I

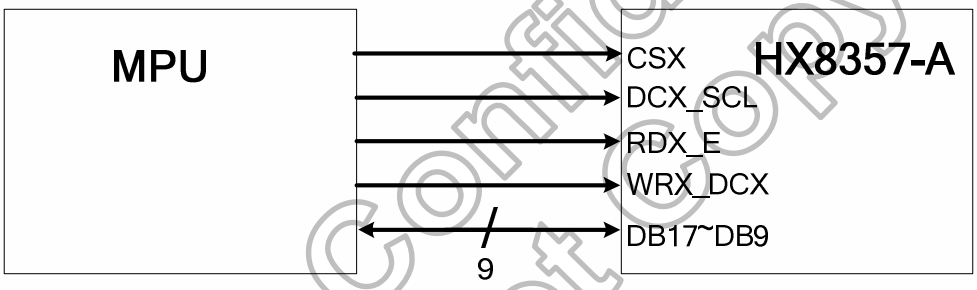


Figure 5. 16 Example of I80 System 9-bit Parallel Bus Interface type II

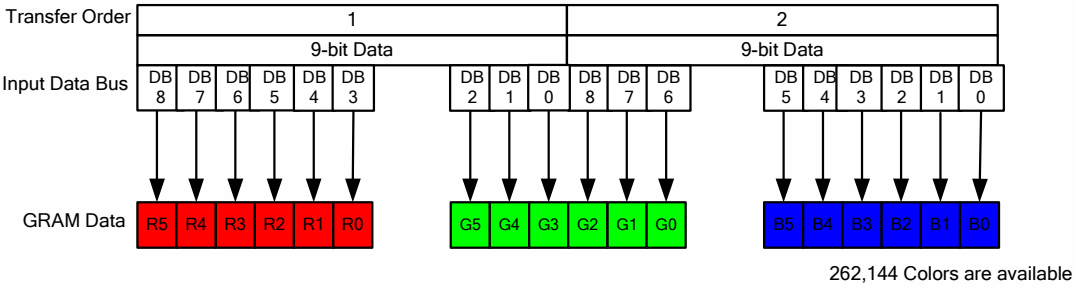


Figure 5. 17 Input Data Bus and GRAM Data Mapping in 9-Bit Bus System Interface with 18 Bit-Data Input (R17H=06h and "BS3, BS2, BS1, BS0"="1001")

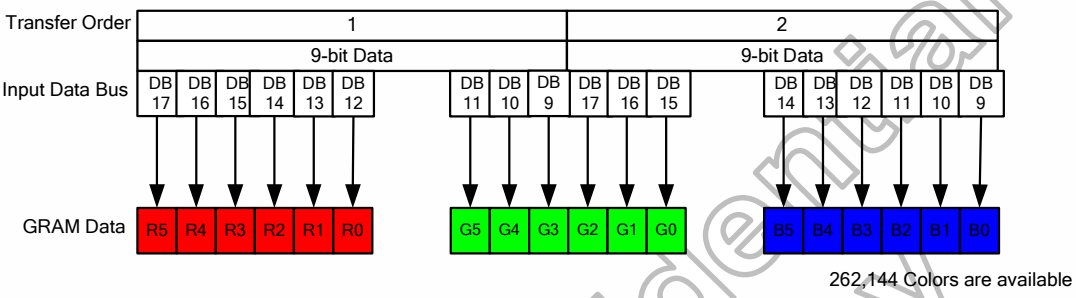


Figure 5. 18 Input Data Bus and GRAM Data Mapping in 9-Bit Bus System Interface with 18 Bit-Data Input (R17H=06h and "BS3, BS2, BS1, BS0"="1011")

8-bit Parallel bus system interface

The I80-system 8-bit parallel bus interface **type I** in command-parameter interface mode can be used by setting external pins ""BS3, BS2, BS1, BS0" pins to "0001". And I80-system 8-bit parallel bus interface **type II** in command-parameter interface mode can be used by setting ""BS3, BS2, BS1, BS0" pins to "0011". Figure 5.5 is the example of type I interface with I80 microcomputer system interface. And Figure 5.6 is the example of type II interface with I80 microcomputer system interface.

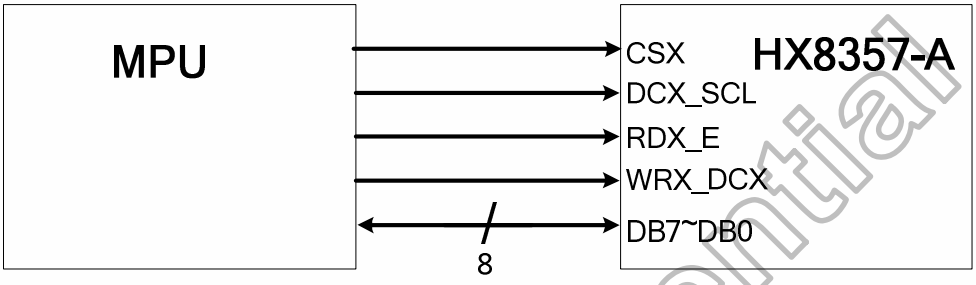


Figure 5. 19 Example of I80- System 8-bit Parallel Bus Interface type I

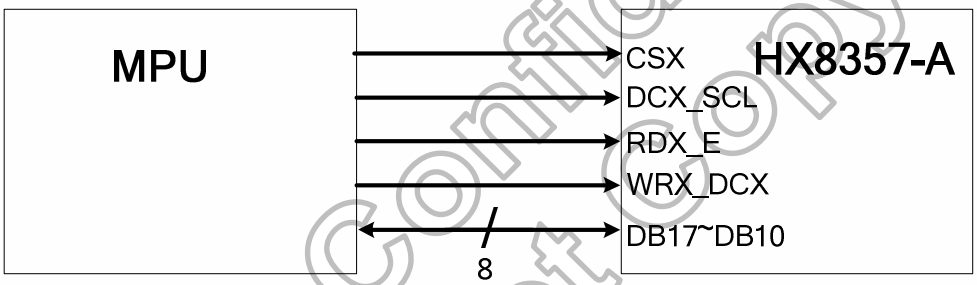


Figure 5. 20 Example of I80- System 8-bit Parallel Bus Interface type II

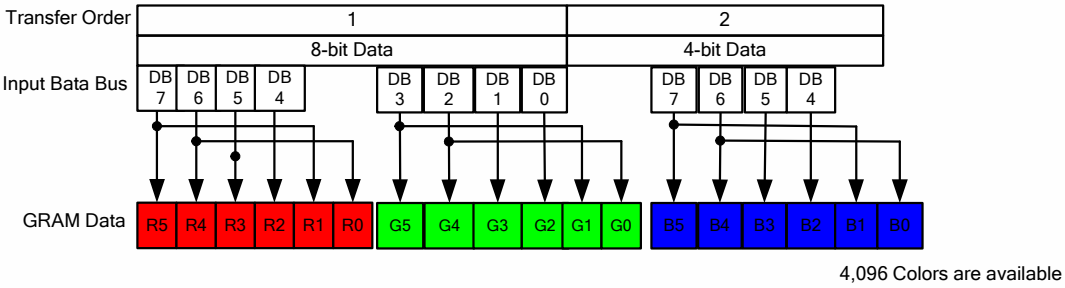


Figure 5. 21 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 12 Bit-Data Input (R17H=03h and"BS3, BS2, BS1, BS0"="0001")

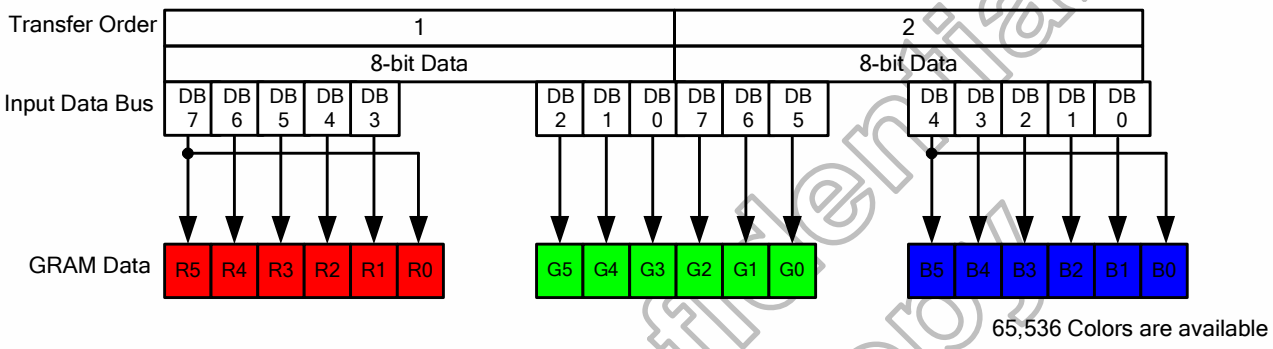


Figure 5. 22 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 16 Bit-Data Input (R17H=05h and "BS3, BS2, BS1, BS0"="0001")

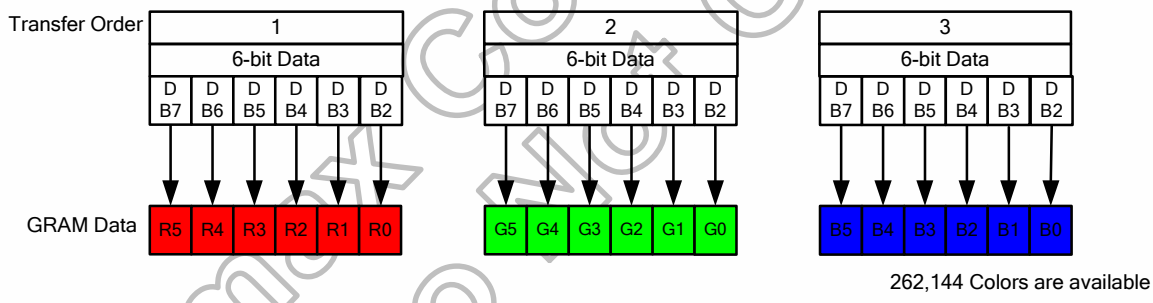


Figure 5. 23 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 18 Bit-Data Input (R17H=06h and "BS3, BS2, BS1, BS0"="0001")

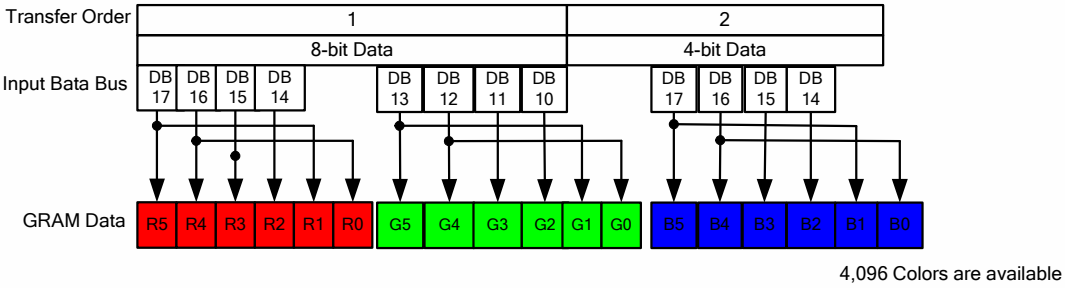


Figure 5. 24 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 12 Bit-Data Input (R17H=03h and"BS3, BS2, BS1, BS0"="0011")

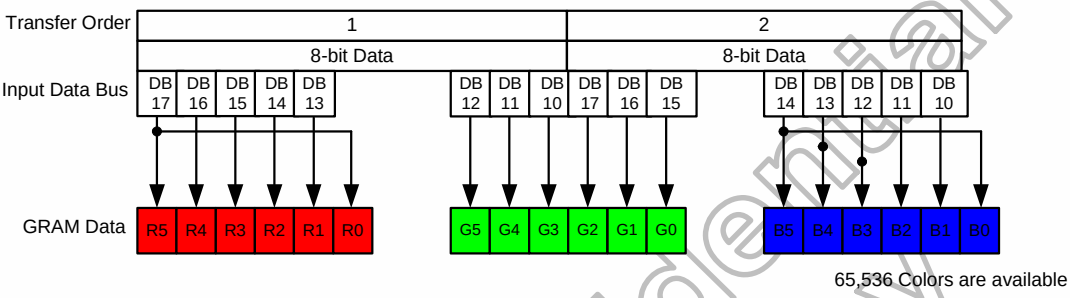


Figure 5. 25 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 16 Bit-Data Input (R17H=05h and "BS3, BS2, BS1, BS0"="0011")

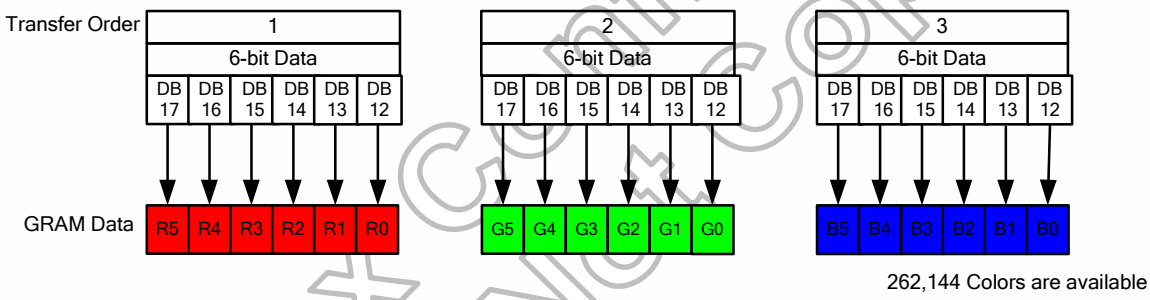


Figure 5. 26 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 18 Bit-Data Input (R17H=06h and "BS3, BS2, BS1, BS0"="0011")

MCU Data Color Coding for RAM data ***Read***

- Parallel 8-Bits Bus Interface type I (BS3,BS2,BS1,BS0="0001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixels/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5. 11 8-Bits Parallel Interface type I GRAM Read Table

- Parallel 16-Bits Bus Interface type I (BS3,BS2,BS1,BS0="0000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixels/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5. 12 16-Bits Parallel Interface type I GRAM Read Table

- Parallel 9-Bits Bus Interface type I (BS3,BS2,BS1,BS0="1001")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixels/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5. 13 9-Bits Parallel Interface type I GRAM Read Table

- Parallel 18-Bits Bus Interface type I (BS3,BS2,BS1,BS0="1000")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5. 14 18-Bits Parallel Interface type I GRAM Read Table

- Parallel 8-Bits Bus Interface type II (BS3,BS2,BS1,BS0="0011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x											262K-Color (1-pixels/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 5. 15 8-Bits Parallel Interface type II GRAM Read Table

- Parallel 16-Bits Bus Interface type II (BS3,BS2,BS1,BS0="0010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
Read Data Format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
		x	x	x	x	x	x	x	x		x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	262K-Color (2-pixels/ 3bytes)
	B5	B4	B3	B2	B1	B0	x	x	x	R5	R4	R3	R2	R1	R0	x	x	x	
	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	x	x	x	

Table 5. 16 16-Bits Parallel Interface type II GRAM Read Table

- Parallel 9-Bits Bus Interface type II (BS3,BS2,BS1,BS0="1011")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 5. 17 9-Bits Parallel Interface type II GRAM Read Table

- Parallel 18-Bits Bus Interface type II (BS3,BS2,BS1,BS0="1010")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22H**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5. 18 18-Bits Parallel Interface type II GRAM Read Table

5.1.3 Serial bus system interface

The HX8357-A supports two kinds serial bus interface in register-content mode by setting external pins “BS3, BS2, BS1” pins to “010” 3-wire serial interface and “BS3,BS2, BS1” pins to “110” 4-wire serial inteface. The serial bus system interface mode is enabled through the chip select line (CSX), and it is accessed via a control consisting of the serial input data (SDA), and the serial transfer clock signal (DCX_SCL).

5.1.3.1 3-wire serial interface

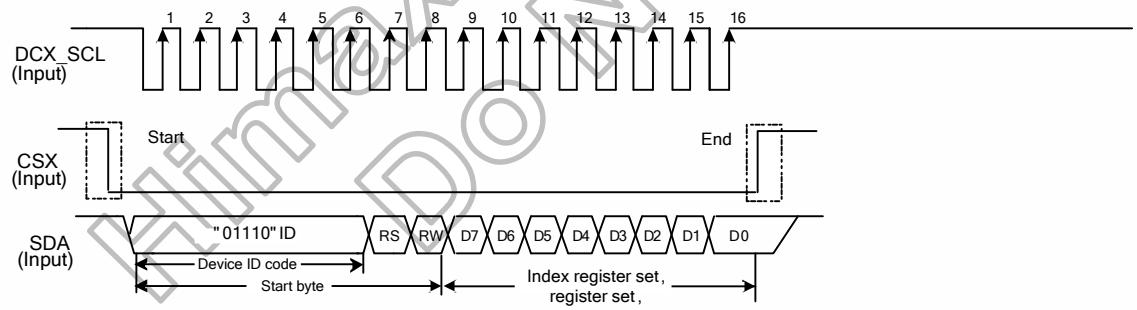
As the chip select signal (CSX) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code; register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin BS0 input as “ID”.

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to “0” when writing data to the index register or reading the status and it must be set to “1” when writing or reading a command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

RS	R/W	Function
0	0	Set index register
1	0	Writes Instruction or GRAM data
1	1	Reads command (Not support GRAM read)

Table 5. 19 The Function of RS and R/W Bit Bus

A) TransferTiming Format in Serial Bus Interface for Index Register or Register Wirte



B)Transfer Timing Format in Serial Bus Interface for Index Register or Register Read

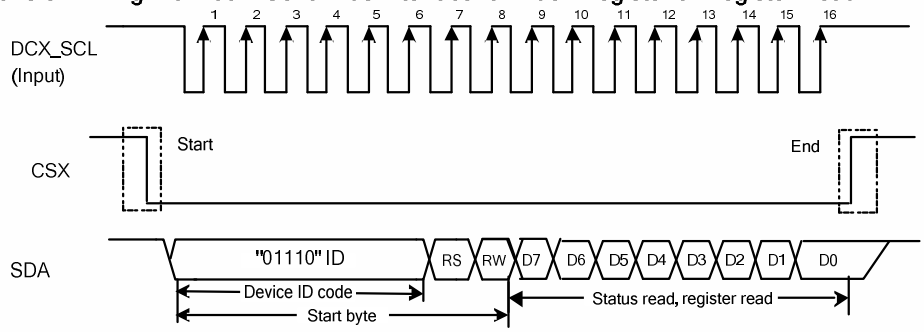
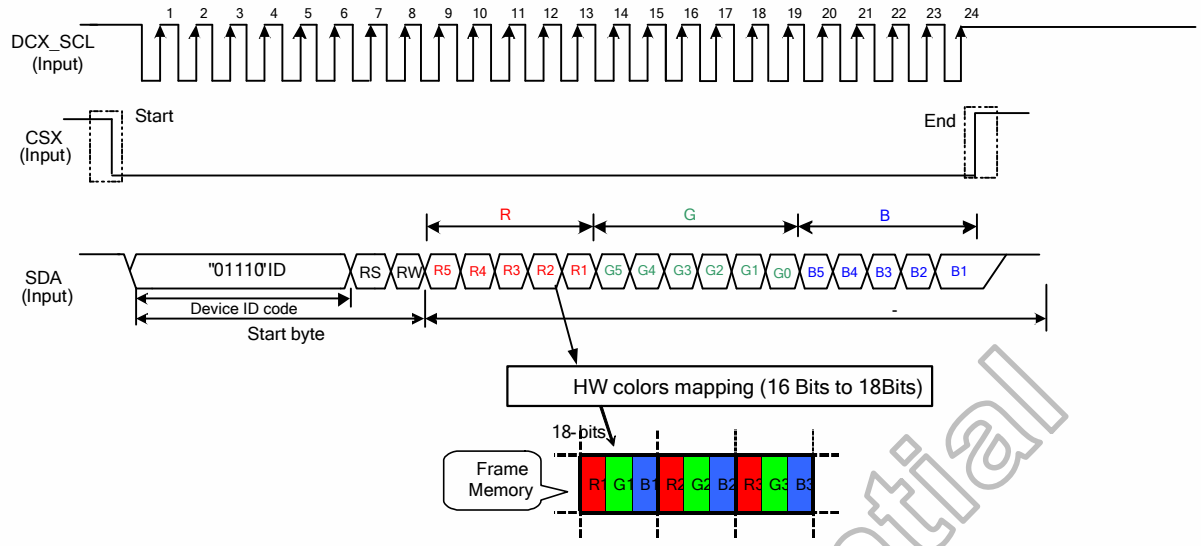


Figure 5. 27 Index Register Read/Write Timing in 3-wire Serial Bus System Interface

A)16-bit Data Transfer Timing Format in Serial Bus Interface for GRAM write (Index 17h= 05)



B)18-bit Data Transfer Timing Format in Serial Bus Interface for GRAM write (Index 17H=06)

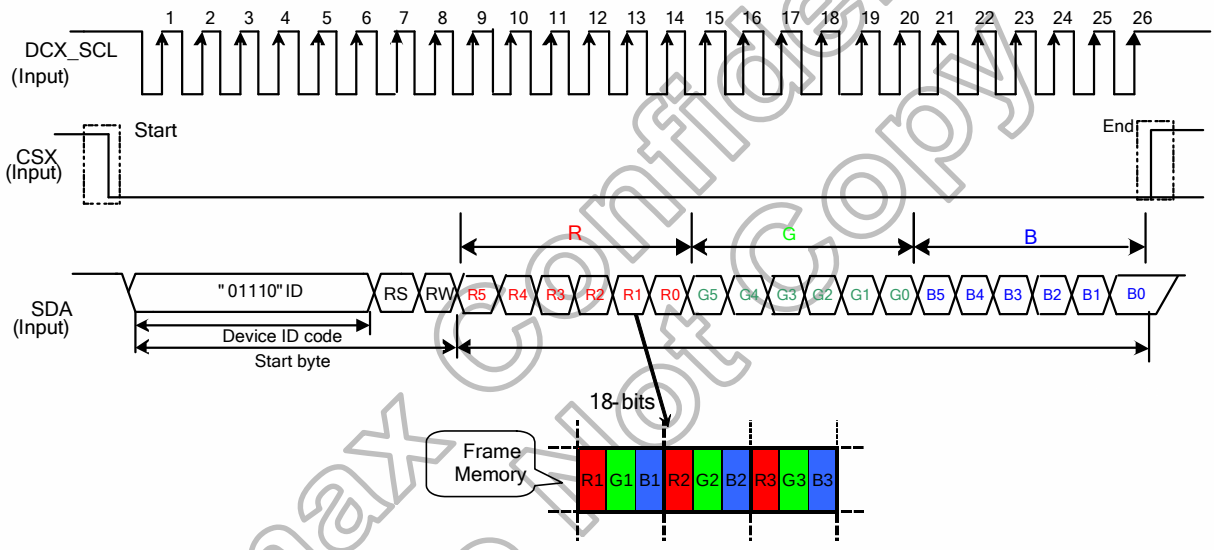


Figure 5. 28 Data Write Timing in 3-wire Serial Bus System Interface

5.1.3.1 4-wire serial interface

4-pin serial case, data packet contains just transmission byte and control bit DCX is transferred by WRX_DCX pin. If WRX_DCX is low, the transmission byte is command byte. If WRX_DCX is high, the transmission byte is stored to index register or GRAM. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, DCX_SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

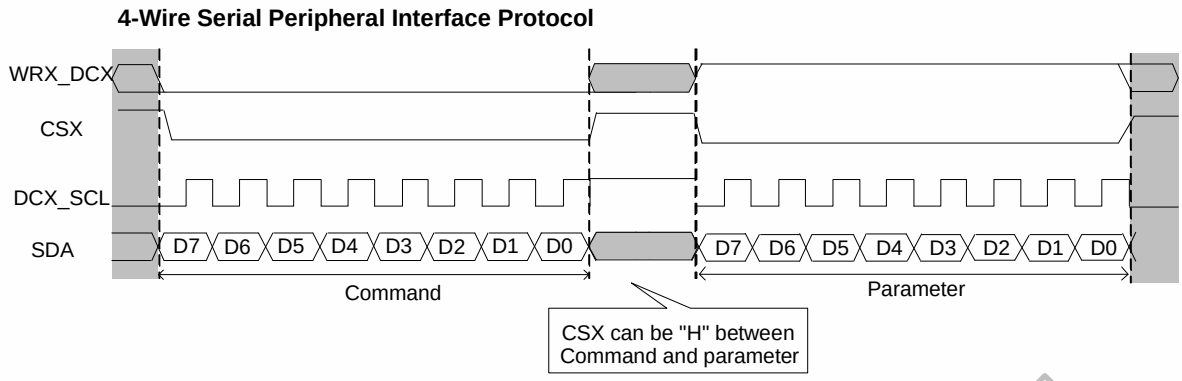


Figure 5. 29 Index Register Write Timing in 4-wire Serial Bus System Interface

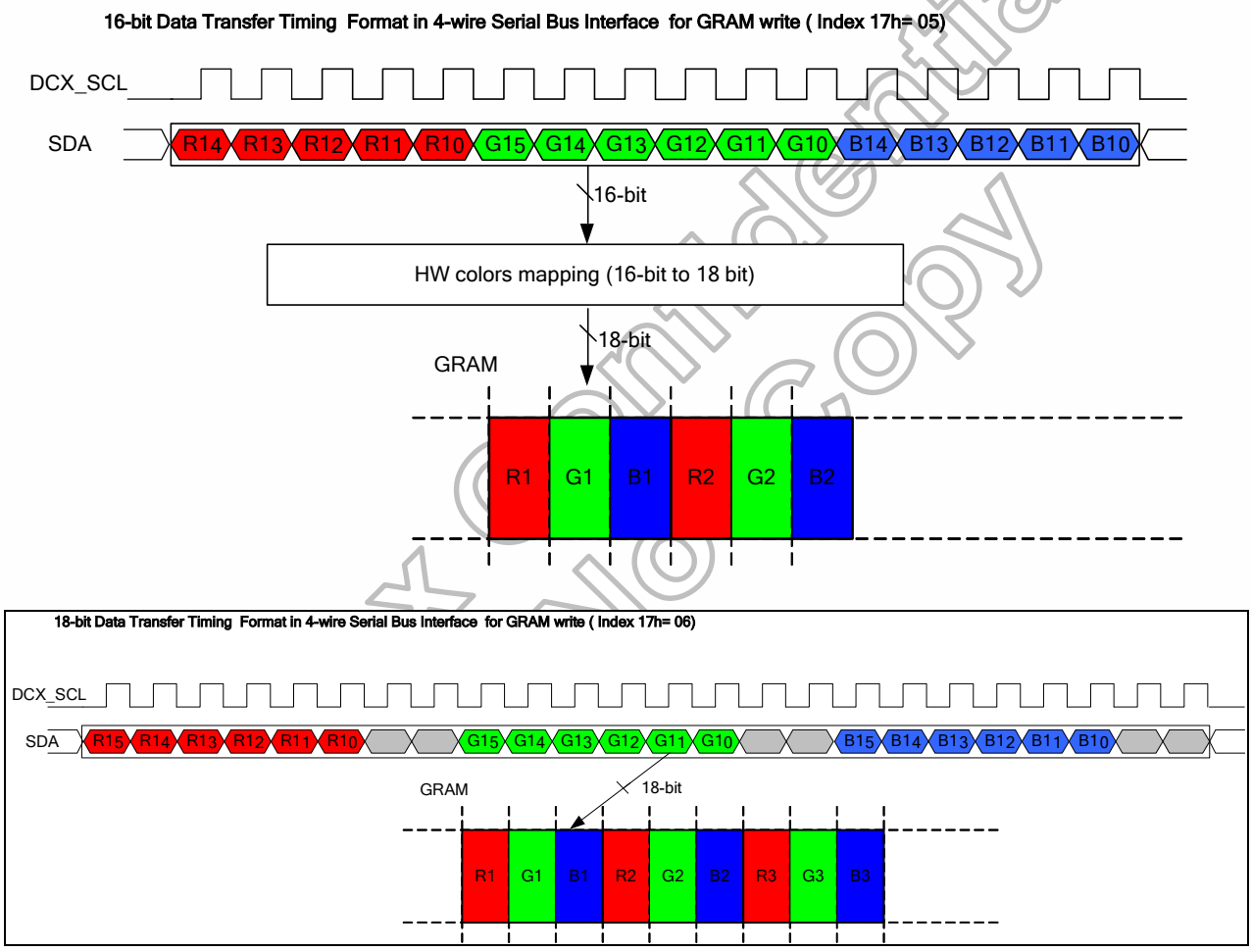


Figure 5. 30 Data Write Timing in 4-wire Serial Bus System Interface

5.2 RGB interface

The HX8357-A uses **RCM[1:0]='10' or '11' hardware setting to select RGB interface.** When after Power on Sequence, the RGB interface is activated. When RCM[1:0]='10' use VS, HS, DE, PCLK, DB17-0 parallel lines for the RGB interface (RGB mode 1). When RCM[1:0]='11' use VS, HS, PCLK, DB17-0 parallel lines for the RGB interface (RGB mode 2)

Pixel clock (PCLK) must be running all the time without stopping and it is used to entering VS, HS, DE and DB17-0 lines states when there is a rising edge of the PCLK.

In RGB interface mode 1, the valid display data is inputted in pixel unit via DB17-0 according to the high-level('H') of DE signal, and display operations are executed in synchronization with the frame synchronizing signal (VS), line synchronizing signal (HS) and pixel clock (PCLK). In RGB interface mode 2, the valid display data is inputted in pixel unit via DB17-0 according to the HBP setting of HS signal, and the VBP setting of VS. In these two RGB interface mode, the input display data is not written to GRAM and is displayed directly.

Vertical synchronization (VS) signal is used to tell when there is received a new frame of the display, and this is negative ('-', '0', low) active. Horizontal synchronization signal (HS) is used to tell when there is received a new line of the frame, and this is negative ('-', '0', low) active. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display, and this is positive ('+', '1', high) active. DB17-0 are used to tell what is the information of the image that is transferred on the display when DE='H'.

The pixel clock cycle is described in the following figure.

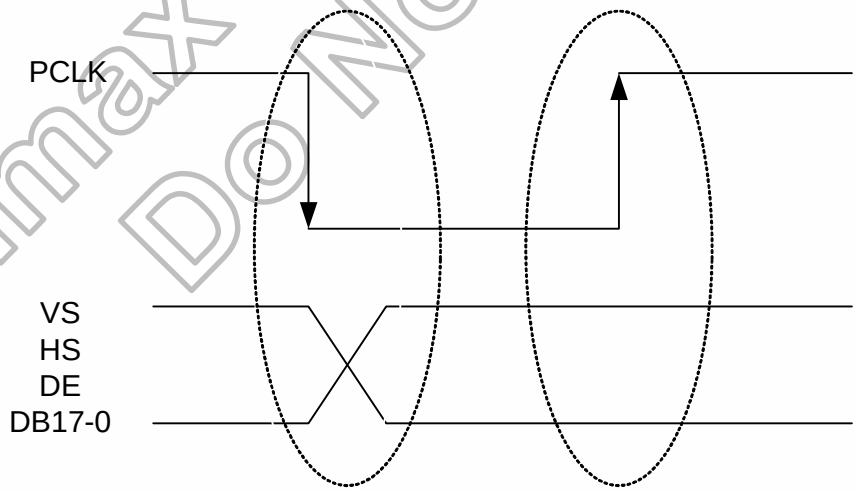


Figure 5. 31 DOTCLK Cycle

General timing diagram in RGB interface is as follow

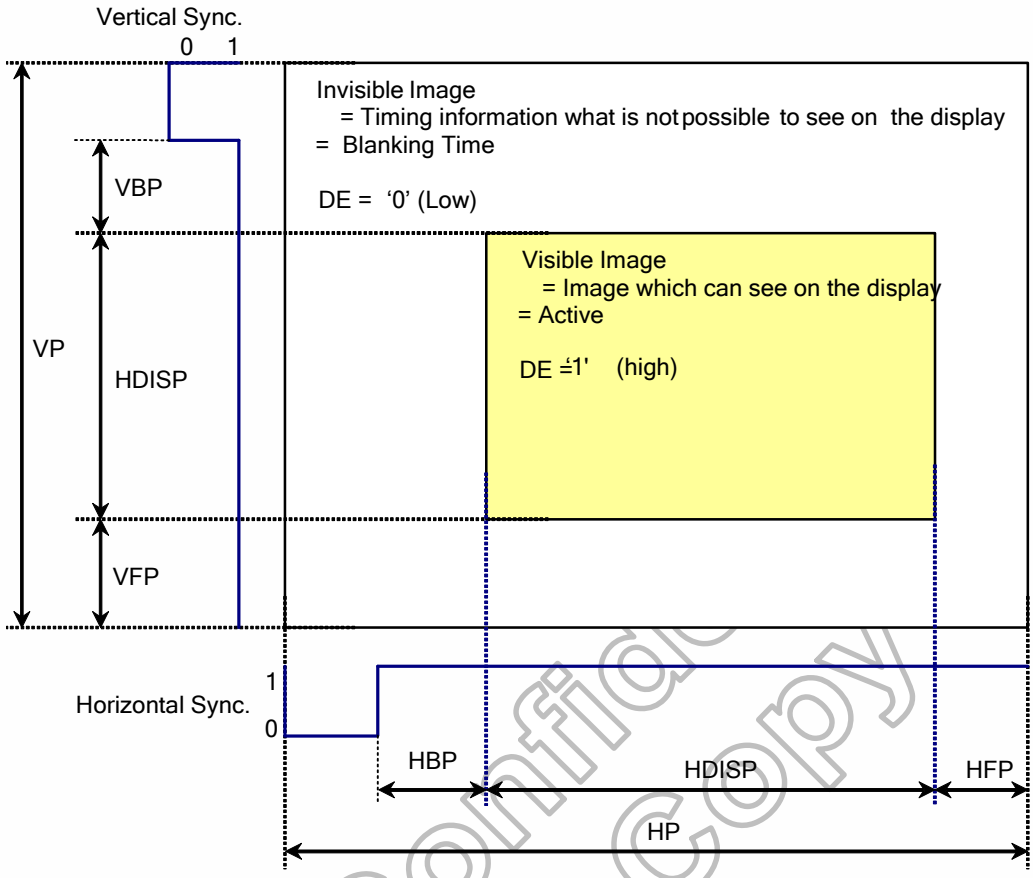
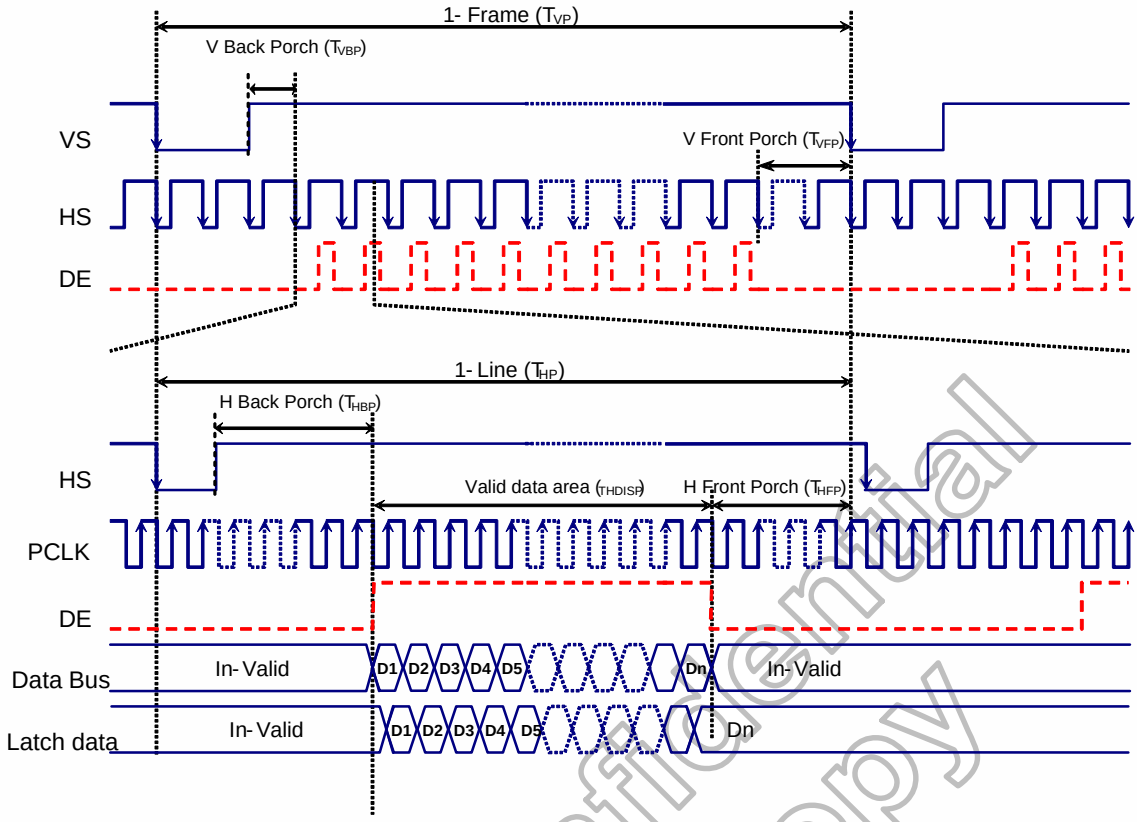


Figure 5. 32 RGB Interface Circuit Input Timing Diagram

The image information is correct on the display when the timings are in range on the interface. However, the image information will be incorrect on the display, when timings are out of the range on the RGB interface and the correct image information will be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range RGB interface timings.



Note: (1) RGB mode 2 doesn't need DE signal
(2) EPL='0', VSPL='0', HSPL='0' and DPL='0' of RGB interface control 2(R32H) command.

Figure 5. 33 RGB Mode timing Diagram

All 3-kinds of bus width can be available during RGB interface mode (selected by COLMOD (17H) command for 6-bits, 16-bits and 18-bits data width)

17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
50h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	16-bits data
60h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bits data
17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
E0h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bits data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note: (1) When 17H=”E0h”, 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(2) Only 17H= “50h”,”60h”, “E0h” are valid on RGB I/F, Others are invalid.
(3) ‘x’ don’t care, but need to set IOVCC or VSSD level.

Table 5. 20 RGB interface Bus Width Set Table

RGB interface mode

RGB I/F Mode	PCLK	DE	VS	HS	Video Data bus DB[B:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

In RGB Mode 1 (RCM1, RCM0 = “10”), writing data to display is done by PCLK and Video Data Bus (DB[17:0]), when DE is high state. The external synchronization signals (PCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer PCLK, VS, HS and DE signals to driver.

In RGB Mode 2 (RCM1, RCM0 = “11”), blanking porch setting of VS and HS signals are defined by RGB interface control 1 (R31h) command. DE pin is not used.

5.2.1 Color order on RGB interface

The meaning of the pixel information, when there are used 3 components/pixel (Red, Green and Blue) on RGB interface, is describing on the following table:

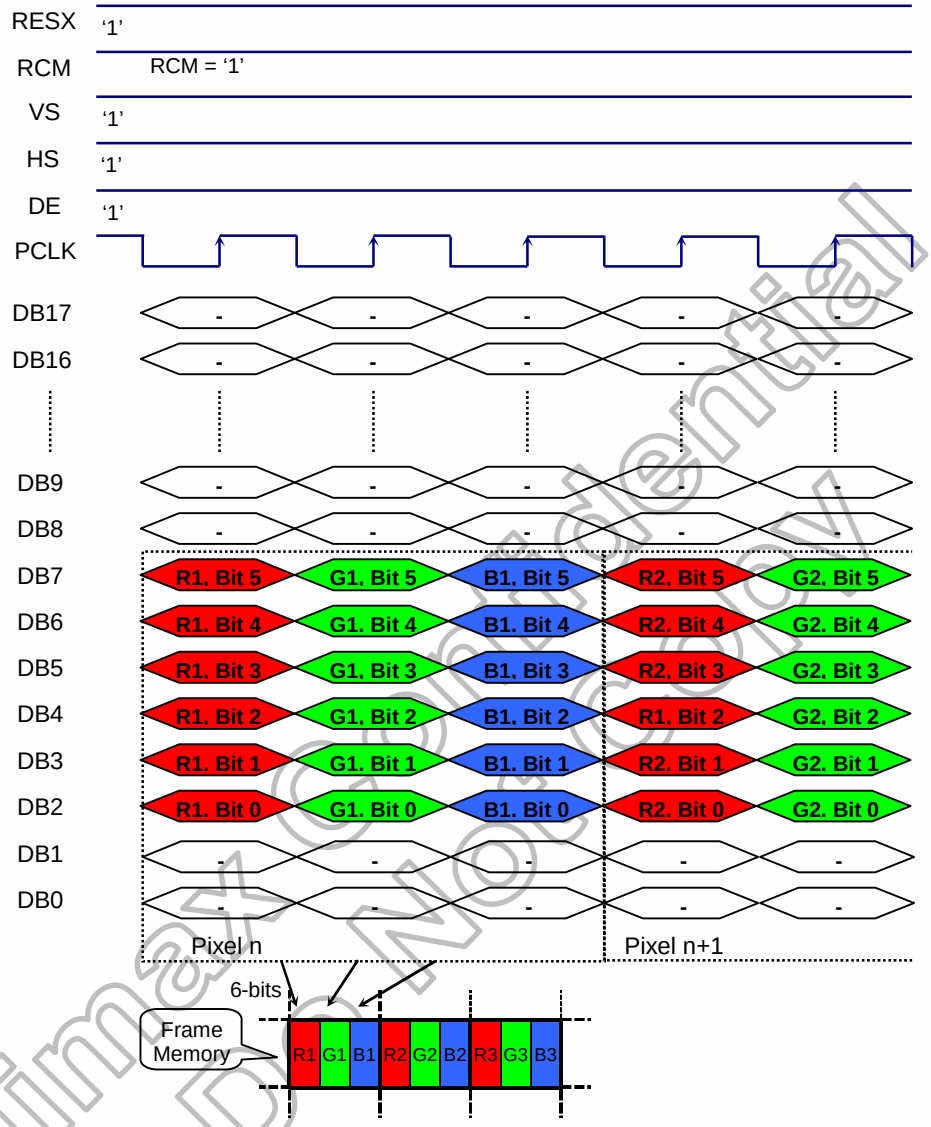
Pixel Color	R Component	G Component	B Component
Black	All bits are 0	All bits are 0	All bits are 0
Blue	All bits are 0	All bits are 0	All bits are 1
Green	All bits are 0	All bits are 1	All bits are 0
Cyan	All bits are 0	All bits are 1	All bits are 1
Red	All bits are 1	All bits are 0	All bits are 0
Magenta	All bits are 1	All bits are 0	All bits are 1
Yellow	All bits are 1	All bits are 1	All bits are 0
White	All bits are 1	All bits are 1	All bits are 1

Note: There are only defined main colors on this table - Not all gray levels of colors.

Table 5. 21 Meaning of the Pixel Information for Main Colors on RGB Interface

5.2.2 RGB data color coding

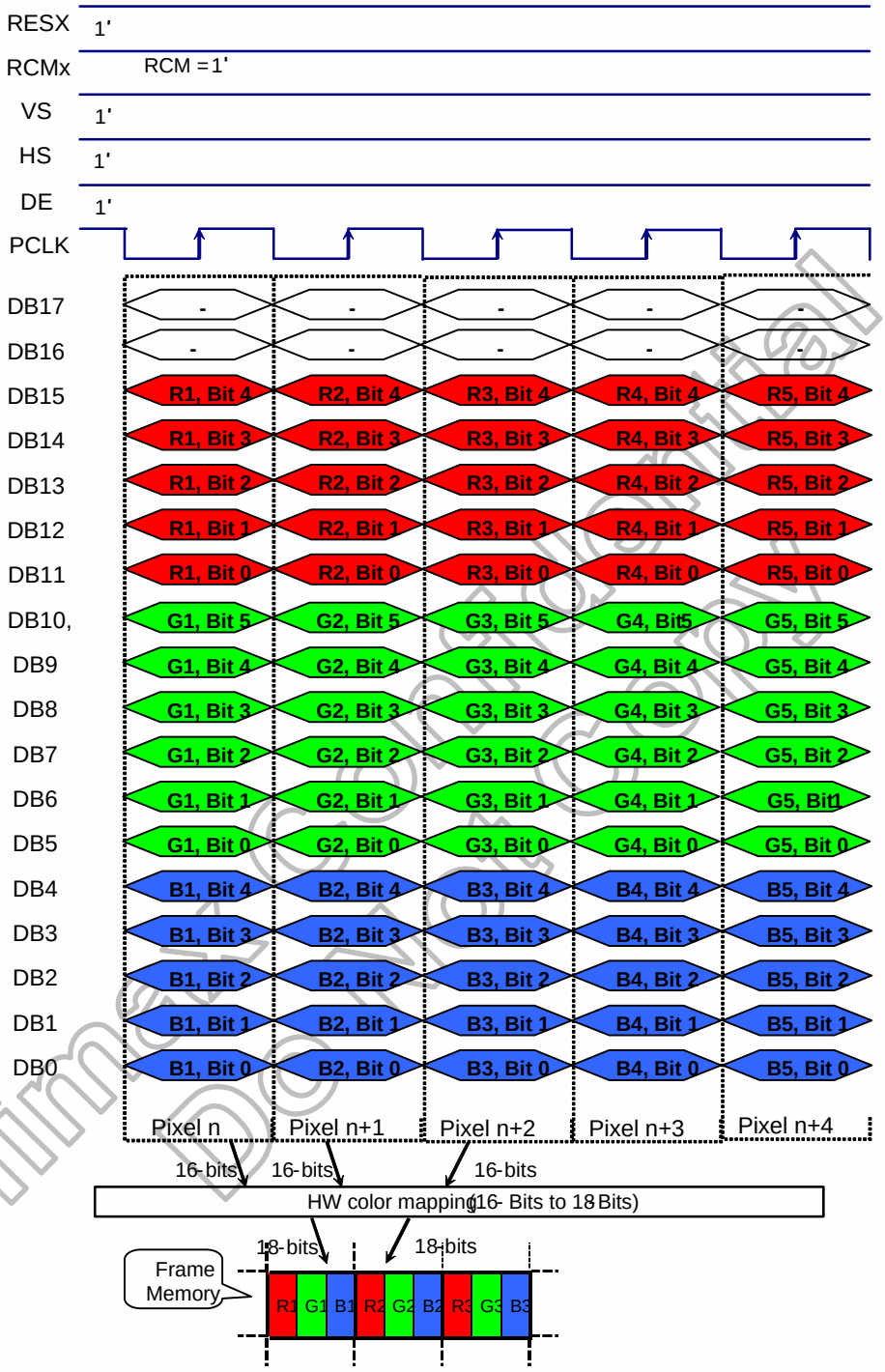
18-bits/pixel Colors Order on 6-bits Data width RGB Interface (RGB 6-6-6-bits input).
There are 1 pixel (3 sub-pixels) per 3 bytes, 262K-colors, 17H="E0h"



Note: (1) The data order is as follows, MSB=DB7, LSB=DB0 and picture data is MSB=Bit7, LSB=Bit0 for Red, Green and Blue data. (3-trandfer data one pixel)
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5. 34 RGB 18-bits/pixel on 6-bits Data width

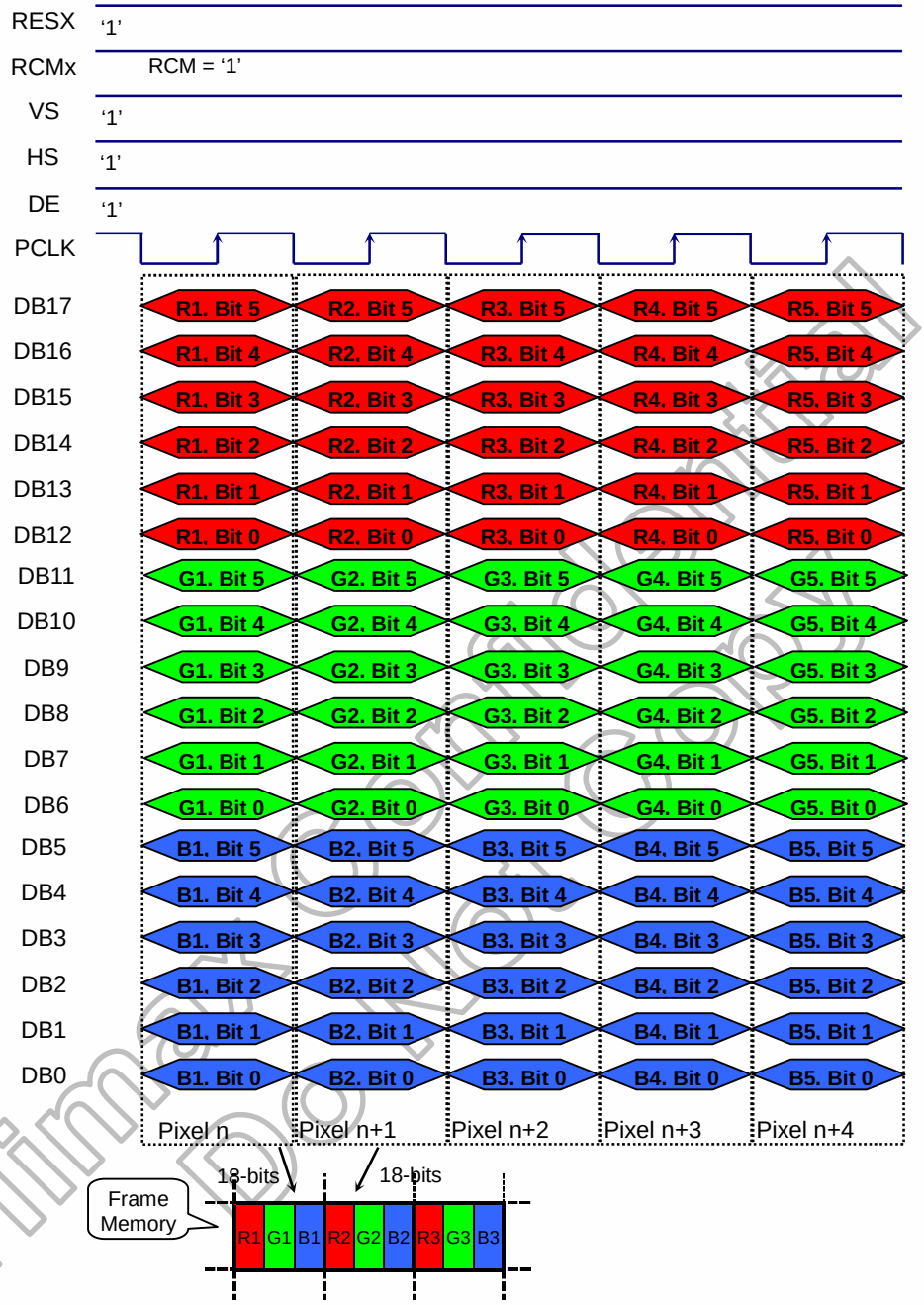
16-bits/pixel Colors Order on the 16-bits Data width RGB Interface (RGB 5-6-5-bits input).
There are 1 pixel (3 sub-pixels) per 1 bytes, 65K-colors, 17H="50h"



Note: (1) The data order is as follows, MSB=DB17, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5. 35 RGB 16-bits/pixel on 16-bits Data width

18-bits/pixel Colors Order on the 18-bits Data width RGB Interface (RGB 6-6-6-bits input). There are 1 pixel (3 sub-pixels) per 1 bytes, 262K-colors, 17H="60h"



Note: (1) The data order is as follows, MSB=DB17, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Red, Green and Blue data.
(2) '-' Don't care, but need to set IOVCC or VSSD level.

Figure 5. 36 RGB 18-bits/pixel on 18-bits Data width

5.2.3 MDDI interface (mobile display digital interface)

5.2.3.1 Introduction of MDDI

The HX8357-A support MDDI, which is a differential serial interface with high-speed, low voltage swing characteristics. Both command and display image data can be transferred by MDDI. The devices connected by Data and STB link are host and client part.

Host transfer data to client in “forward” direction, client transfer data to host in “reverse” direction. The Data line is Dual direction, both command and image data are all send through the Data line. The STB line send strobe signal from host to client.

Data transferred in MDDI link are encoded as packet type.

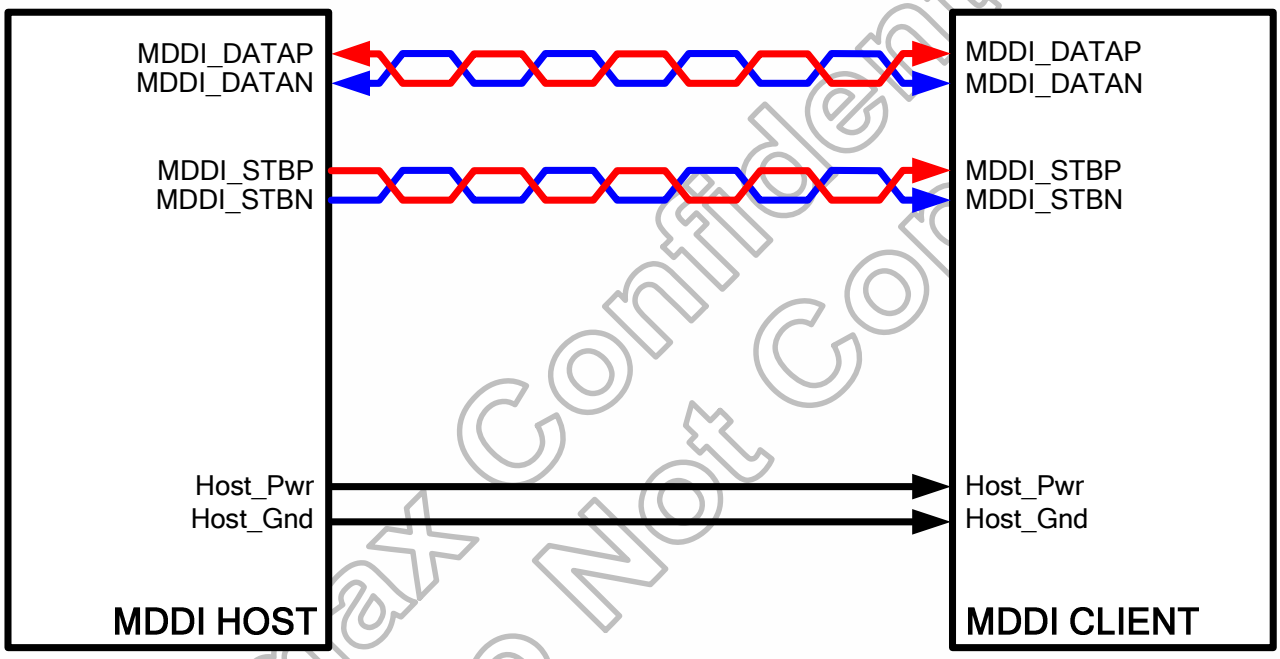


Figure 5. 37 Physical Connection of MDDI Host and Client

5.2.3.2 Terminology

The devices connected by the MDDI link are called the host and client. Data going from the host to the client travels in the ***forward*** direction, and data from the client to the host travels in the ***reverse*** direction.

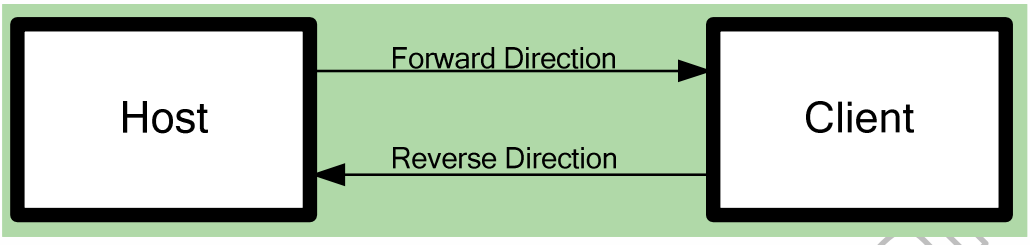


Figure 5. 38 MDDI Terminology

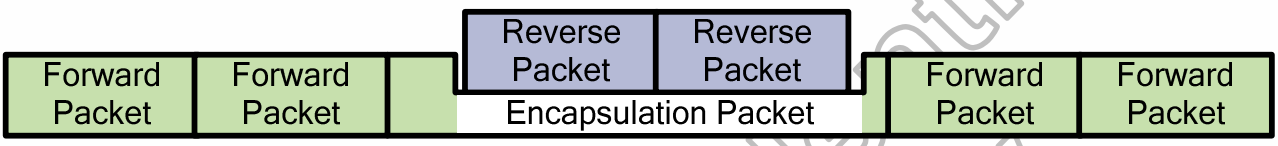


Figure 5. 39 Example of Bi-Directional MDDI Communication

5.2.3.3 Data-STB encoding

Data is encoded using a DATA-STB format. DATA is carried over a bi-directional differential cable, while STB is carried over a unidirectional differential cable driven only by the host. Figure 5.39 illustrates how the data sequence “1110001011” is transmitted using DATA-STB encoding.

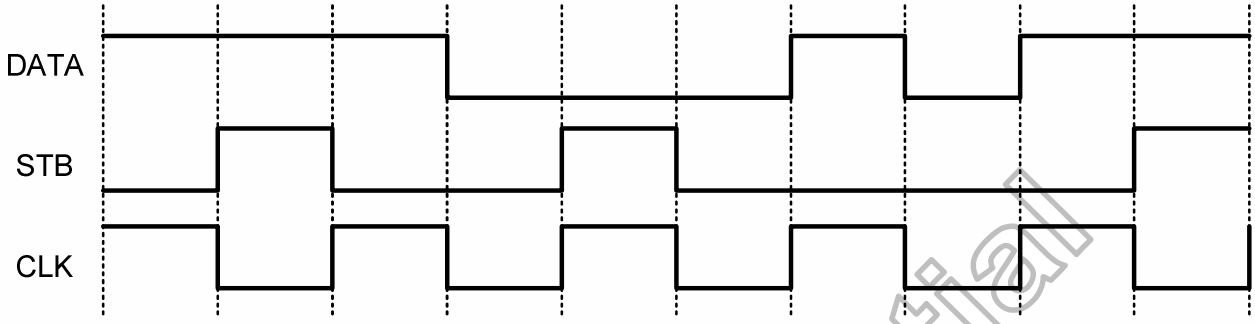


Figure 5. 40 Data-STB Encoding

Figure 5.40 shows a sample circuit to generate DATA and STB from input data, and them recover the input data from DATA and STB.

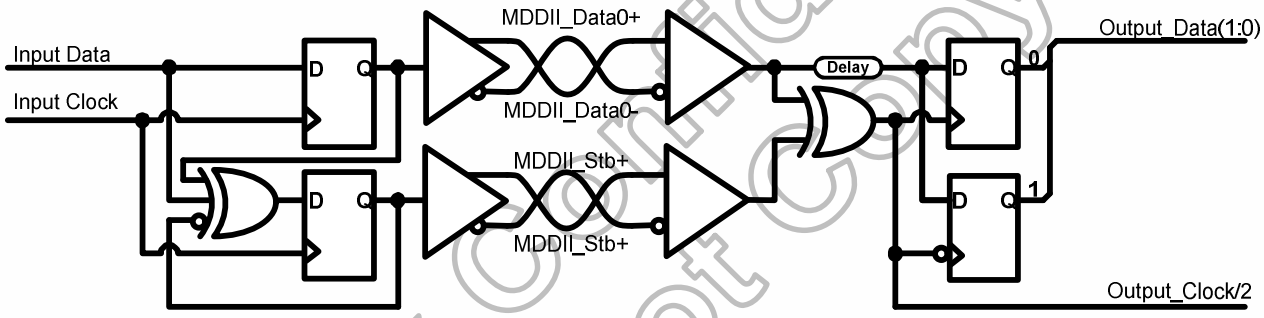


Figure 5. 41 Data / STB Generation & Recovery Circuit

5.2.3.4 MDDI data/STB

The Data (MDP/MDN) and STB (MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets the MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

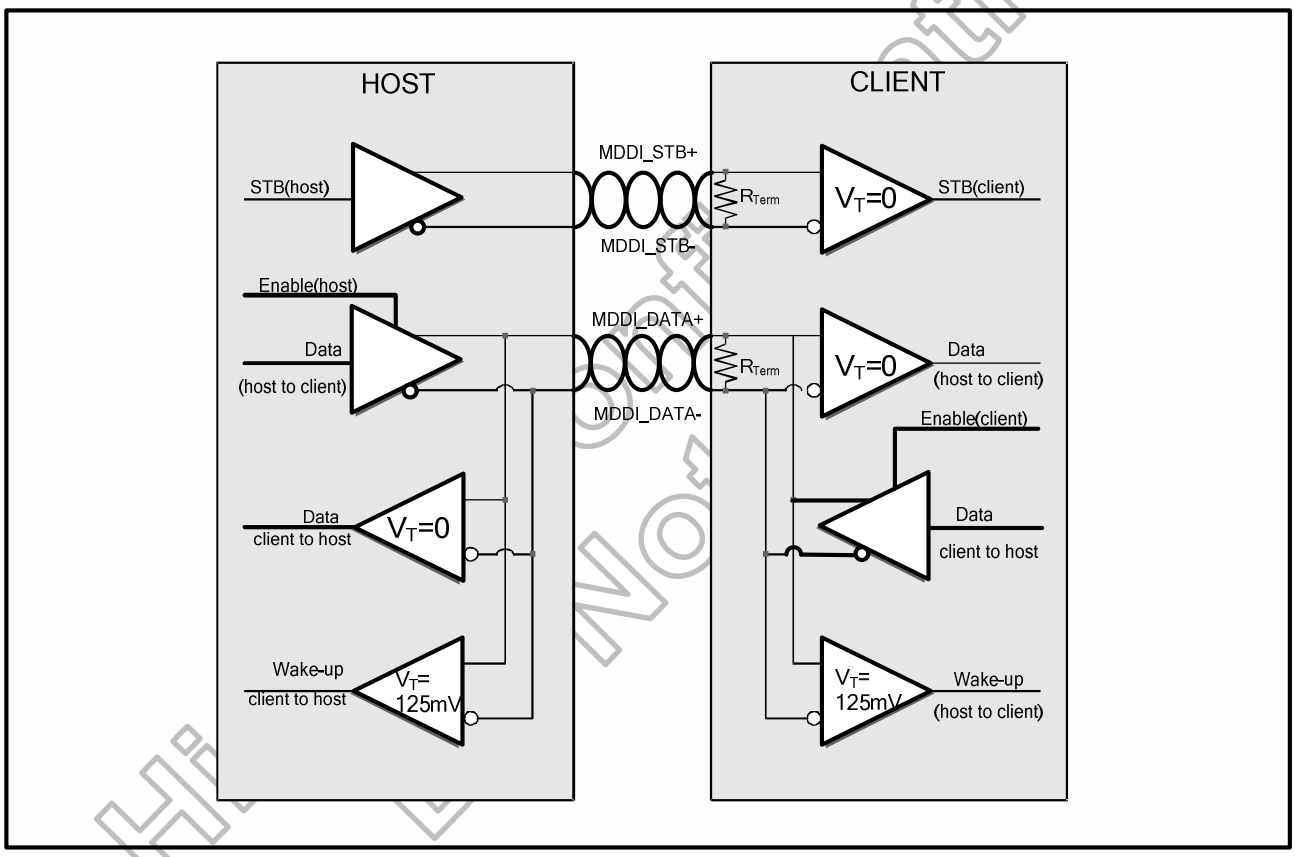


Figure 5. 42 Differential Connection between Host and Client

5.2.3.5 MDDI packet

Data transmitted over the MDDI link is grouped into packets. Several packets format is supported in HX8357-A. Most packets are in forward direction, transferred from host to client; but reverse encapsulation packet is in reverse direction, transferred from MDDI client to host. A number of packets, started by sub-frame header packet, construct one sub frame.

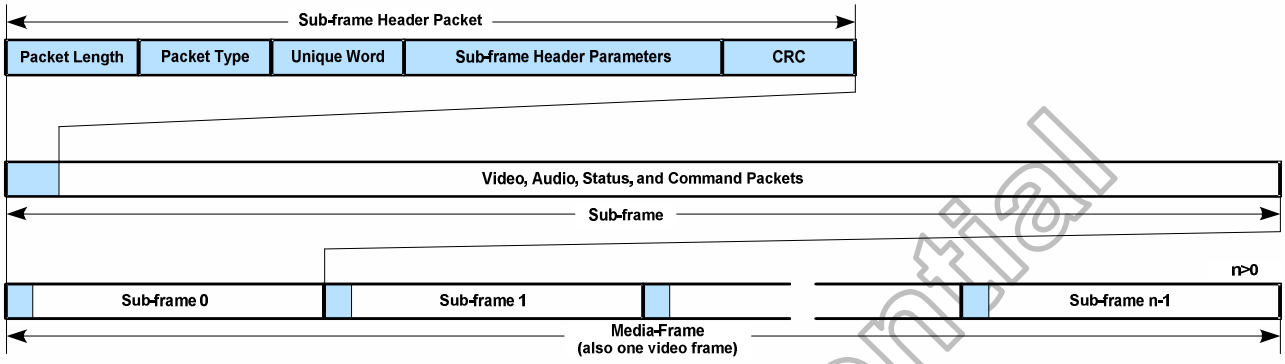


Figure 5. 43 MDDI Packet Structure

Refer to MDDI frame structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frames make up a media-frame.

HX8357-A support 9 types of packets, which described in the table below.

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward

Table 5. 22 List of Supported MDDI Packet

Sub-frame header packet

Packet Length	Packet type =0x3bffh	Unique word =0x005a	Reserved 1	Sub-frame length	Protocol Version	Sub-frame Count	Media-frame Count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 0x3bffh for sub-frame header packet
unique word : link packet type to form a 32-bit unique word for good autocorrelation.
reserved 1 : not used(all zero)
sub-frame length : specifies number of bytes per sub-frame
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packet.
media frame count : specifies number of media frame
CRC : error check

Register access packet

Packet Length	Packet type =146	bClient ID	Read/Write Info	Register Address	Parameter CRC	Register Data list	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	4 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 146(decimal) for register access packet
bClient ID : set all zero
Read/Write Info : when write value to register, bit[15:14] = “00”
when request data from register, bit[15:14]=“10”
when data from register, bit[15:14] = “11”
bit[13:0] : 00_0000_0000_0001
register address : Register address is set written here.
parameter CRC : To error check from packet length to register address
register data list : Paramter data is written here.
register data CRC : To error check register data list.

Video stream packet

Packet Length	Packet type =16	bClient ID	video data format descriptor	pixel data attributes	X left edge	Y top edge	X right edge	Y bottom dedge	X start	Y start
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	packet length - 26 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 16 (decimal) for register access packet
bClient ID : set all zero
video data format descriptor : bits[15:13]=010, raw RGB format (fixed value)
bit[12]=1,only packed type is available (fixed value)
bits[11:0]=0110_0110_0110, 18bit pixel
bits[11:0]=0101_0110_0101, 16bit pixel
: bits[1:0]=11, displayed both eyes (fixed value)
pixel data attributes : bit[5]=1, X left edge .. Y start is not defined.(fixed value)
others are all zero
X left edge : X coordinate of the left edge of the active window filled by the Pixel Data field.
X top edge : Y coordinate of the top edge of the active window filled by the Pixel Data field
X right edge : X coordinate of the right edge of the active window filled by the Pixel Data field.
Y bottom edge : Y coordinate of the bottom edge of the active window filled by the Pixel Data field.
X start : X coordinate of the first pixel in the Pixel Data field below
Y start : X coordinate of the first pixel in the Pixel Data field below
Pixel count : Write number of pixel
Patameter CRC : To error check from packet length to pixel count
pixel data : pixel data info. Number of pixel data must not be over 65509
pixel data CRC : To pixel data error check.

Filler packet

Packet Length	Packet type =0	filler bytes (all zero)	CRC
2 bytes	2 bytes	packet length – 4 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 16 (decimal) for register access packet
filler bytes : set to all zero (The size is under packet length available)
CRC : To error check

Link shutdown packet

Packet Length	Packet type =69	CRC	All zeros
2 bytes	2 bytes	2 bytes	16 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 16 (decimal) for register access packet
CRC : To error check
All zeros : write all zero (size is 16 bytes, because MDDI for HX83xx is type 1)

Fixed Value

For more information about MDDI packet refer to VESA MDDI spec

5.2.3.6 Tearing-iess display

When you use the HX8357-A, it is important to match timing at which to write data with timing at which to read data. If the two types of timing not match each other, tearing effect will occur. IN HX8357-A, two ways to prevent display-tearing phenomenon are supported.

The first case is such that the speed at which to write data is lower than the speed at which to read data. Under this situation, the writing data speed not critical, but longer period during transferring data will cause a larger current consumption in the interface. The system, therefore, selects a wider period during writing data.

The second case is such that the data writing speed is higher than the data reading speed. Under that situation, the data updating speed becomes very high, but the transfer period can be shortened. Current consumption by the interface can be minimized, but higher-speed data is required. Most important is to prevent contention of updating data and scanning display data.

Figure below provides an example of preventing tearing effects.

(1) Panel read is faster than MPU write

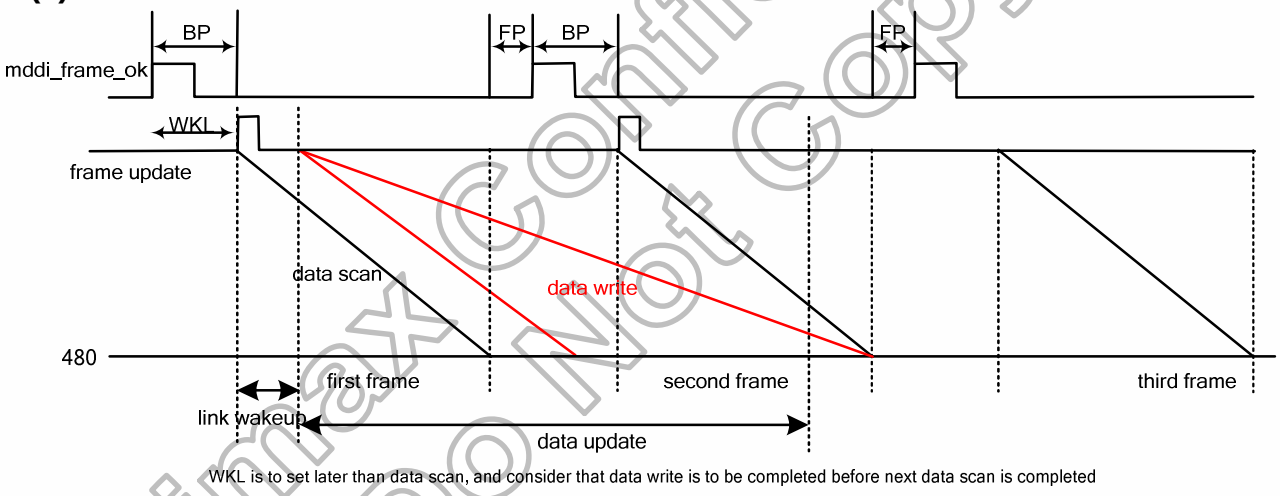


Figure 5. 44 Panel Read is faster than MPU Write

Tearing-less display: The Panel read speed is faster than MPU Write.

(2) Panel read is slower than MPU write

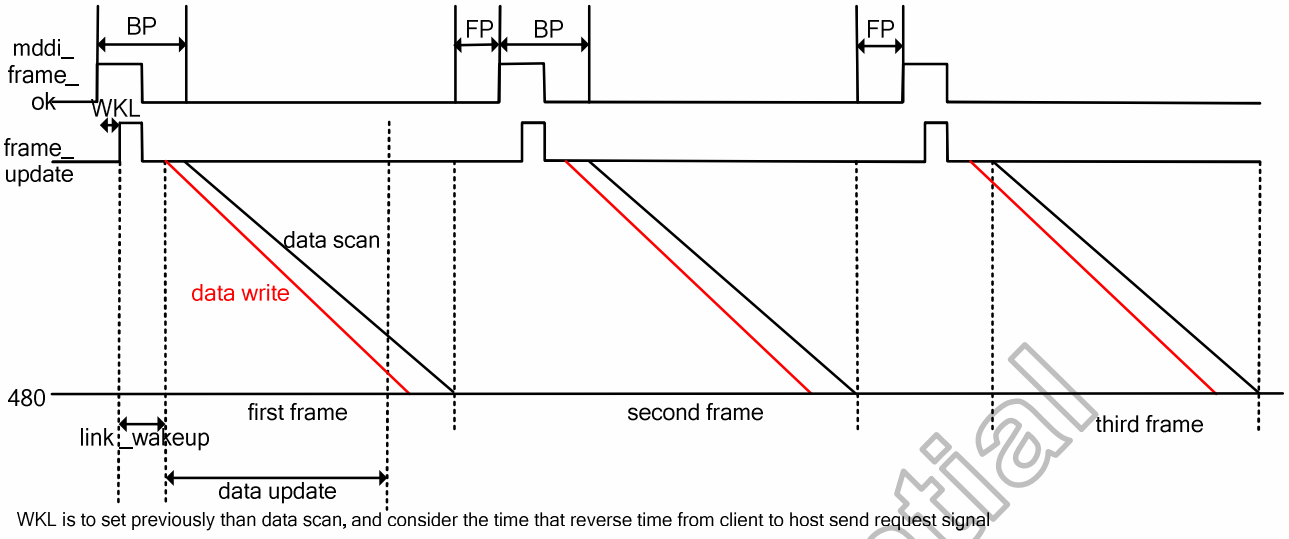


Figure 5. 45 Panel Read is slower than MPU Write

Tearing-less display: The Panel read speed is slower than MPU Write.

5.2.3.7 Hibernation / wake up

For reducing current consumption, HX8357-A support hibernation mode. The MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force the MDDI link into hibernation frequently to reduce power consumption. In hibernation mode, hi-speed drivers and receivers are disabled and low-speed & low-power receivers are enabled to detect wake-up sequence.

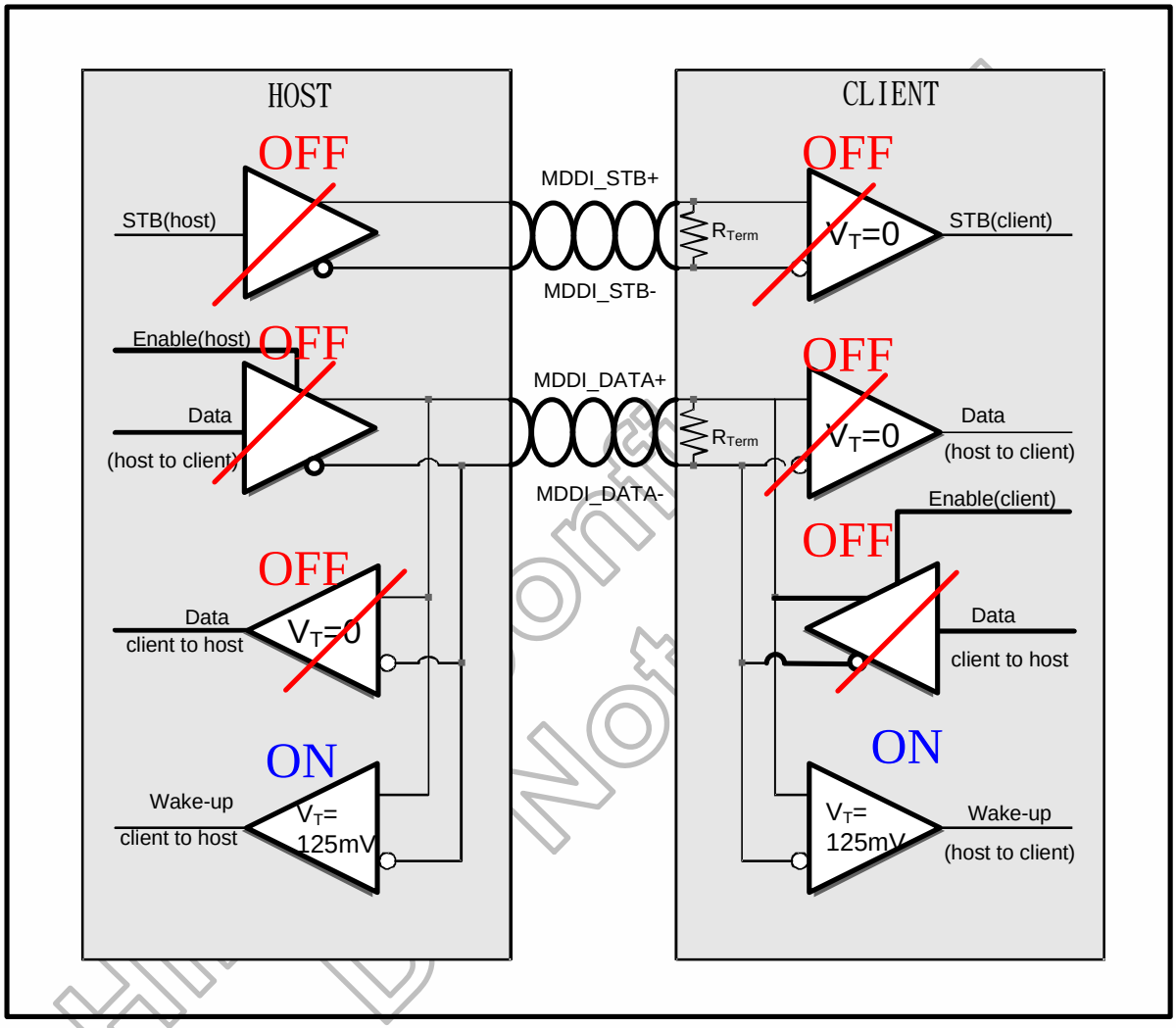


Figure 5. 46 MDDI Transceiver / Receiver State in Hibernation

When the link wakes up from hibernation the host and client exchange a sequence of pulses. These pulsed can be detected using low-speed line receivers that consume only a fraction of the current as the differential receivers required to receive the signals at the maximum link operating speed.

Either the host or client can wake up the link, which are supported in HX8357-A: Host-Initial Wakeup & Client-Initial Wakeup.

5.2.3.8 MDDI link wakeup sequence

Figure 5.50 below provide a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The labeled events are:

Host-initiated wake-up:

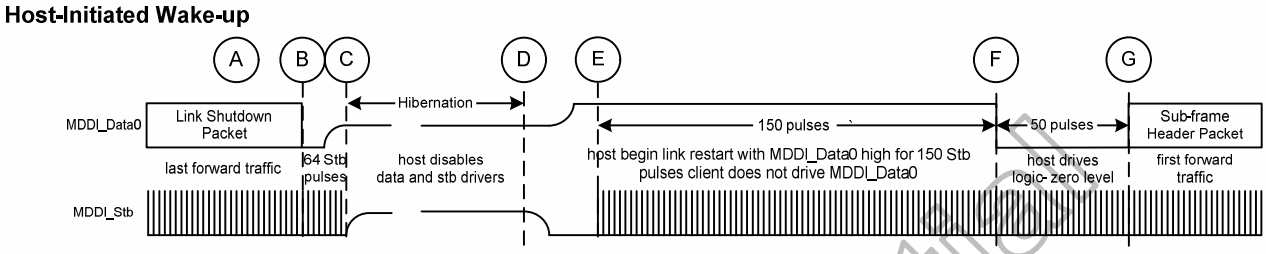


Figure 5. 47 Host-initiated Link Wakeup Sequence

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.
B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.
C. The host enters the low-power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state. It is also allowable for MDDI_Stb to be driven to a logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.
D. After a while, the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.
E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic-zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.
F. The host drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.
G. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point G.

An example of a typical client-initiated service request event with no contention is illustrated in below figure 5.51. The labeled events are：

Client-initiated wake-up:

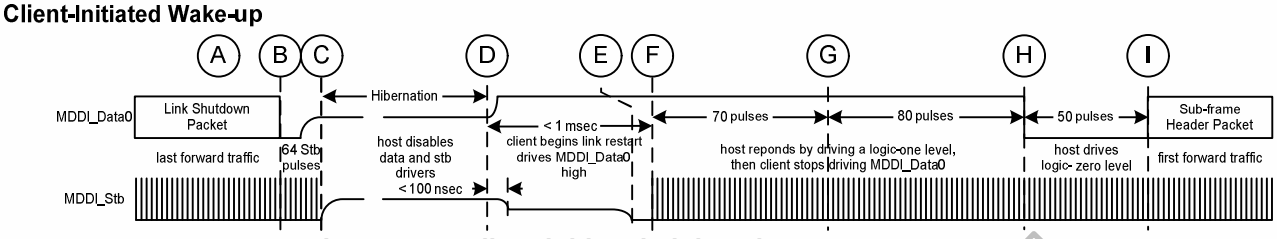


Figure 5. 48 Client-initiated Link Wake-up Sequence

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling its MDDI_Data0 and MDDI_Stb driver outputs. It is also allowable for MDDI_Stb to be driven to a logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

D. After a while, the client begins the link restart sequence by enabling the MDDI_Stb receiver and also enabling an offset in its MDDI_Stb receiver to guarantee the state of the received version of MDDI_Stb is a logic-zero level in the client before the host enables its MDDI_Stb driver. The client will need to enable the offset in MDDI_Stb immediately before enabling its MDDI_Stb receiver to ensure that the MDDI_Stb receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagating into the client. After that, the client enables its MDDI_Data0 driver while driving MDDI_Data0 to a logic-one level. It is allowed for MDDI_Data0 and MDDI_Stb to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_Stb differential receiver is less than 200 nsec.

E. Within 1 msec the host recognizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid fullydriven logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.

F. The host begins outputting pulses on MDDI_Stb and shall keep MDDI_Data0 at a logic-one level for a total duration of 150 MDDI_Stb pulses through point H. The host generates MDDI_Stb in a manner consistent with sending a logic-zero level on MDDI_Data0. When the client recognizes the first pulse on MDDI_Stb it shall disable the offset in its MDDI_Stb receiver.

G. The client continues to drive MDDI_Data0 to a logic-one level for 70 MDDI_Stb pulses, and the client disables its MDDI_Data0 driver at point G. The host continues to drive MDDI_Data0 to a logic-one level for a duration of 80 additional MDDI_Stb pulses, and at point H drives MDDI_Data0 to a logic-zero level.

H. The host drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.

I. After asserting MDDI_Data0 to a logic-zero level and driving MDDI_Stb for a duration of 50 MDDI_Stb pulses the host begins to transmit data on the forward link at point I by sending a Sub-frame Header Packet. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.

5.2.3.9 Sequence for the client to wake up the link

The HX8357-A supports two link wake up mode for the client based on VSYNC. Only in hibernation mode, the client can wake up the link. User should configure the register for a wakeup before link is shut down.

Link wakeup based on VSYNC

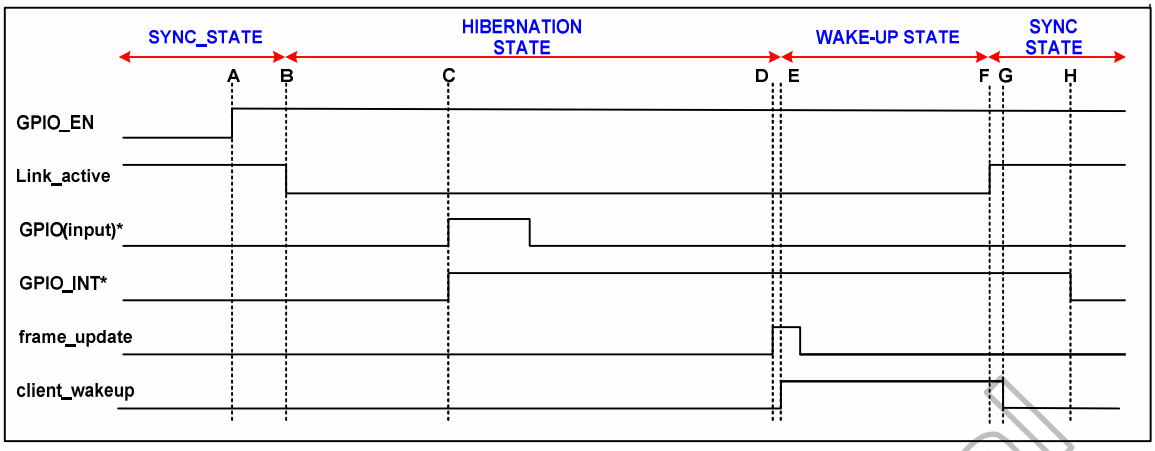
When all display data finishes being displayed in display mode, a data request is sent to the MDDI host for new video data. The MDDI link is normally in hibernation mode for reducing power dissipation by the interface. Before the on-chip RAM is updated, the MDDI link must be woken up. In that case, you can use a link wakeup by the client as a data request. When the link wakeup register VWAKE_EN is set in VSYNC mode, the link is woken up by the client synchronously with a vertical sync signal generated in the HX8357-A. If the interface speed and the wakeup period are well known, link wakeup based on VSYNC can be used to attain consistent display.

Figure below shows detailed timing on a link wakeup based on VSYNC.

GPIO based link wake-up

In VSYNC-based link wake-up, wake-up enable register setting prior to link shut-down. GPIO based Link wake-up is enabled by interrupt from outside of the IC. For GPIO based link wake-up, GPIO interrupt enable and GPIO PAD mode (to input mode) setting must be set. Once HX8357-A receive interrupt, internal GPIO base link wake-up flag set to high, and the following procedure is similar to that of VSYNC based link wake-up.

The following figure shows detailed timing for GPIO based link wake-up.



The Detailed descriptions for labeled events are as follows:

A. Host send register access packet to sets GPIO clear interrupt register to disable clear interrupt (R6Fh:GPIO_CLR) and GPIO interrupt enable register (R6Dh: GPIO_EN) for a particular GPIO.

B. After host sending all data, Link goes into hibernation (and link_active goes low) .

C. GPIO input goes high, and the GPIO interrupt (GPIO_INT) is latched.

D. Frame_update signal goes high indicating that the display has wrapped around. Link wake-up point can be set using WKF and WKL (R68h) registers.

E. Client_wakeup signal of the MDDI client goes high to start the client initiated link wake-up.

F. Link_active goes high after the host make link leaving hibernation.

G. After link wake-up, client_wakeup signal is reset to low.

H. MDDI host clears the interrupt by writing '0' to the register with the bit set for that particular interrupt (GPCLR: R6Fh). Between point G and H the host will have read the GPIO_INT values to see what interrupts are active.

GPIO control

The HX8357-A offers 8 GPIO that can be used as input or output independently. Some application or device on the upper clamshell needs several control signals which are supplied by base band modem or application processor directly. If number of application on the upper clamshell increases, also control signals increase, causing the interface more costly. In HX8357-A, GPIO can be the solution for that problem. User may control the 8 GPIOs as input or output by use of simple register setting. So additional connection between base band modem / AP (application processor) and components on upper clamshell are not needed.

The following table shows several set of register for GPIO.

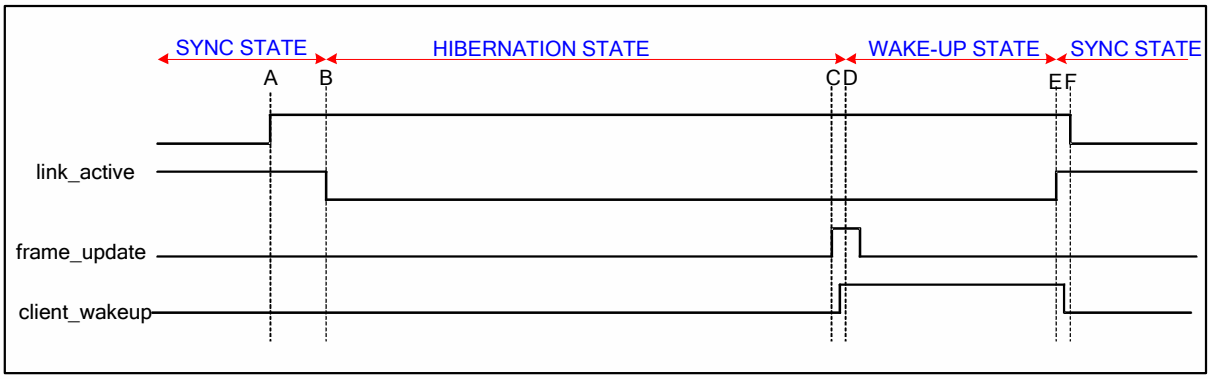
Register	Width	Description		Reset Value
GPIO (6Bh)	[7:0]	Write	For GPIO output mode: output GPIO register value to GPIO PAD	8'h00
		Read	For GPIO input mode: read GPIO PAD status	
GPIO_CON (6Ch)	[7:0]	Write	GPIO PAD input/output mode control : (0 : input / 1 : output)	8'h00
		Read	GPIO_CON register value	
GPCLR (6Fh)	[7:0]	Write	For GPIO input mode: clear specified GPIO interrupt (set by GPIO PAD input).	8'h00
		Read	GPIO interrupt state (set by GPIO PAD input).	
GPIO_EN (6Dh)	[7:0]	Write	For GPIO input mode: enable specified GPIO interrupt	8'h00
		Read	GPIO_EN register value.	
GPPOL (6Eh)	[7:0]	Write	For GPIO input mode: GPIO interrupt polarity setting	8'hFF
		Read	GPPOL register value.	

Table 5. 23 GPIO Control Related Register

In GPIO output mode, the IC output GPIO (6Bh) register value to the defined PAD.
Set GPIO_CON register as output mode before use GPIO output.

8 different GPIO output can be controlled simultaneously using 1-register access packet (6Bh register access) so that minimum access time for each GPIO output will be 1-register access time.
GPIO input mode can only be used as client-initiated link wake-up.

For more information, refer to GPIO based link wake-up section.



The Detailed descriptions for labeled events are as follows:

A. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.

B. link_active goes low when the host puts in the link into hibernation after no more data needs to be sent to the HX8357-A

C. frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the beginning of the frame buffer. Link wake-up point can be set using WKF and WKL (R68h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up.

D. client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

E. link_active goes high after the host brings the link out of hibernation.

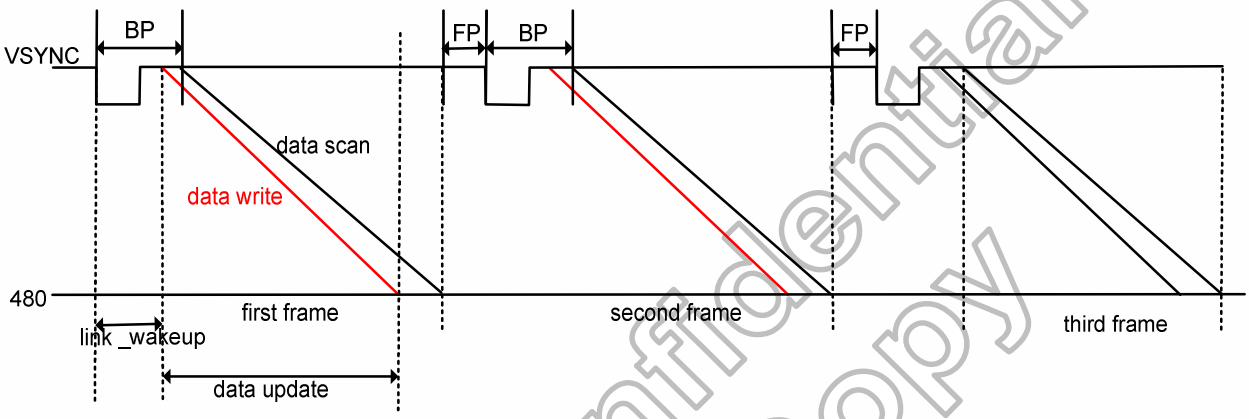
F. After link wake-up, client_wakeup signal and the VWAKE register are cleared automatically.

5.2.3.10 VSYNC mode in MDDI (host initiated wake-up)

VSYNC mode in MDDI can enable host initiated wakeup. In this mode, wake up from hibernation state need no special signal. Host only sends wakeup signal & data synchronizing with VSYNC signal. To operate VSYNC mode, MY, MX, MY bit (R16h) must set to '000'. Next figures show timing for data writing to GRAM and displaying read data.

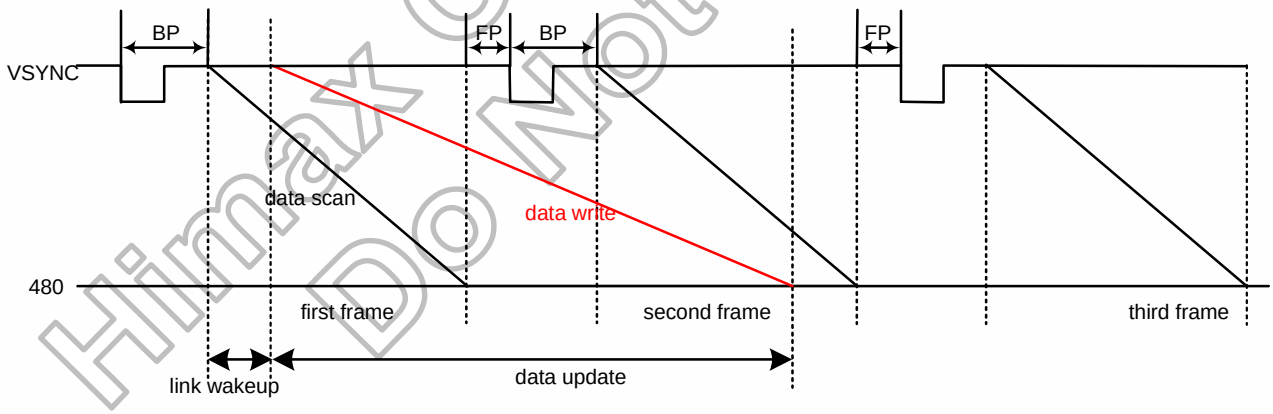
When data writing is completed within on frame

This case is that MPU write speed faster Panel Read speed



When completion of data writing takes one frame or more period:

This case is that MPU write speed slower Panel Read speed



5.2.3.11 MDDI operation mode

The MDDI Link supports six operation modes, the mode flow is illustrated as below.

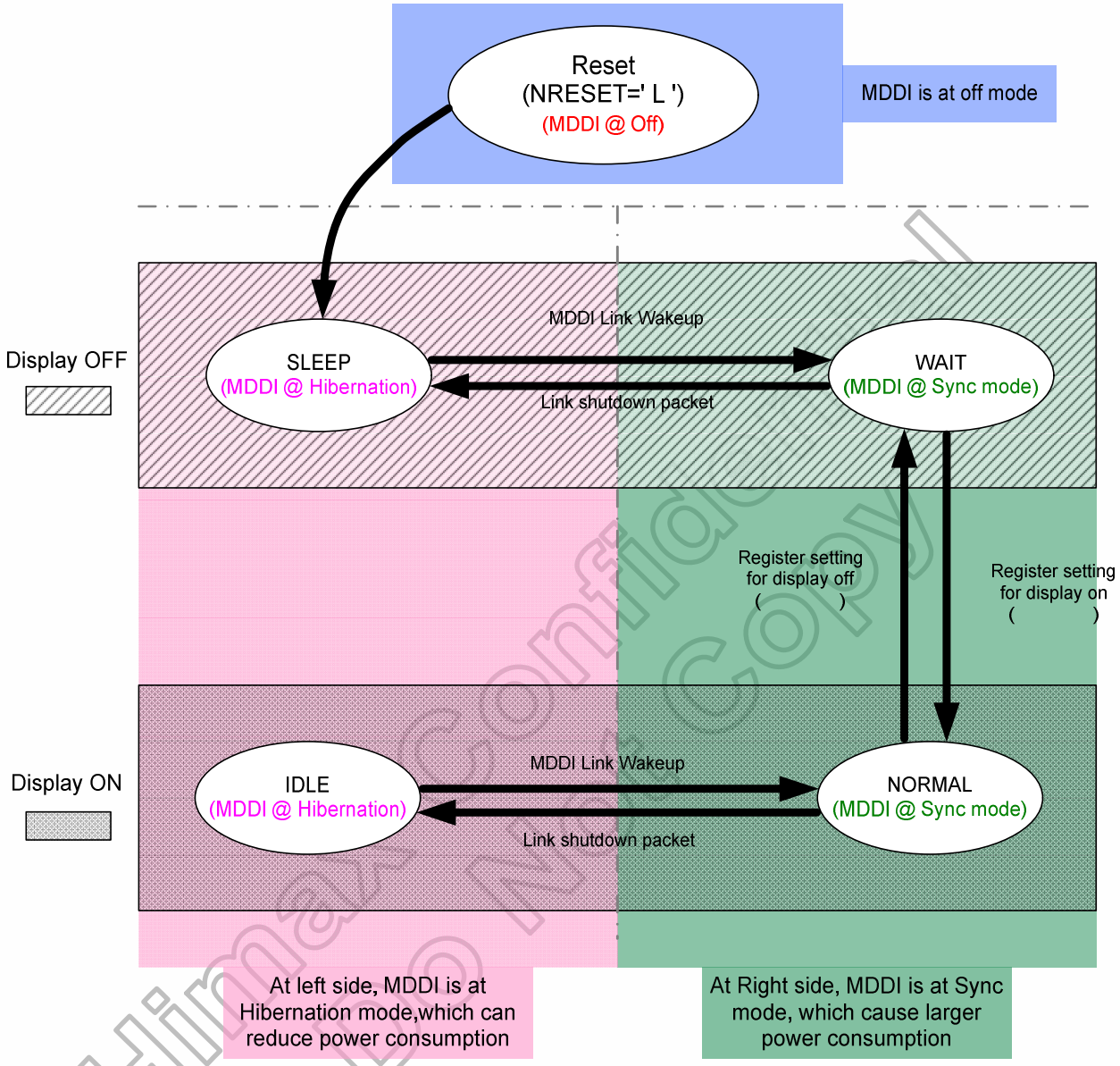


Figure 5. 49 MDDI Operation Mode

The MDDI Link supports five operation modes listed in Table below

Function	RESET	SLEEP	WAIT	NORMAL	IDLE
MDDI hibernation receiver	OFF	ON	OFF	OFF	ON
MDDI normal receiver or normal driver	OFF	OFF	ON	ON	OFF
Register and RAM access	Disable	Disable	Enable	Enable	Disable
Internal oscillator(OSC)	OFF	OFF	ON/OFF (1)	ON(2)	ON(2)
Booster(VDDVDH,VGH,VGL,VCL)	OFF	OFF	OFF	ON	ON
Regulator (VCOMH,VCOML,VREG1)	OFF	OFF	OFF	ON	ON

Note: (1) If OSC_EN = 0 is OFF, and if OSC_EN = 1 is ON.
(2) Do not set OSC_EN = 1 in Normal mode, If OSC stopped, indication also stops.

Table 5. 24 Operation Mode List

5.2.3.12 Sub panel interface

The HX8357-A supports the Sub Panel interface which connected to Sub Panel driver IC with Parallel Interface. When HX8357-A receive MDDI packets from host device, the HX8357-A will convert MDDI packet to parallel data and send to sub panel driver IC.

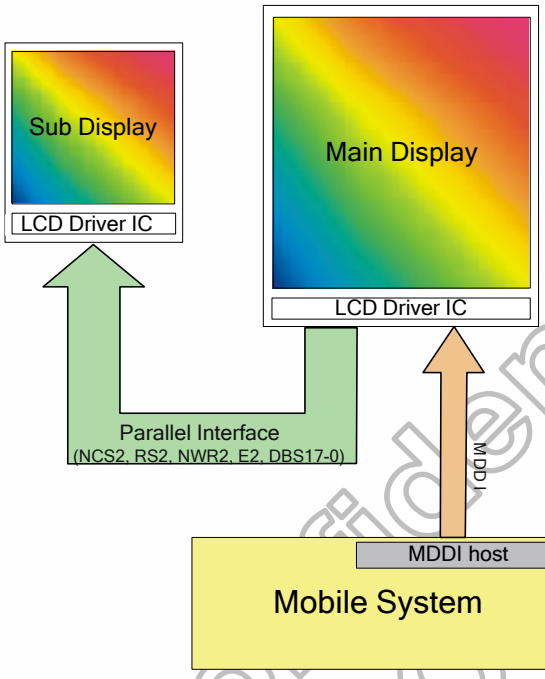


Figure 5. 50 Sub Panel Interface

5.2.3.13 Sub panel function

When the register access packet is received, then following register access packets or video stream packets are transferred to the sub panel via Sub Panel Interface. Sub panel selection address (R72h) can be changed by setting register SUB_SEL. The SUB_SEL value must be set to unused address in both Main/Sub Panel Driver IC. If video data is transferred to the sub panel driver IC via the Sub Panel Interface, additional RAM Index (default 0022h) is automatically generated by HX8357-A.

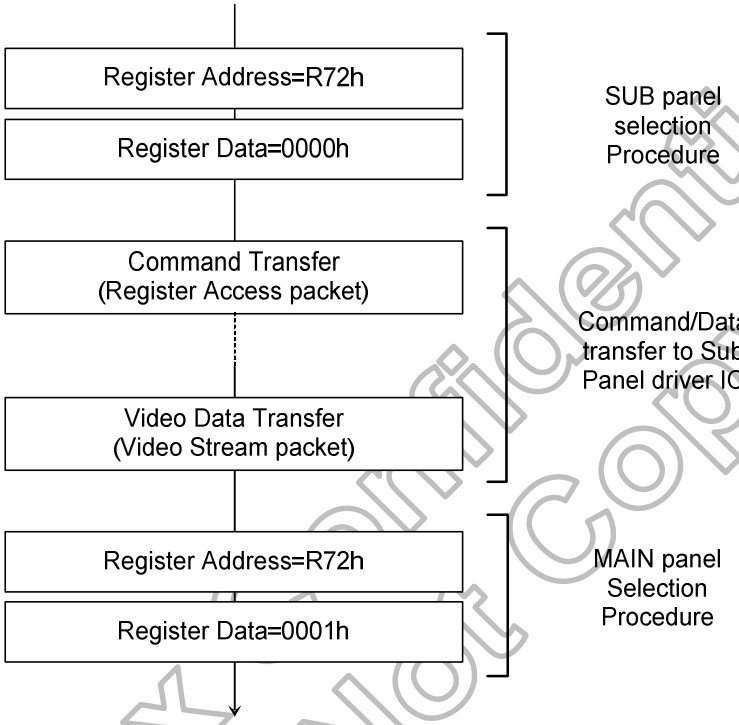


Figure 5. 51 Main/Sub Panel Selection Procedure

5.2.3.14 Sub panel interface timing

The HX8357-A's Sub Panel Interface is supports two type panel (TFT and STN) and offer 18-/16-/9-/8-bit interface format (i80 and m68 system).

TFT type sub panel timing

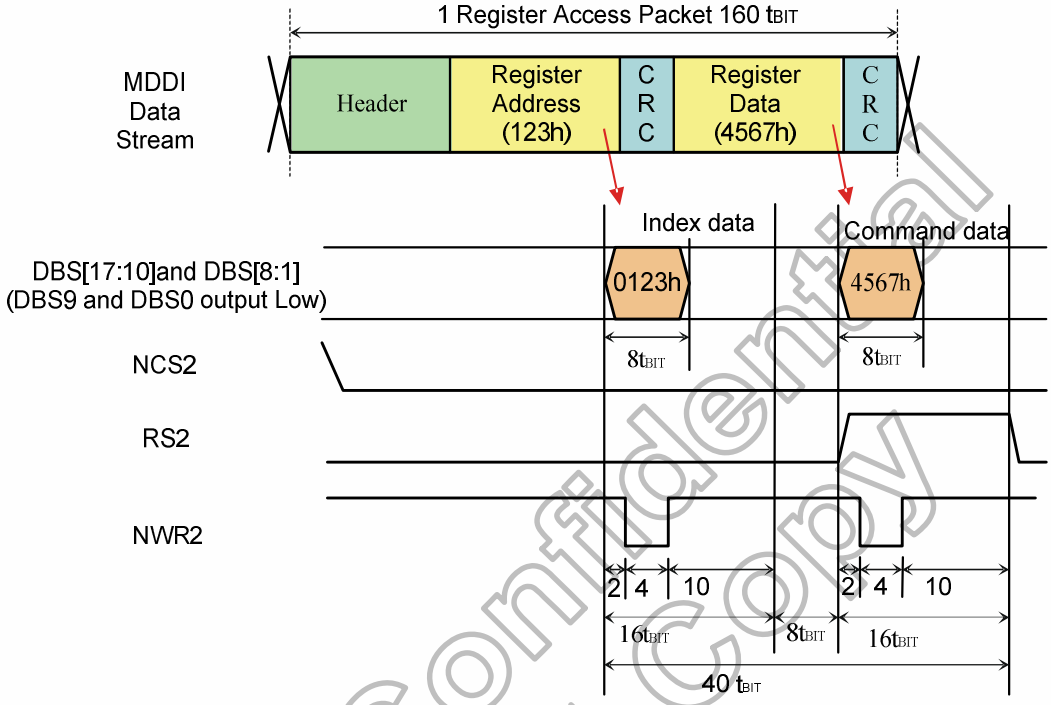


Figure 5.55 18-/16-Bit Sub Panel Interface Register Access Data Timing for i80 Series TFT Sub Panel

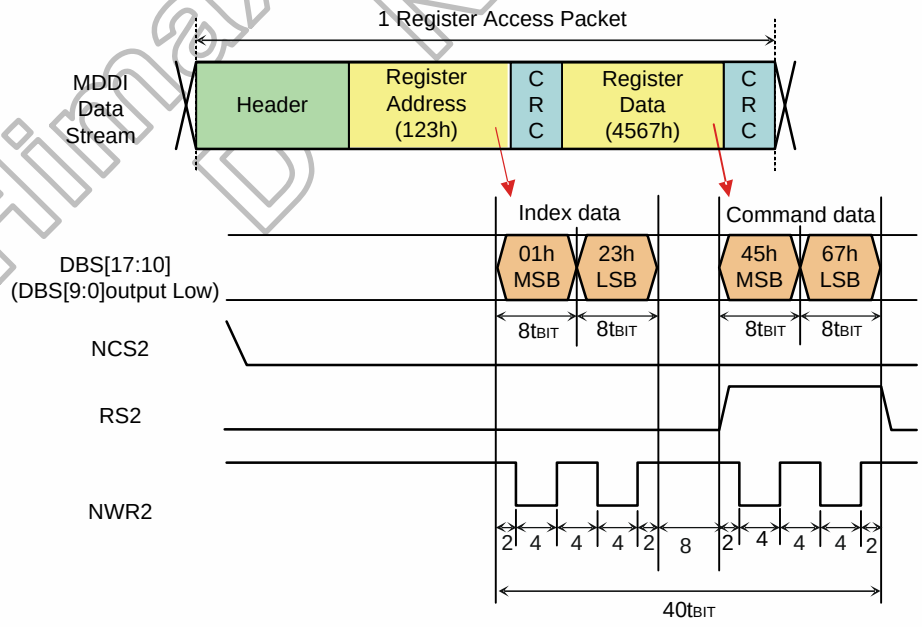


Figure 5. 52 9-/8-Bit Sub Panel Interface Register Access Data Timing for i80 Series TFT Sub Panel

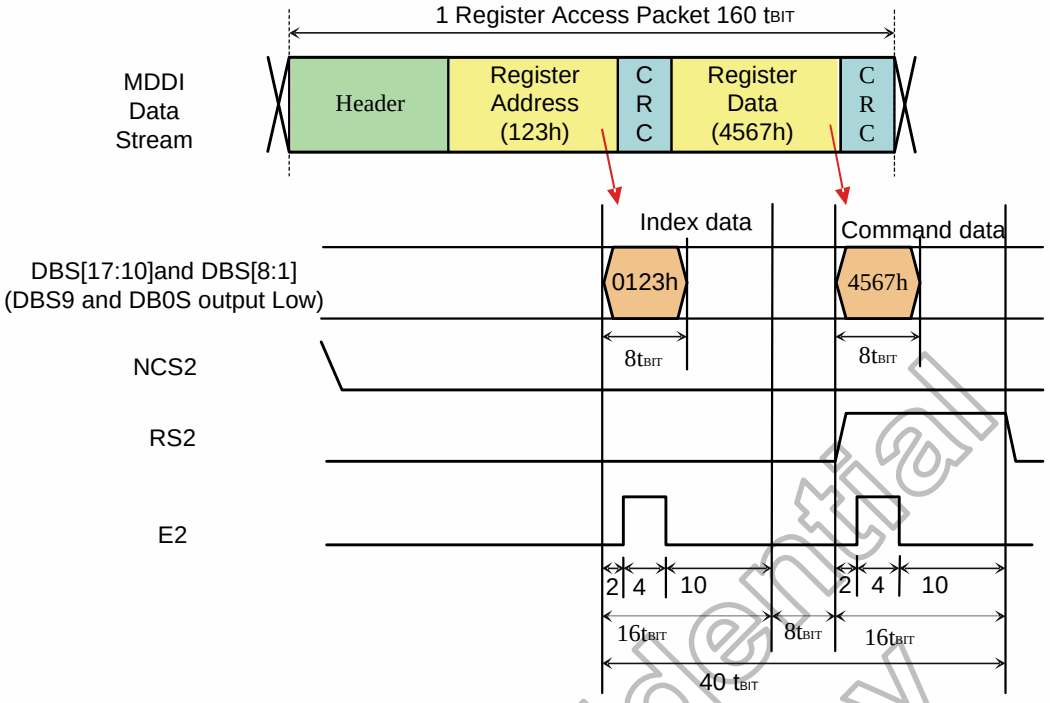


Figure 5. 53 18-/16-Bit Sub Panel Interface Register Access Data Timing for i80 Series TFT Sub Panel

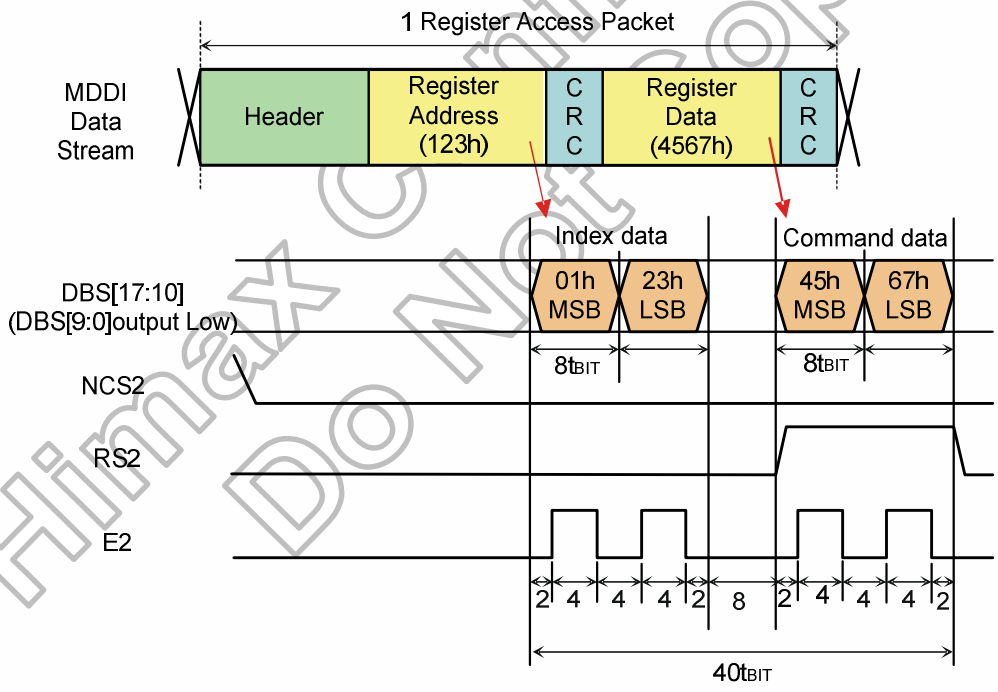


Figure 5. 54 9-/8-Bit Sub Panel Interface Register Access Data Timing for m68 Series TFT Sub Panel

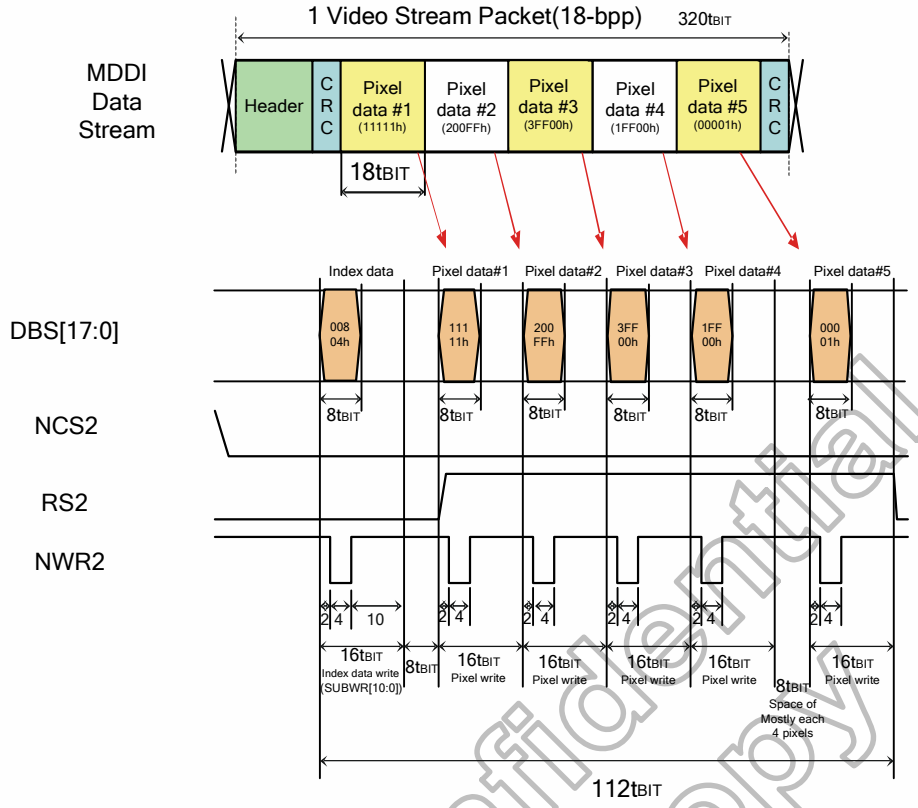


Figure 5. 55 18-Bit Sub Panel Interface Video Data Timing for i80 Series TFT Sub Panel

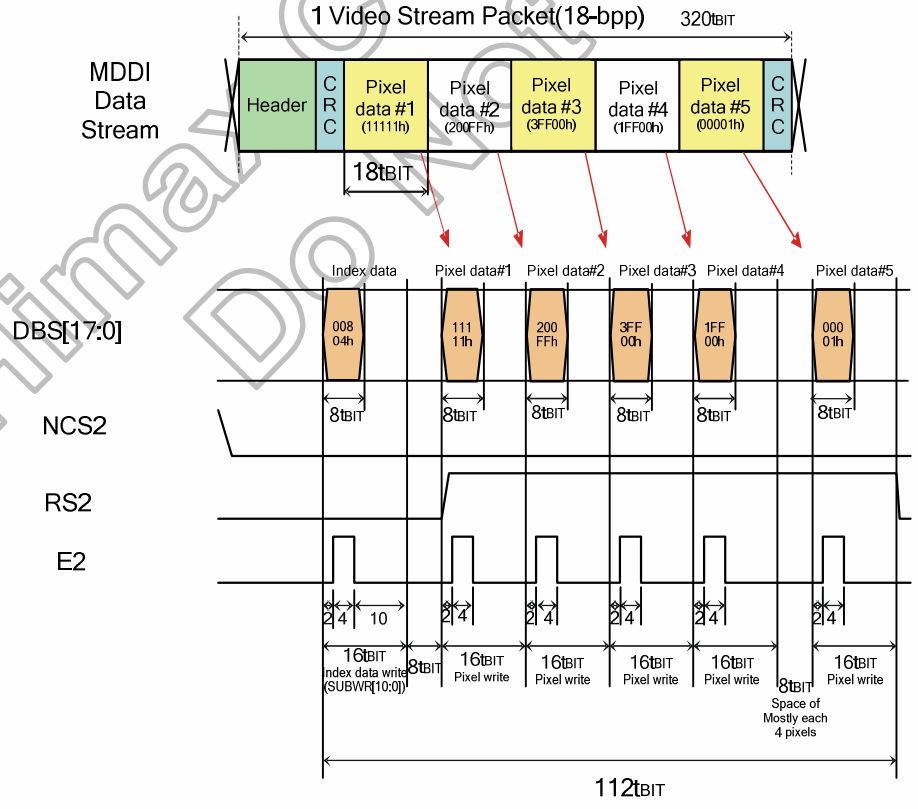


Figure 5. 56 18-Bit Sub Panel Interface Video Data Timing for M68 Series TFT Sub Panel

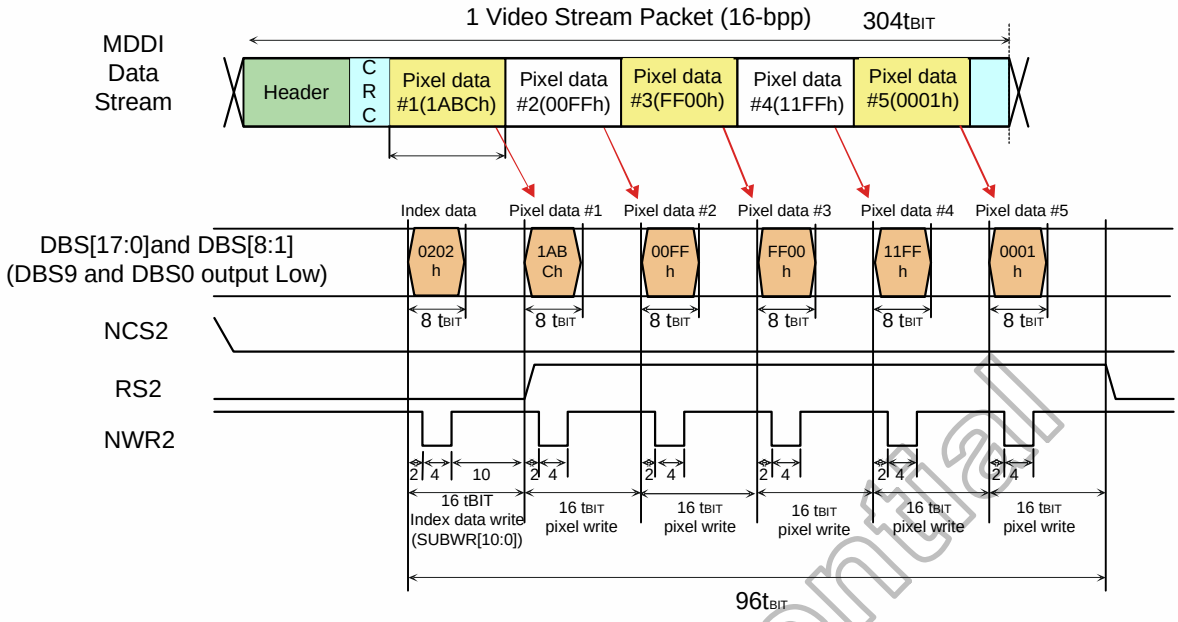


Figure 5. 57 16-Bit Sub Panel Interface Video Data Timing for I80 Series TFT Sub Panel

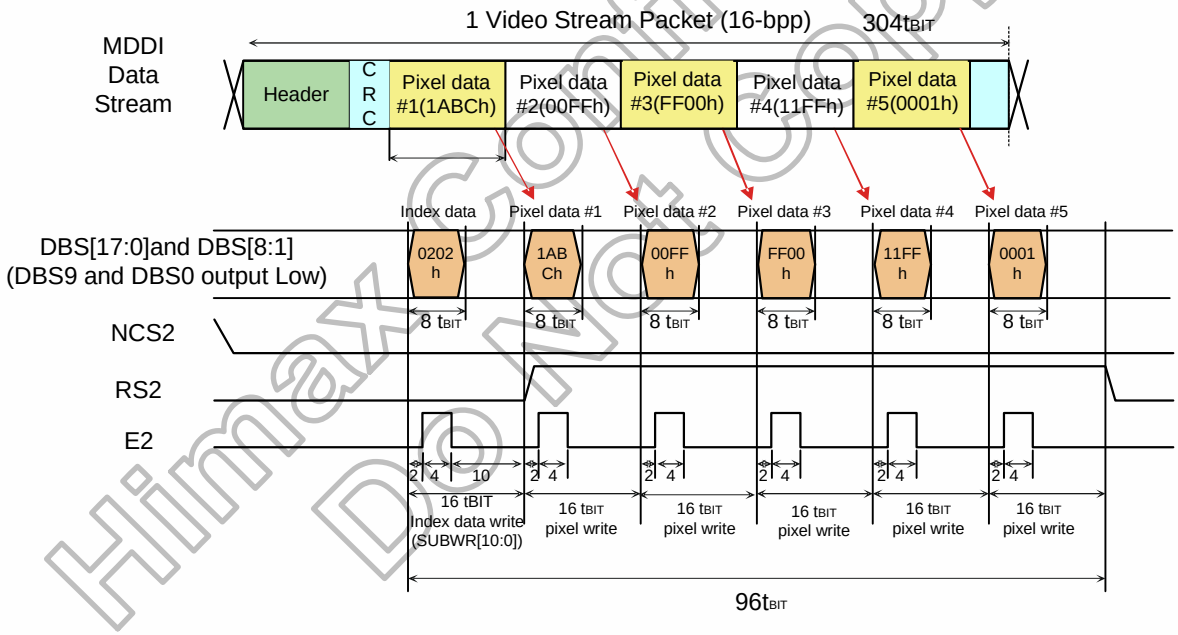


Figure 5. 58 16-Bit Sub Panel Interface Video Data Timing for m68 Series TFT Sub Panel

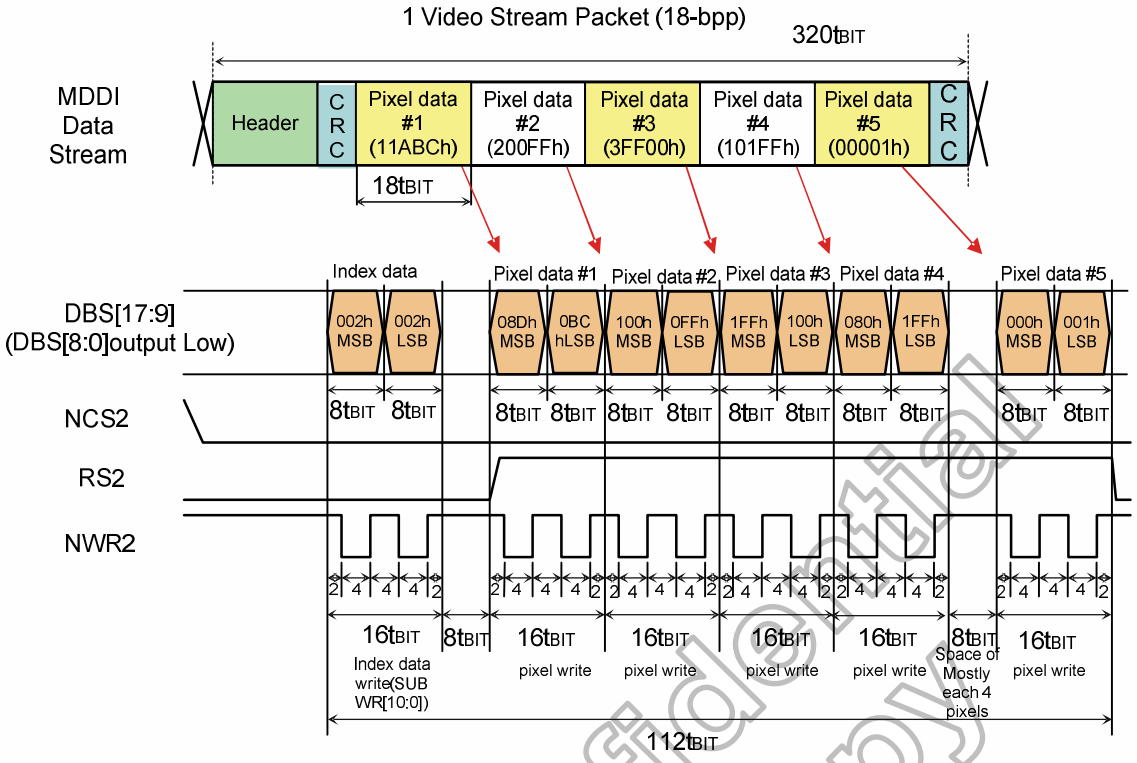


Figure 5. 59 9-Bit Sub Panel Interface Video Data Timing for i80 Series TFT Sub Panel

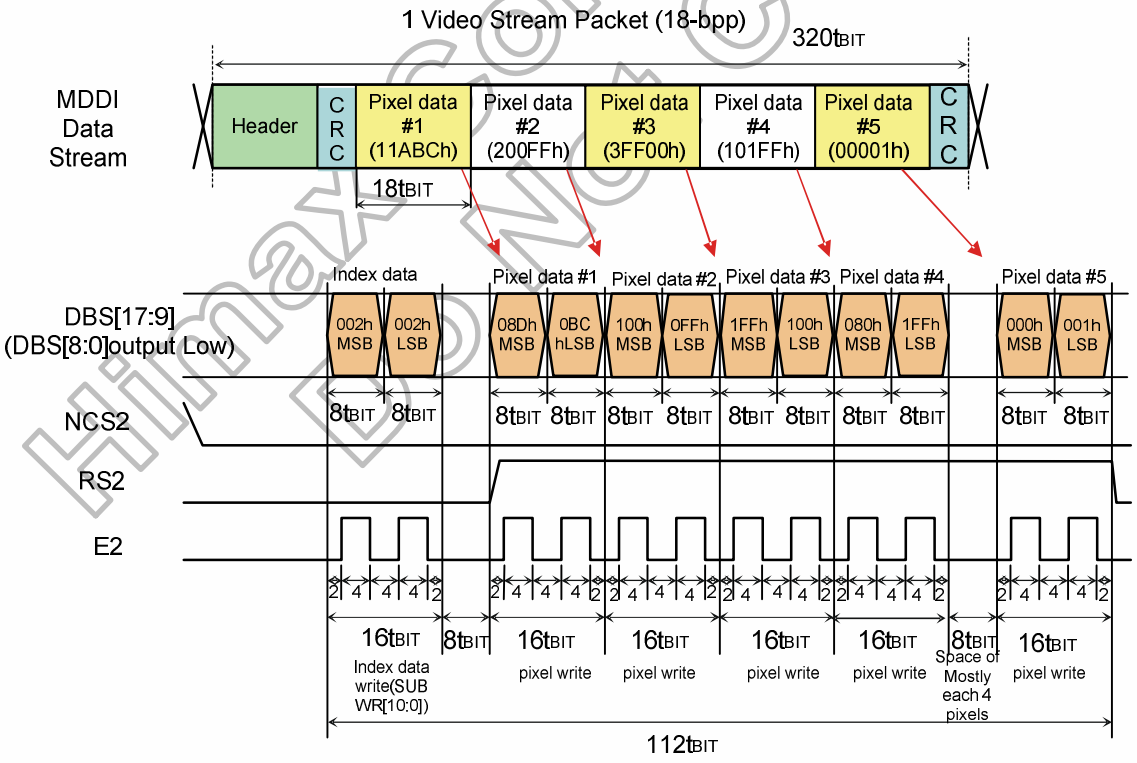


Figure 5. 60 9-Bit Sub Panel Interface Video Data Timing for m68 Series TFT Sub Panel

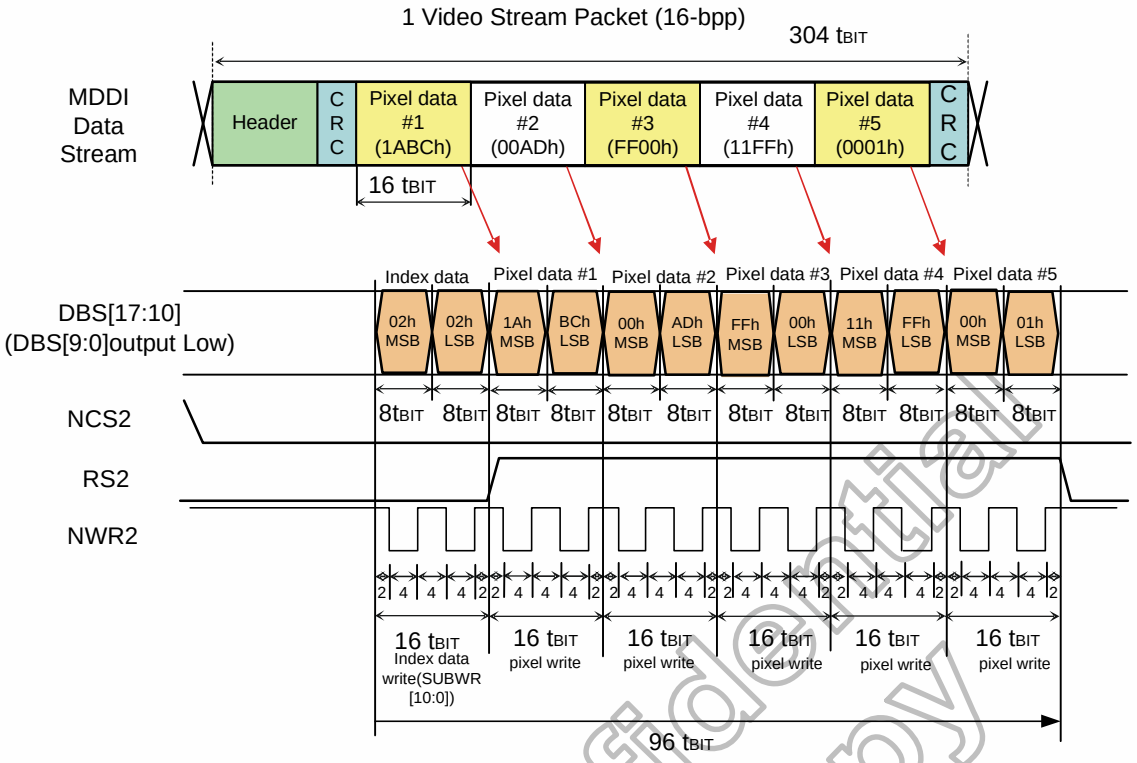


Figure 5. 61 8-Bit Sub Panel Interface Video Data Timing for i80 Series TFT Sub Panel

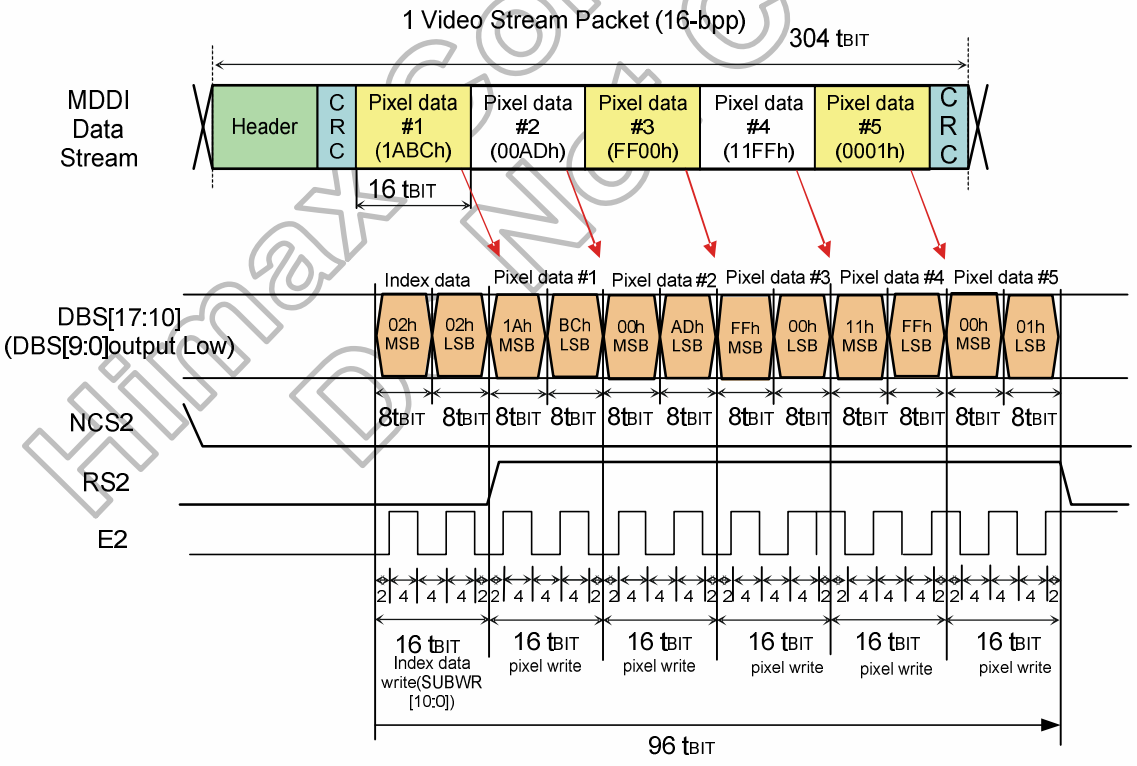


Figure 5. 62 8-Bit Sub Panel Interface Video Data Timing for m68 Series TFT Sub Panel

STN type sub panel timing

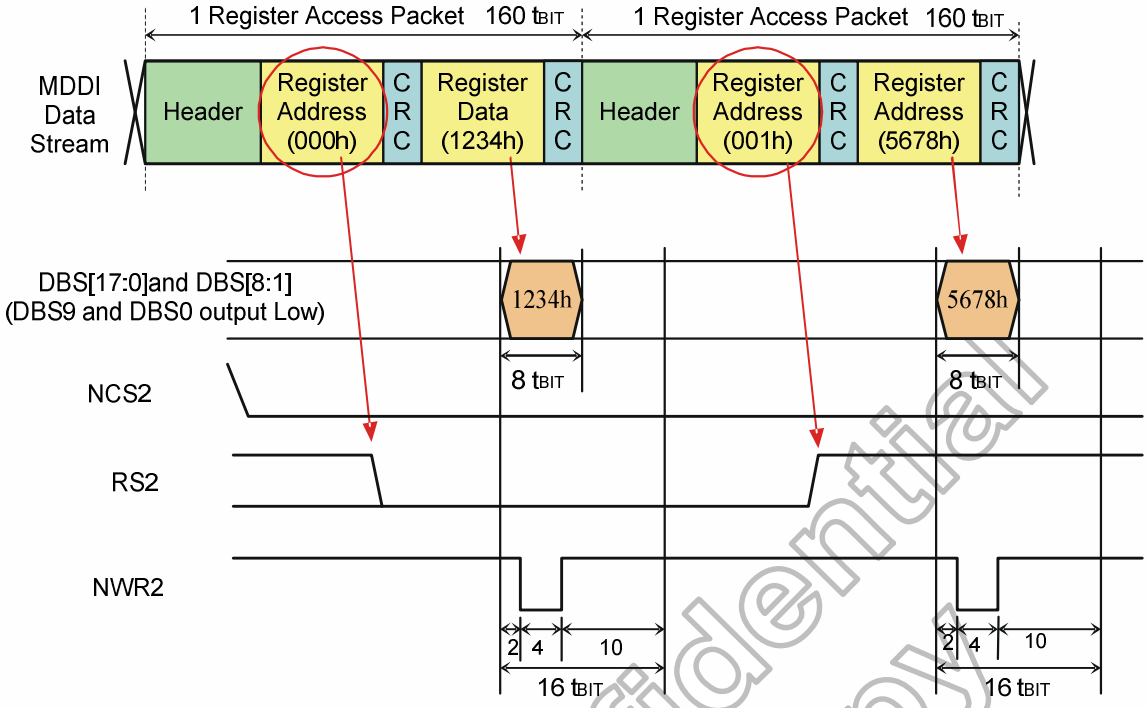


Figure 5. 63 18-/16-Bit Sub Panel Interface Register Access Data Timing for i80 Series STN Sub Panel

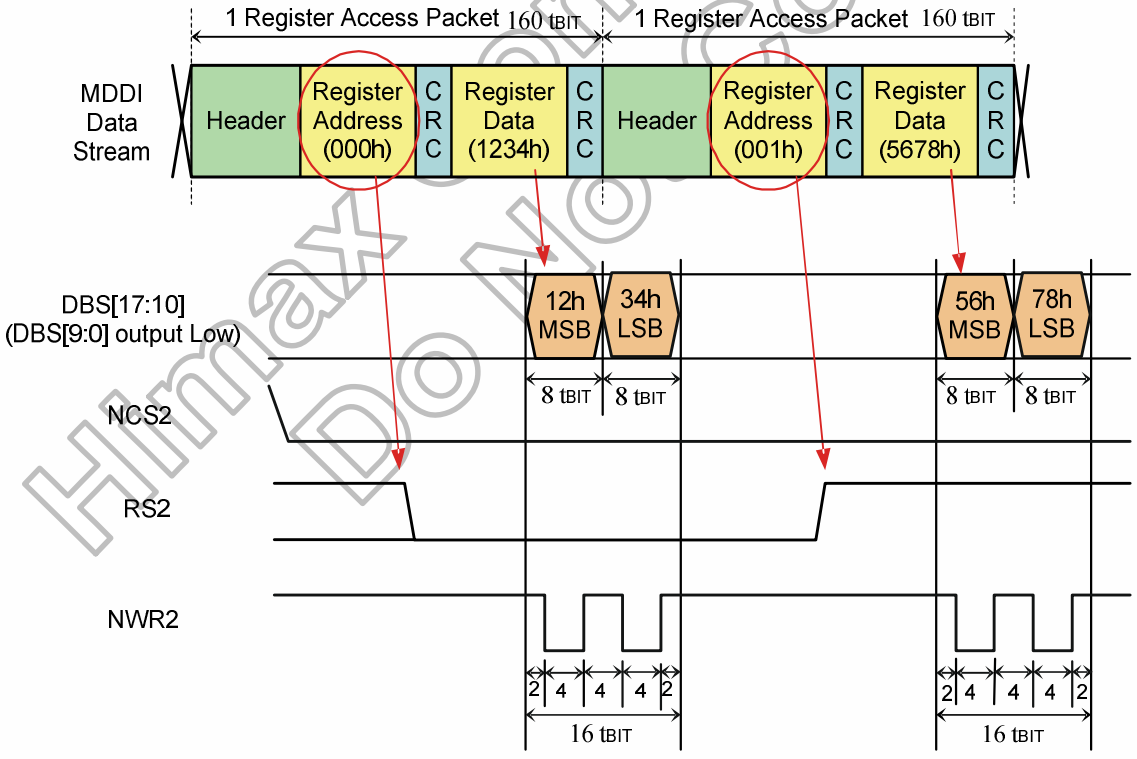


Figure 5. 64 9-/8-Bit Sub Panel Interface Register Access Data Timing for i80 Series STN Sub Panel

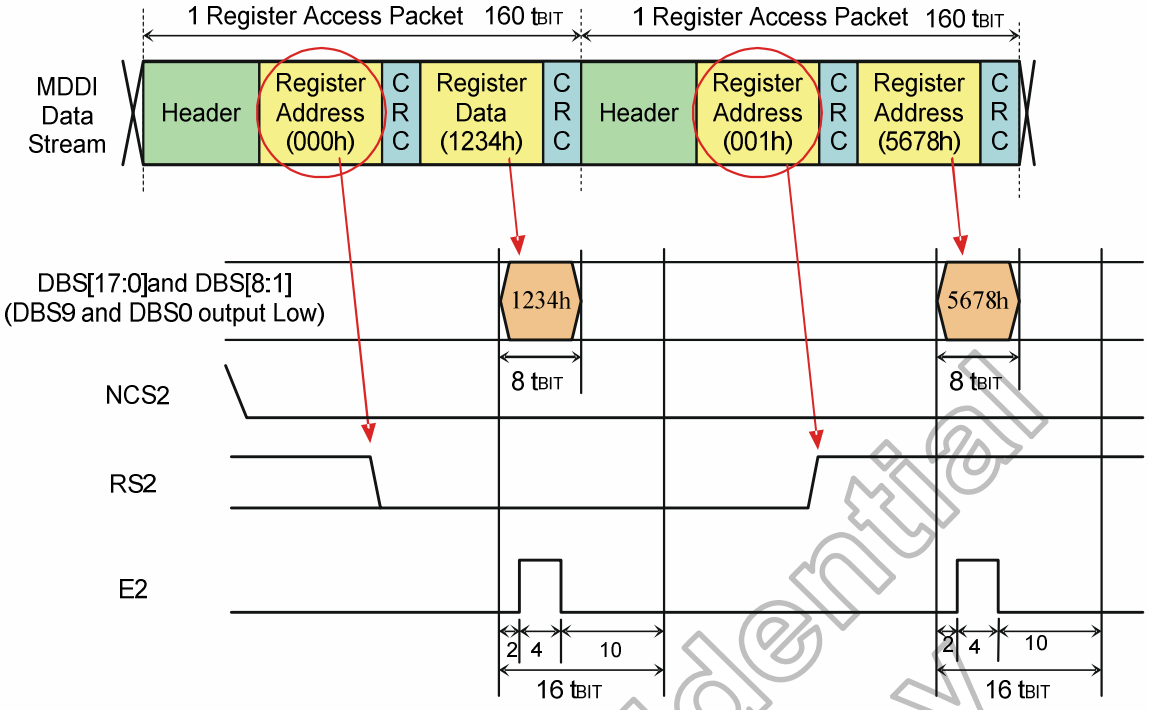


Figure 5. 65 18-/16-Bit Sub Panel Interface Register Access Data Timing for m68 Series STN Sub Panel

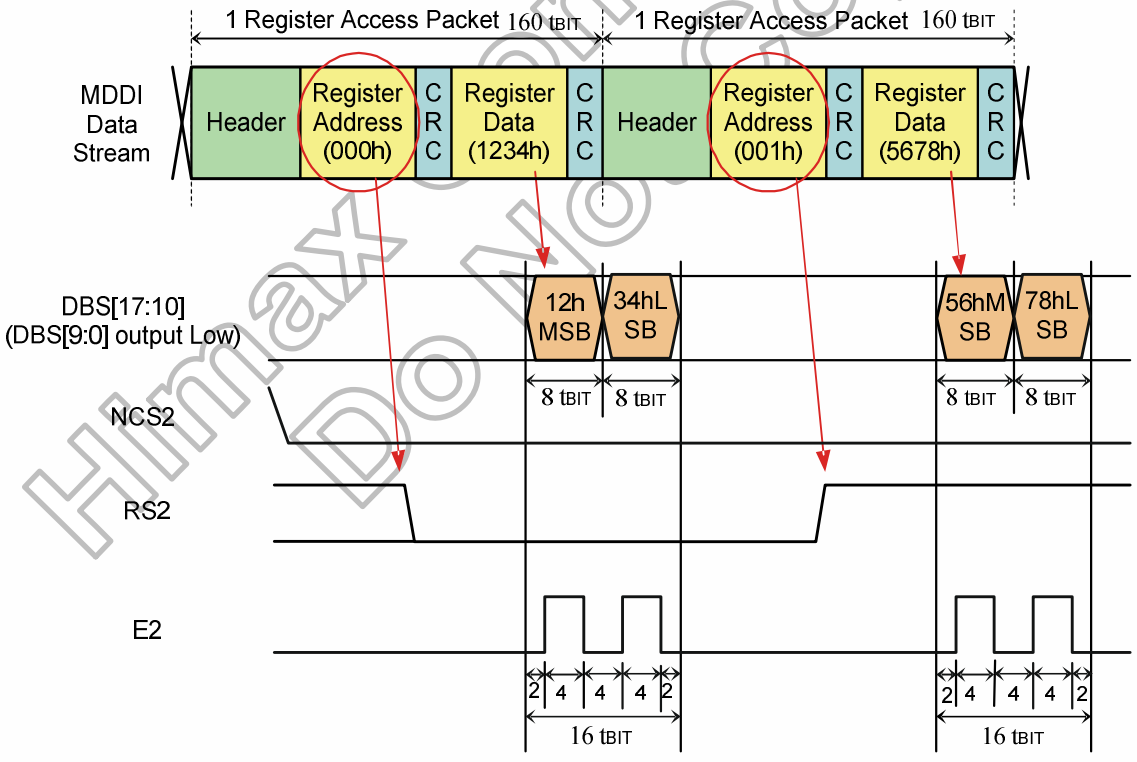
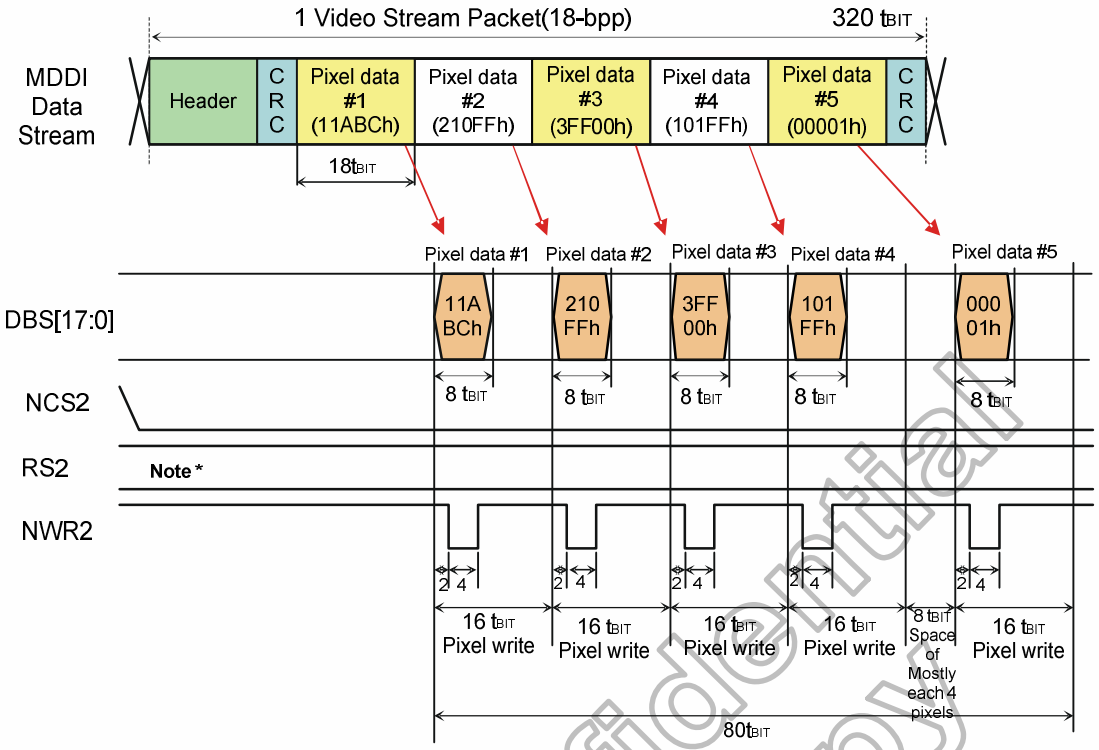
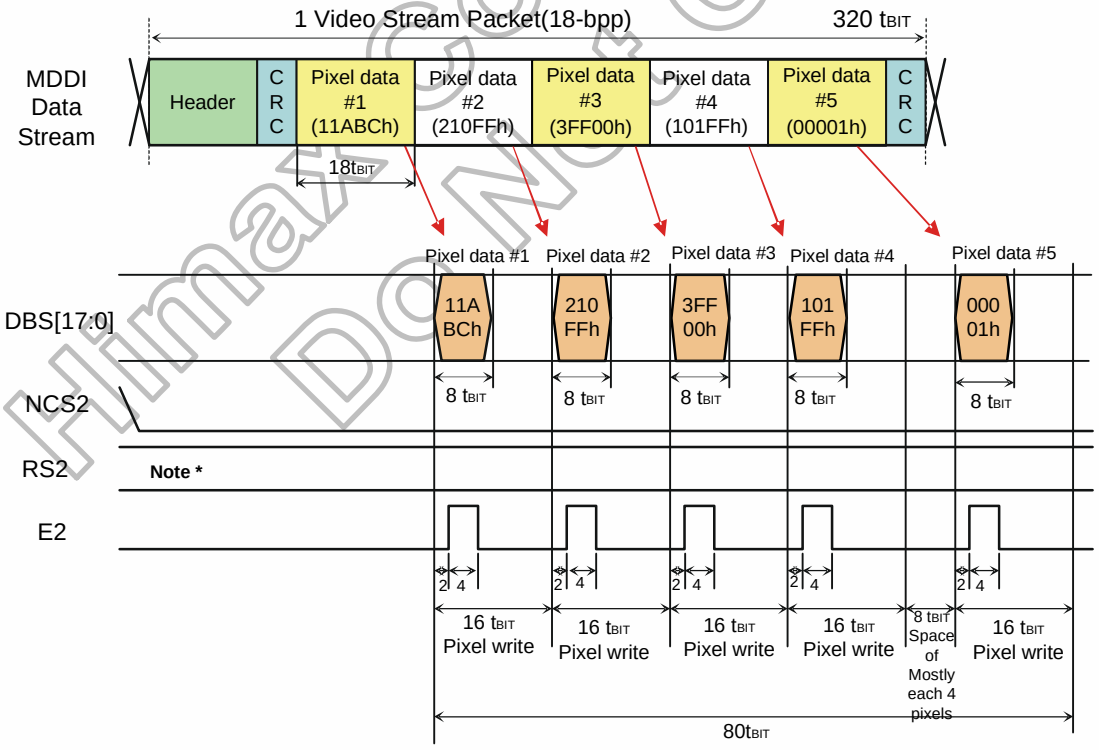


Figure 5. 66 9-/8-Bit Sub Panel Interface Register Access Data Timing for m68 Series STN Sub Panel



Note * : The status RS2 output is specified by SUBRS[1:0] bit of index:020h

Figure 5. 67 18-Bit Sub Panel Interface Video Data Timing for i80 Series STN Sub Panel



Note * : The status RS2 output is specified by SUBRS[1:0] bit of index:020h

Figure 5. 68 18-Bit Sub Panel Interface Video Data Timing for m68 Series STN Sub Panel

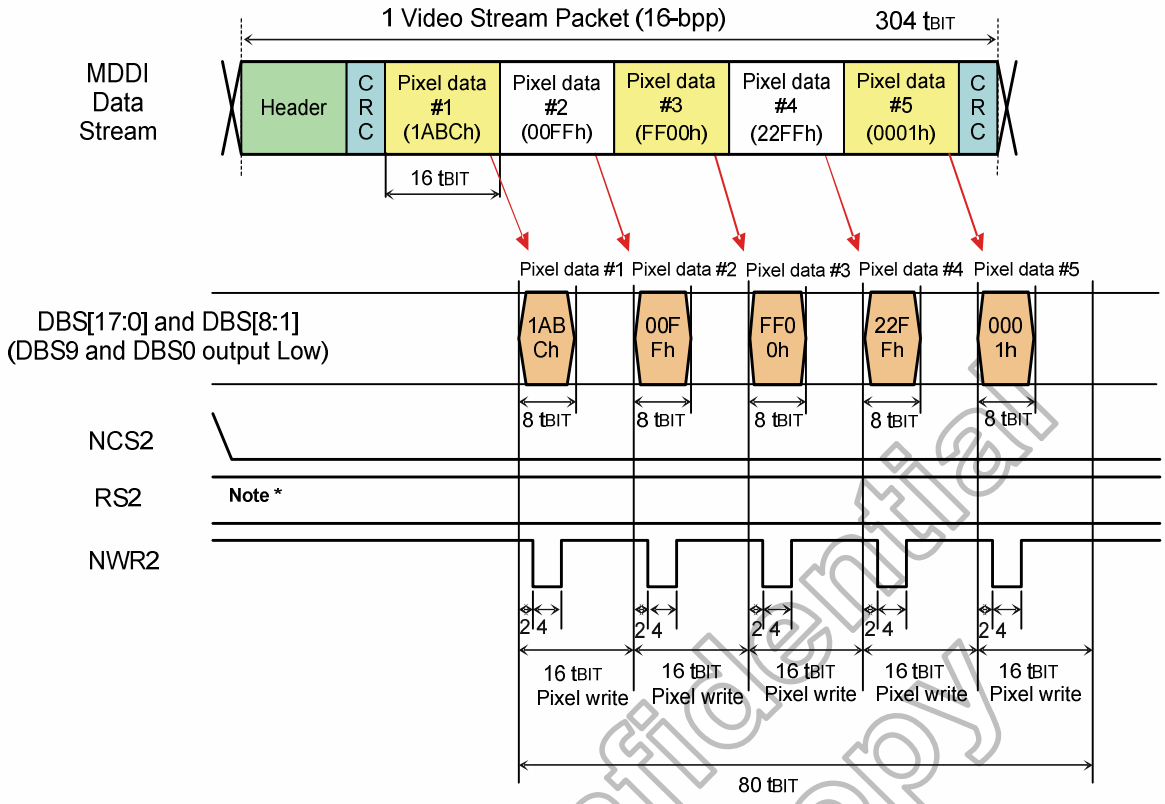


Figure 5. 69 16-Bit Sub Panel Interface Video Data Timing for i80 Series STN Sub Panel

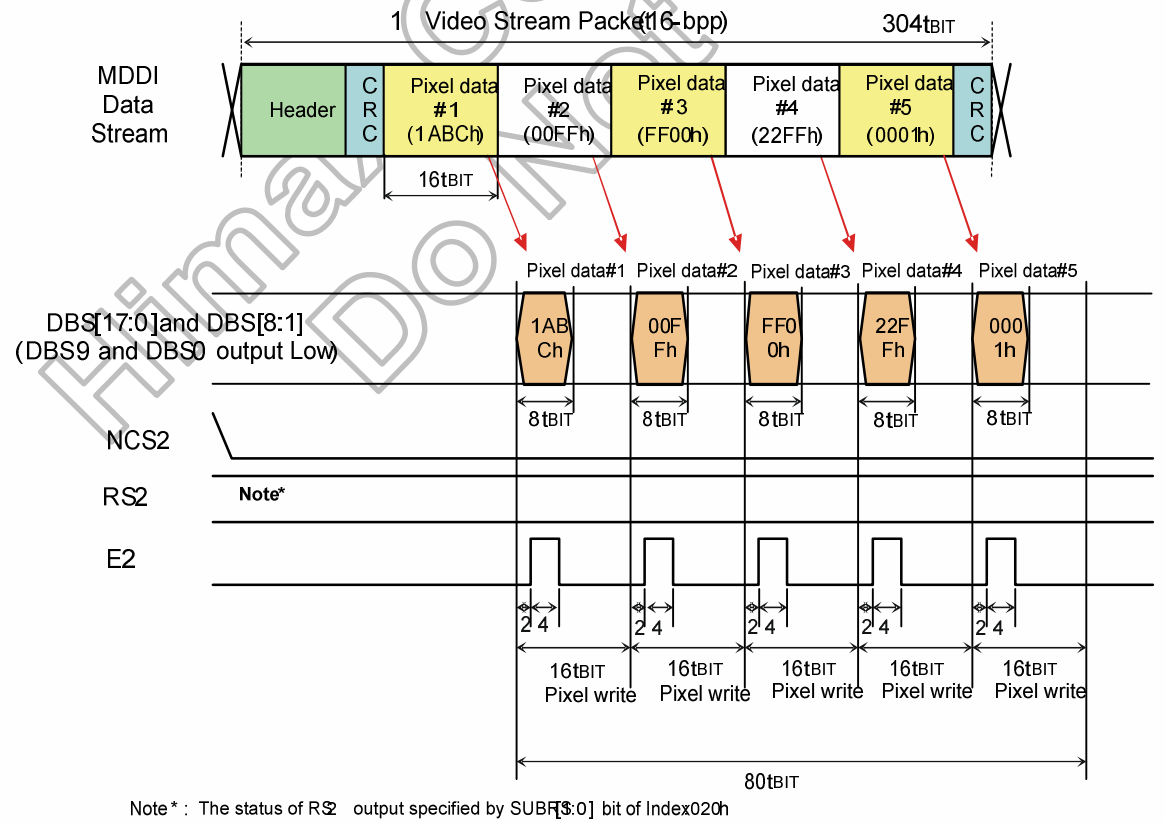
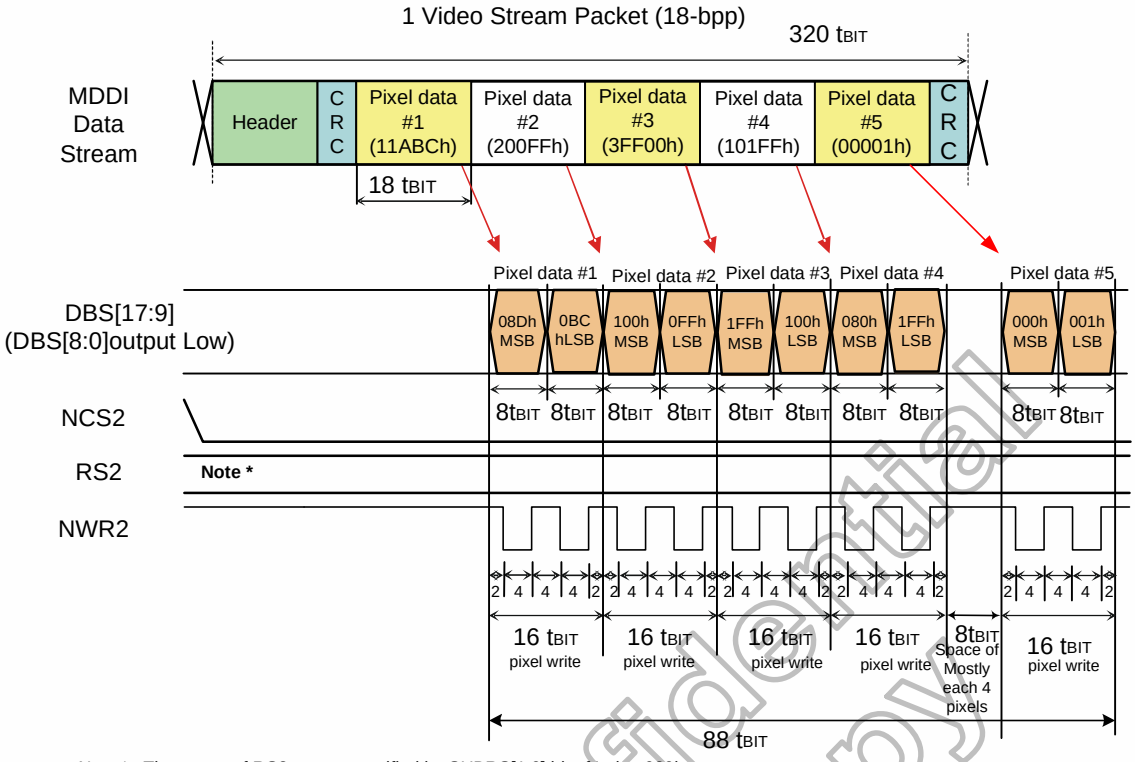
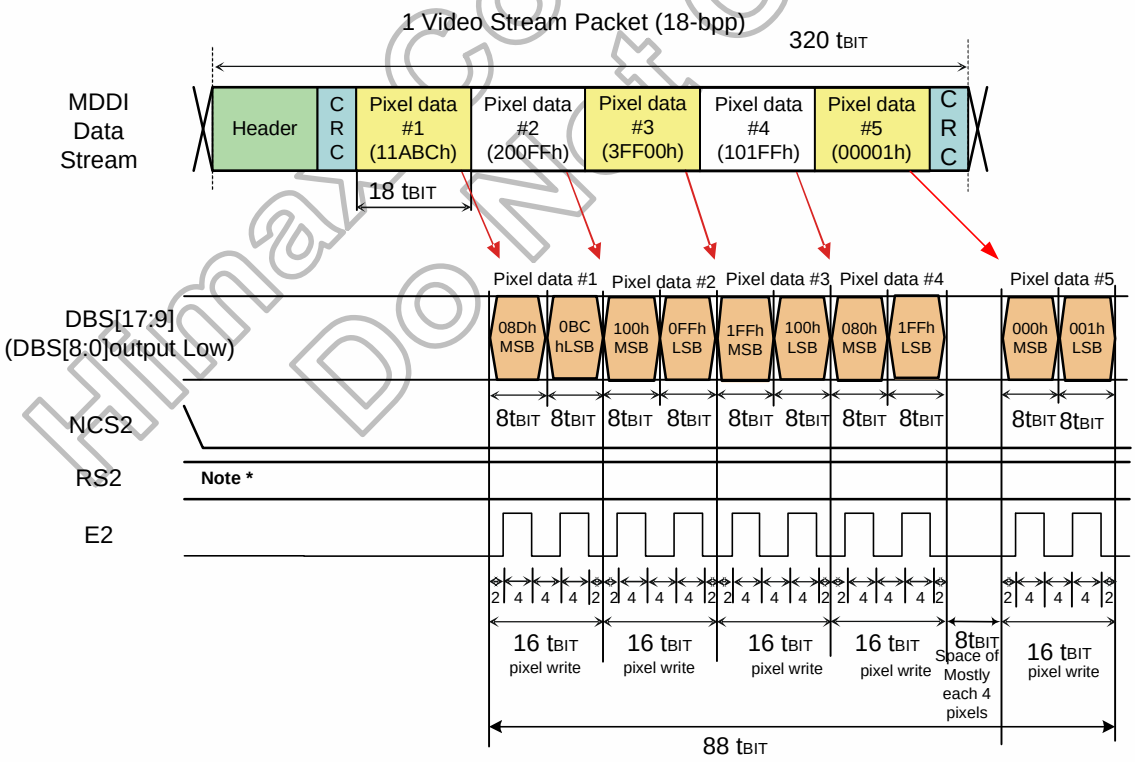


Figure 5. 70 16-Bit Sub Panel Interface Video Data Timing for m68 Series STN Sub Panel



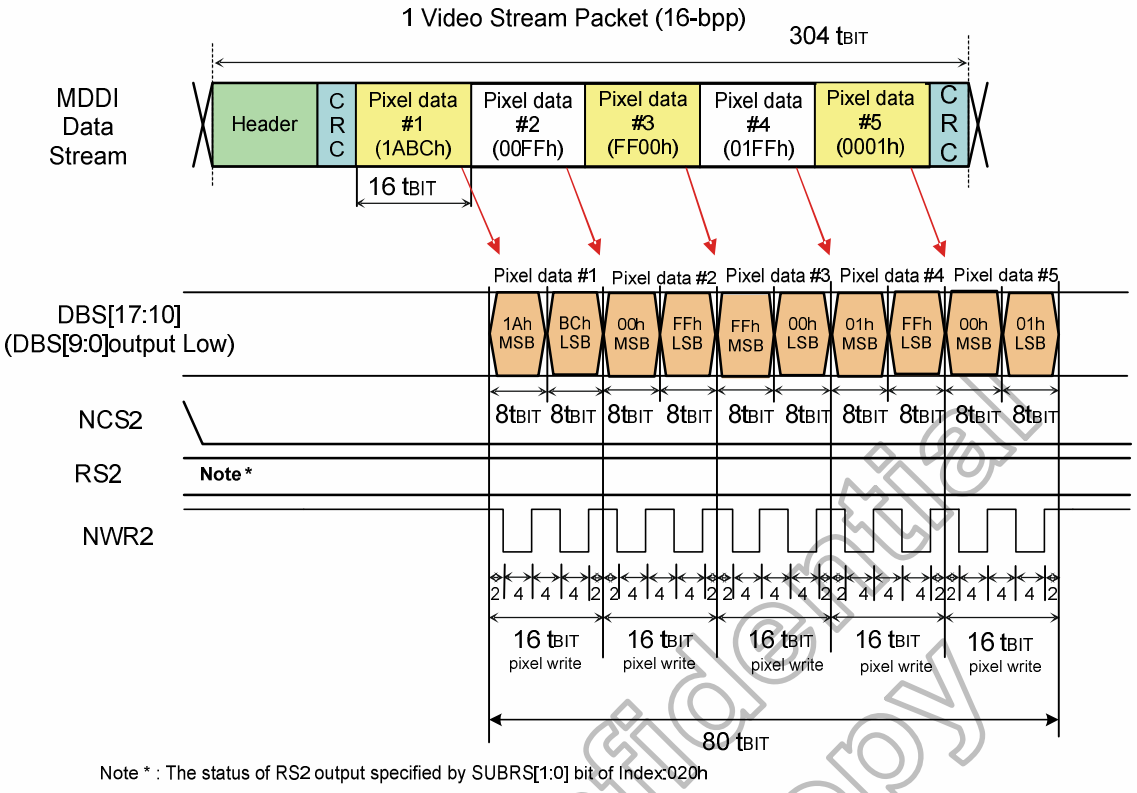
Note * : The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5. 71 9-Bit Sub Panel Interface Video Data Timing for i80 Series STN Sub Panel



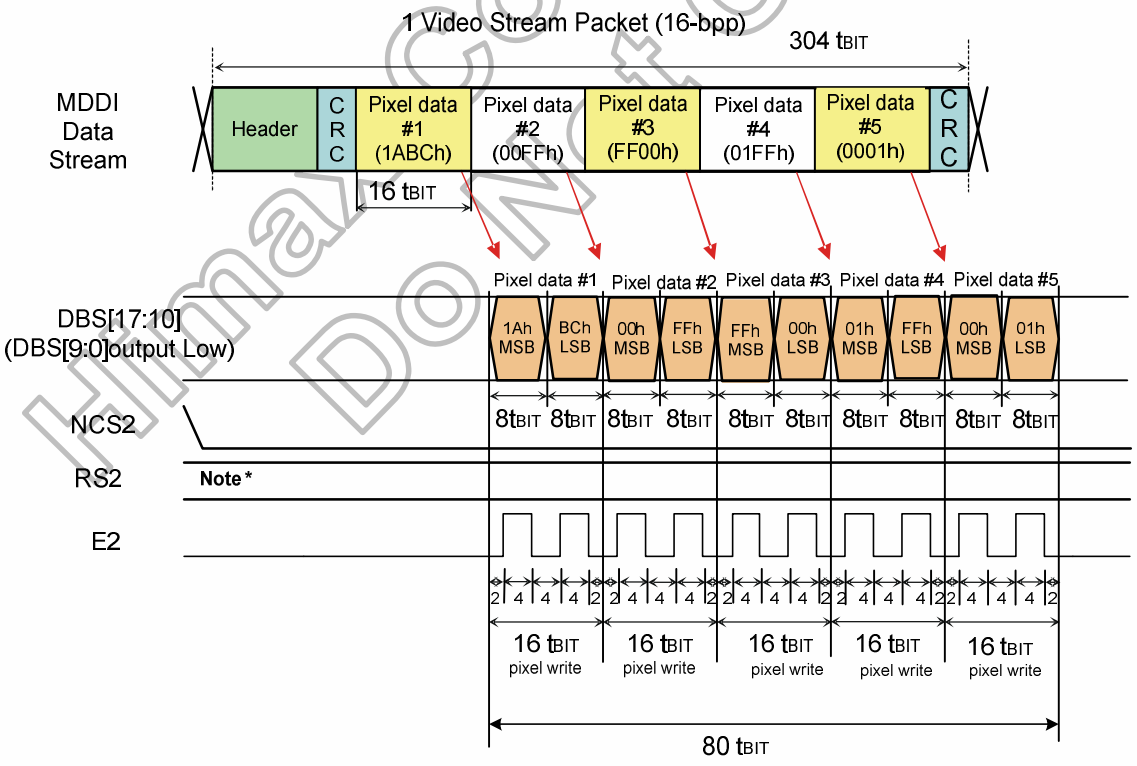
Note * : The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5. 72 9-Bit Sub Panel Interface Video Data Timing for m68 Series STN Sub Panel



Note * : The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5. 73 8-Bit Sub Panel Interface Video Data Timing for i80 Series STN Sub Panel

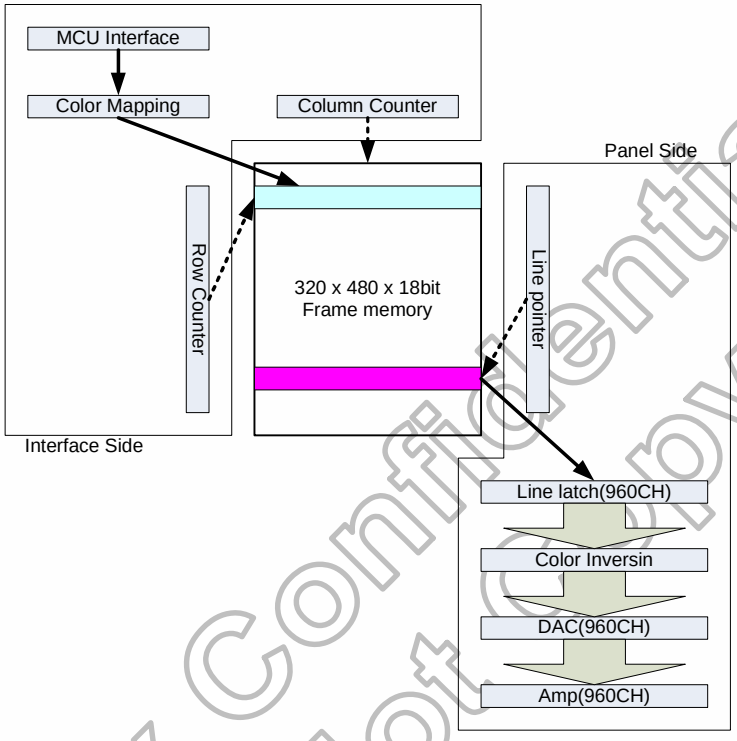


Note * : The status of RS2 output specified by SUBRS[1:0] bit of Index:020h

Figure 5. 74 8-Bit Sub Panel Interface Video Data Timing for m68 Series STN Sub Panel

6. Display Data GRAM

The display data RAM stores display dots and consists of 2,764,800 bits (320x480x18bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



6.1 Display data GRAM mapping

Every pixel (18-bit) data in GRAM is located by a (Row, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting R22h commands from start positions of the window address.

(000,000)H	(000,001)H	(000,002)H	---------	(000,13C)H	(00,13D)H	(000,13E)H	(000,13F)H
(001,000)H	(001,001)H	(001,002)H	---------	(001,13C)H	(01,13D)H	(001,13E)H	(001,13F)H
(002,000)H	(002,001)H	(002,002)H	---------	(002,13C)H	(02,13D)H	(002,13E)H	(002,13F)H
(003,000)H	(003,001)H	(003,002)H	---------	(003,13C)H	(03,13D)H	(003,13E)H	(003,13F)H
(004,000)H	(004,001)H	(004,002)H	---------	(004,13C)H	(04,13D)H	(004,13E)H	(004,13F)H
(005,000)H	(005,001)H	(005,002)H	---------	(005,13C)H	(05,13D)H	(005,13E)H	(005,13F)H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(1DA,000)H	(1DA,001)H	(1DA,002)H	---------	(1DA,13C)H	(1DA,13D)H	(1DA,13E)H	(1DA,13F)H
(1DB,000)H	(1DB,001)H	(1DB,002)H	---------	(1DB,13C)H	(1DB,13D)H	(1DB,13E)H	(1DB,13F)H
(1DC,000)H	(1DC,001)H	(1DC,002)H	---------	(1DC,13C)H	(1DC,13D)H	(1DC,13E)H	(1DC,13F)H
(1DD,000)H	(1DD,001)H	(1DD,002)H	---------	(1DD,13C)H	(1DD,13D)H	(1DD,13E)H	(1DD,13F)H
(1DE,000)H	(1DE,001)H	(1DE,002)H	---------	(1DE,13C)H	(1DE,13D)H	(1DE,13E)H	(1DE,13F)H
(1DF,000)H	(1DF,001)H	(1DF,002)H	---------	(1DF,13C)H	(1DF,13D)H	(1DF,13E)H	(1DF,13F)H

Table 6. 1 GRAM Address for Display Panel Position (320 X 480)

6.2 Address counter (AC) of GRAM

The HX8357-A contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers register (**CAC** and **RAC**) can set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV, MX** and **MY** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

The address pointers set the position of GRAM whose addresses range:

RES_SEL2	RES_SEL1	RES_SEL0	MV	X Range	Y Range	Panel Resolution
1	1	1	0	0~319d.	0~479d.	320RGB x480 dot
			1	0~479d.	0~319d.	
1	1	0	0	0~319d.	0~431d.	320RGB x432 dot
			1	0~431d.	0~319d.	
1	0	1	0	0~319d.	0~425d.	320RGB x426 dot
			1	0~425d.	0~319d.	
1	0	0	0	0~319d.	0~399d.	320RGB x400 dot
			1	0~399d.	0~319d.	
0	1	1	0	0~319d.	0~319d.	320RGB x320 dot
			1	0~319d.	0~319d.	
0	1	0	0	0~319d.	0~239d.	320RGB x240 dot
			1	0~239d.	0~319d.	
0	0	x	0	0~319d.	0~15d.	320RGB x16 dot (Note1)
			1	0~15d.	0~319d.	

Note: Reduce line number to save CP timing. (ex: CABC dimming test)

Table 6. 2 Addresses Counter Range

6.2.1 System interface to GRAM write direction

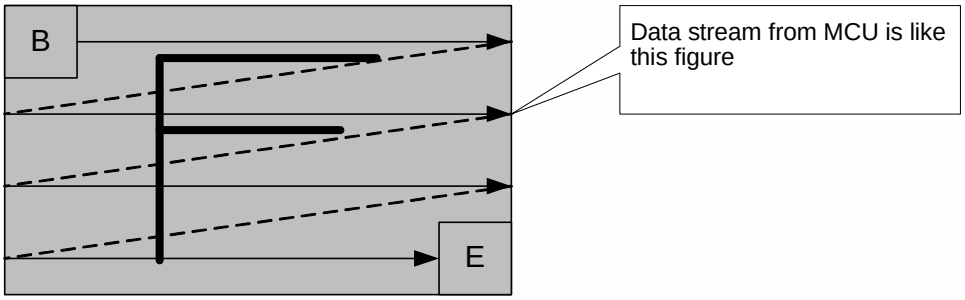


Figure 6. 1 Image Data Sending Order from the Host

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV, MX** and **MY** bits setting

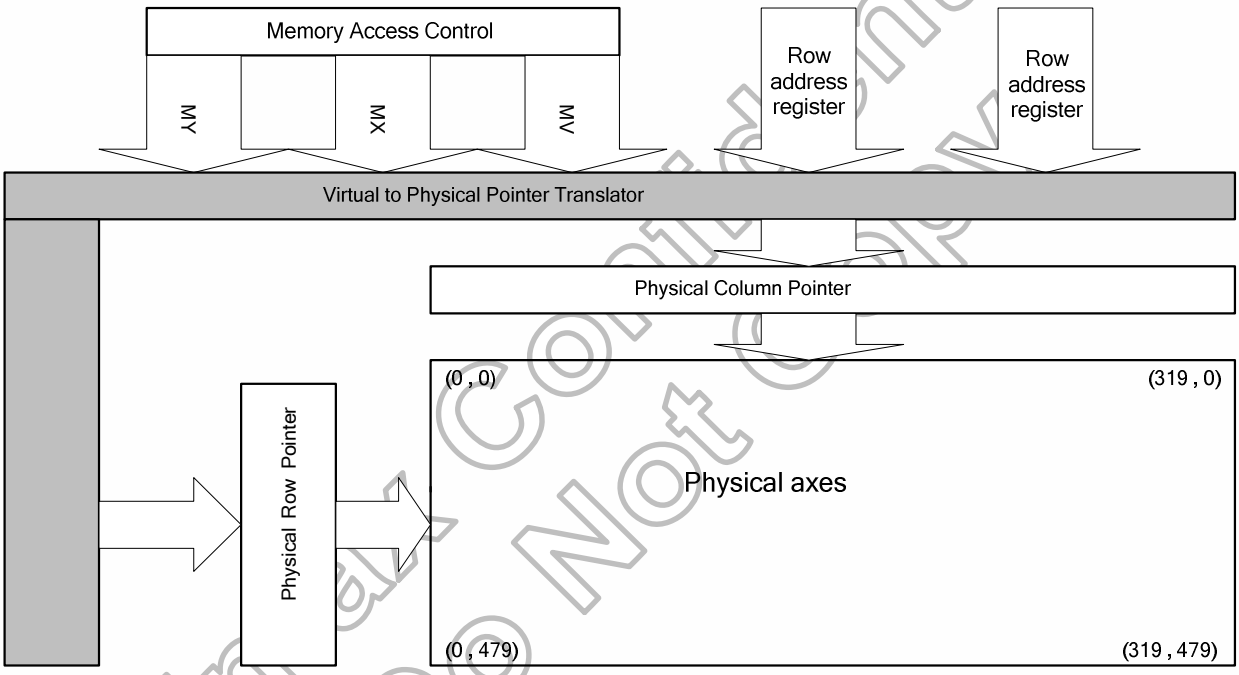


Figure 6. 2 MY, MX, MV Setting of 320RGB x 480 Dot

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (Y - Physical Page Pointer)
0	1	0	Direct to (X-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (X - Physical Column Pointer)	Direct to (Y - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (Y - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (X-Physical Column Pointer)
1	1	1	Direct to (Y - Physical Page Pointer)	Direct to (X - Physical Column Pointer)

Table 6. 3 CASET and PASET Control for Physical Column/Page Pointers

For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start Column"	Return to "Start Page"

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MX, MY, MV.

Table 6. 4 Rules for Updating GRAM Order

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

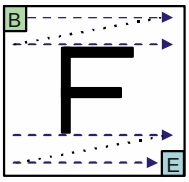
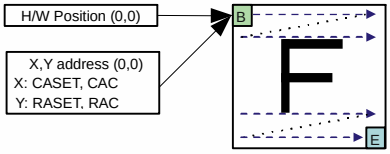
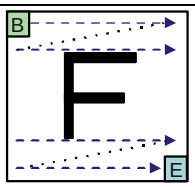
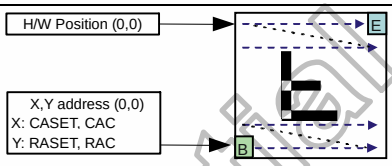
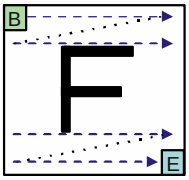
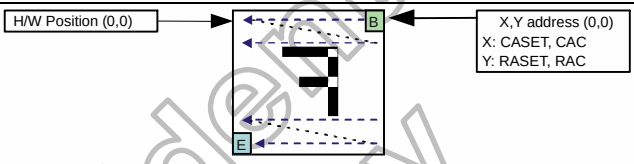
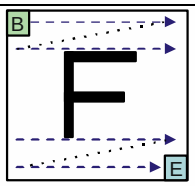
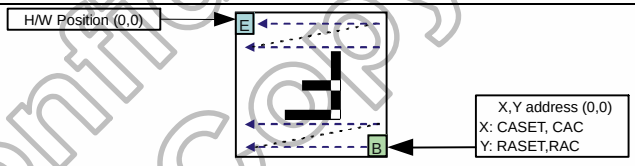
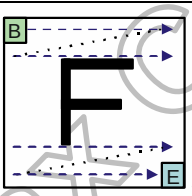
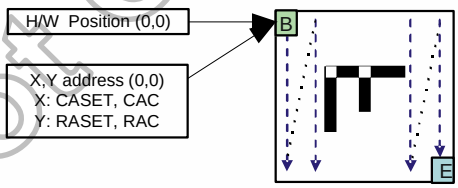
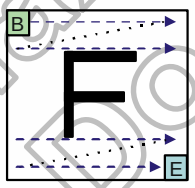
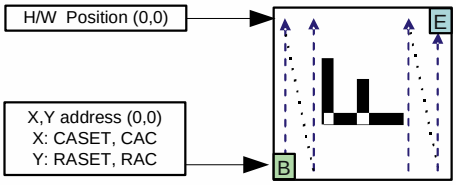
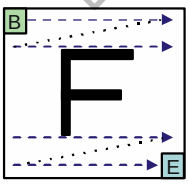
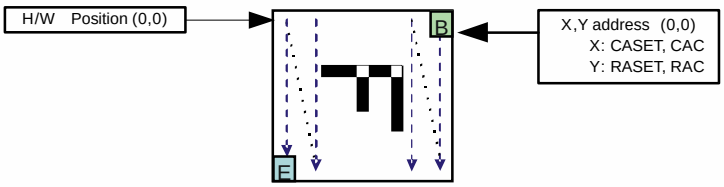
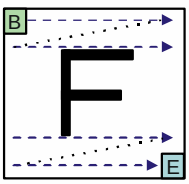
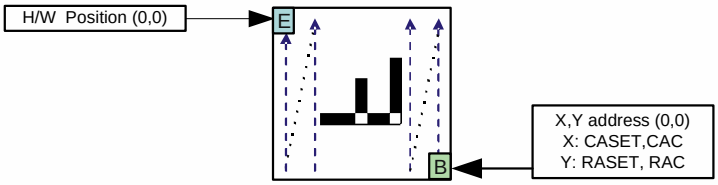
Display Data Direction	MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange X-invert	1	0	1		
X-Y Exchange Y-invert	1	1	0		
X-Y Exchange X-invert Y-invert	1	1	1		

Table 6. 5 Address Direction Settings

Example for rotation with MY, MX and MV

This example is using following values: start page = 0, end page = 40, start column = 0 and end column = 20 => commands: page address set (0, 40) and column address set (0, 20). The sent figure is as follows and its sending order is as follows.

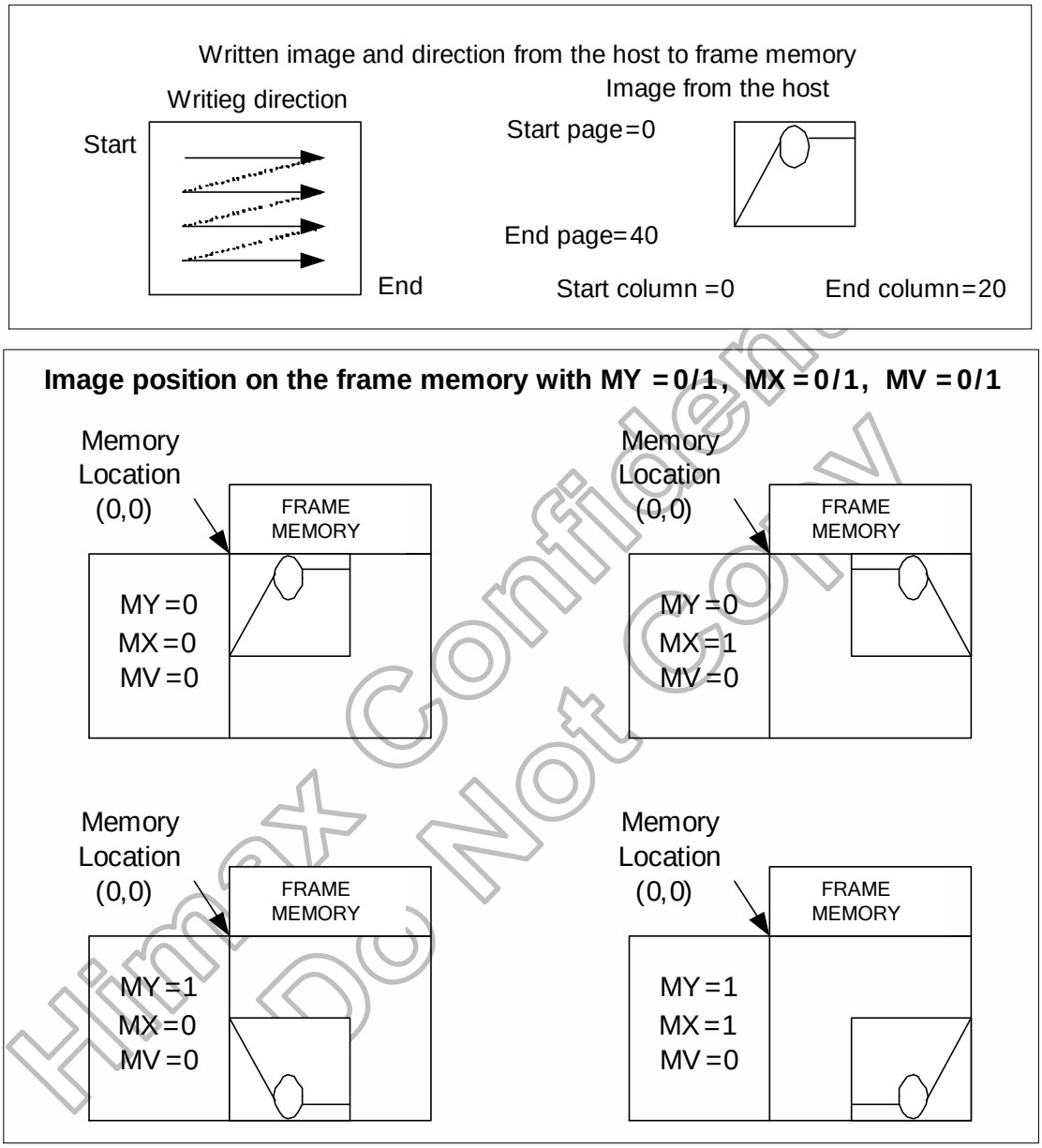
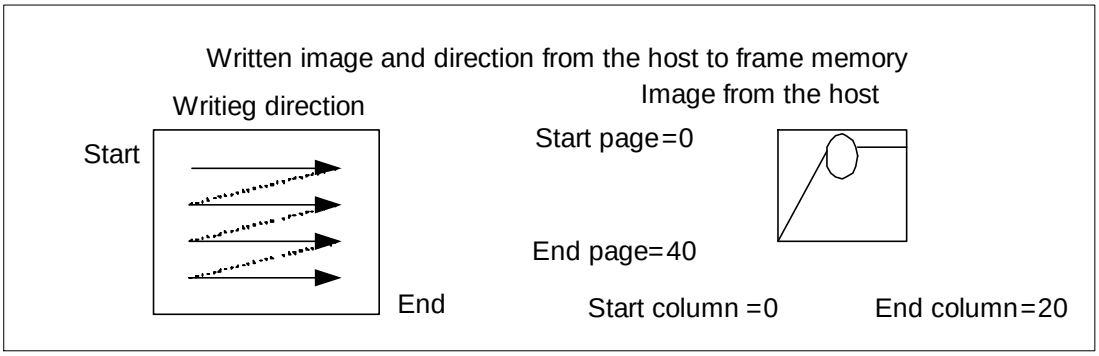


Figure 6. 3 Example for Rotation with MY, MX and MV – 1



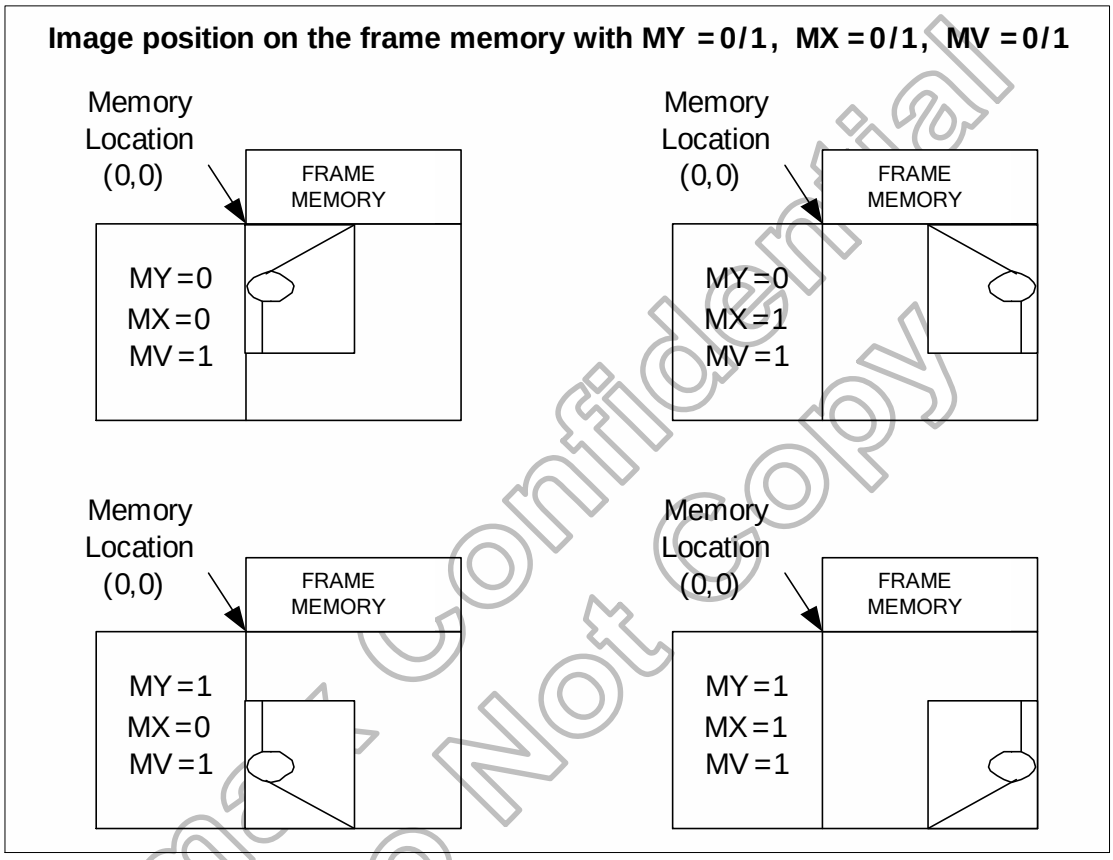


Figure 6. 4 Example for Rotation with MY, MX and MV - 2

6.3 GRAM to display address mapping

By setting the **SS** bit and **SMX**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** bit and **SMY**, the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR** bit and **SRGB**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement. Table 6.5, Table 6.6 and Table 6.7 show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

	SS	SMX	BGR='L' or SRGB = 'H'												
Source Output	0	1	S1	S2	S3	S4	S5	S6	-------	S955	S956	S957	S958	S959	S960
	1	0													
	0	0	S958	S959	S960	S955	S956	S957	-------	S4	S5	S6	S1	S2	S3
	1	1													
X Address			"00"h			"01"h			-------	"13E"h			"13F"h		
RGB data			R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel			Pixel 1			Pixel 2			-------	Pixel 319			Pixel 320		

	SS	SMX	BGR='H' or SRGB = 'L'												
Source Output	0	1	S3	S2	S1	S6	S5	S4	-------	S957	S956	S955	S960	S959	S958
	1	0													
	0	0	S960	S959	S958	S957	S956	S955	-------	S6	S5	S4	S3	S2	S1
	1	1													
X Address			"00"h			"01"h			-------	"13E"h			"13F"h		
Bit Allocation			R	G	B	R	G	B	-------	R	G	B	R	G	B
Pixel			Pixel 1			Pixel 2			-------	Pixel 319			Pixel 320		

Note: (1) RGB direction default setting is defined by the hardware pin SRGB.
(2) Register R16h[4](BGR) bit will override the hardware SRGB setting once software was sent to R16h[4](BGR) bit. Hardware pin SRGB control is invalid, and RGB filter order is controlled by R16h[4](BGR) bit.

Table 6. 6 GRAM X Address and Display Panel Position(320RGBx480 dot)

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S949	S950	S951	S952	S953	S954	S955	S956	S957	S958	S959	S960
G1	000000h			000001h			000002h			---	00013Ch			00013Dh			00013Eh			00013Fh		
G2	001000h			001001h			001002h			---	00113Ch			00113Dh			00113Eh			00113Fh		
G3	002000h			002001h			002002h			---	00213Ch			00213Dh			00213Eh			00213Fh		
G4	003000h			003001h			003002h			---	00313Ch			00313Dh			00313Eh			00313Fh		
G5	004000h			004001h			004002h			---	00413Ch			00413Dh			00413Eh			00413Fh		
G6	005000h			005001h			005002h			---	00513Ch			00513Dh			00513Eh			00513Fh		
G7	006000h			006001h			006002h			---	00613Ch			00613Dh			00613Eh			00613Fh		
G8	007000h			007001h			007002h			---	00713Ch			00713Dh			00713Eh			00713Fh		
G9	008000h			008001h			008002h			---	00813Ch			00813Dh			00813Eh			00813Fh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G471	1D6000h			1D6001h			1D6002h			---	1D613Ch			1D613Dh			1D613Eh			1D613Fh		
G472	1D7000h			1D7001h			1D7002h			---	1D713Ch			1D713Dh			1D713Eh			1D713Fh		
G473	1D8000h			1D8001h			1D8002h			---	1D813Ch			1D813Dh			1D813Eh			1D813Fh		
G474	1D9000h			1D9001h			1D9002h			---	1D913Ch			1D913Dh			1D913Eh			1D913Fh		
G475	1DA000h			1DA001h			1DA002h			---	1DA13Ch			1DA13Dh			1DA13Eh			1DA13Fh		
G476	1DB000h			1DB001h			1DB002h			---	1DB13Ch			1DB13Dh			1DB13Eh			1DB13Fh		
G477	1DC000h			1DC001h			1DC002h			---	1DC13Ch			1DC13Dh			1DC13Eh			1DC13Fh		
G478	1DD000h			1DD001h			1DD002h			---	1DD13Ch			1DD13Dh			1DD13Eh			1DD13Fh		
G479	1DE000h			1DE001h			1DE002h			---	1DE13Ch			1DE13Dh			1DE13Eh			1DE13Fh		
G480	1DF000h			1DF001h			1DF002h			---	1DF13Ch			1DF13Dh			1DF13Eh			1DF13Fh		

Table 6. 7 GRAM Address and Display Panel Position (SMY=L and GS=L, SMY=H and GS=H 320RGBx480 dot)

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S949	S950	S951	S952	S953	S954	S955	S956	S957	S958	S959	S960
G480	000000h			000001h			000002h			---	00013Ch			00013Dh			00013Eh			00013Fh		
G479	001000h			001001h			001002h			---	00113Ch			00113Dh			00113Eh			00113Fh		
G478	002000h			002001h			002002h			---	00213Ch			00213Dh			00213Eh			00213Fh		
G477	003000h			003001h			003002h			---	00313Ch			00313Dh			00313Eh			00313Fh		
G476	004000h			004001h			004002h			---	00413Ch			00413Dh			00413Eh			00413Fh		
G475	005000h			005001h			005002h			---	00513Ch			00513Dh			00513Eh			00513Fh		
G474	006000h			006001h			006002h			---	00613Ch			00613Dh			00613Eh			00613Fh		
G473	007000h			007001h			007002h			---	00713Ch			00713Dh			00713Eh			00713Fh		
G472	008000h			008001h			008002h			---	00813Ch			00813Dh			00813Eh			00813Fh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G10	1D6000h			1D6001h			1D6002h			---	1D613Ch			1D613Dh			1D613Eh			1D613Fh		
G9	1D7000h			1D7001h			1D7002h			---	1D713Ch			1D713Dh			1D713Eh			1D713Fh		
G8	1D8000h			1D8001h			1D8002h			---	1D813Ch			1D813Dh			1D813Eh			1D813Fh		
G7	1D9000h			1D9001h			1D9002h			---	1D913Ch			1D913Dh			1D913Eh			1D913Fh		
G6	1DA000h			1DA001h			1DA002h			---	1DA13Ch			1DA13Dh			1DA13Eh			1DA13Fh		
G5	1DB000h			1DB001h			1DB002h			---	1DB13Ch			1DB13Dh			1DB13Eh			1DB13Fh		
G4	1DC000h			1DC001h			1DC002h			---	1DC13Ch			1DC13Dh			1DC13Eh			1DC13Fh		
G3	1DD000h			1DD001h			1DD002h			---	1DD13Ch			1DD13Dh			1DD13Eh			1DD13Fh		
G2	1DE000h			1DE001h			1DE002h			---	1DE13Ch			1DE13Dh			1DE13Eh			1DE13Fh		
G1	1DF000h			1DF001h			1DF002h			---	1DF13Ch			1DF13Dh			1DF13Eh			1DF13Fh		

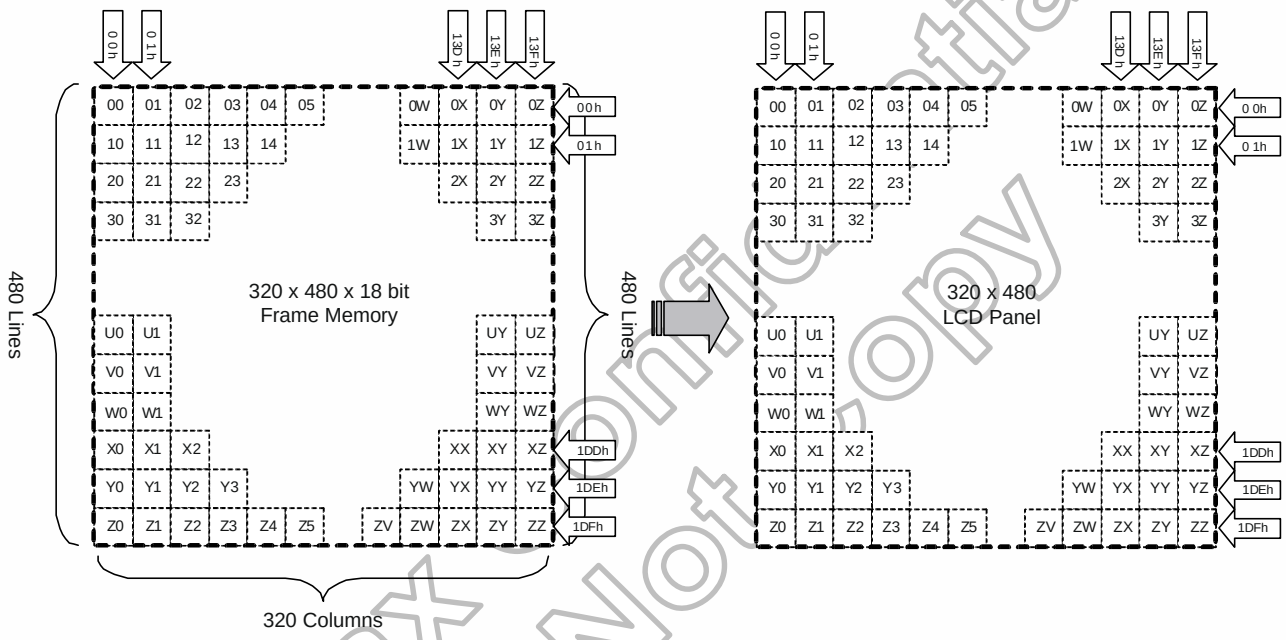
Table 6. 8 GRAM Address and Display Panel Position (SMY =H and GS=L, SMY =L and GS=H , 320RGBx480 dot)

HX8357-A supports three kinds of display mode: one is Normal Display Mode, another is Partial Display Mode, and Scrolling Display Mode.

When the **PLTON** = '0' is set, HX8357-A will be into Normal Display Mode. When the **PLTON** = '1' is set, HX8357-A will be into Partial Display Mode. When the **SCROL** = '1' is set, HX8357-A will be into Scrolling Display Mode.

6.3.1 Normal display on or partial Mode on, vertical scroll off

In this mode(320x480 dot), content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer is 0000h to 01DFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0) (**SMX** = 'L', **SMY** = 'L').



Example:

(1) **PLTON** = '1',

(2) PSL[15:0]=11_{DEC}, PEL[15:0]=130_{DEC}, (**SMY** = 'L').

(3) 320RGBx480 dot display mode.

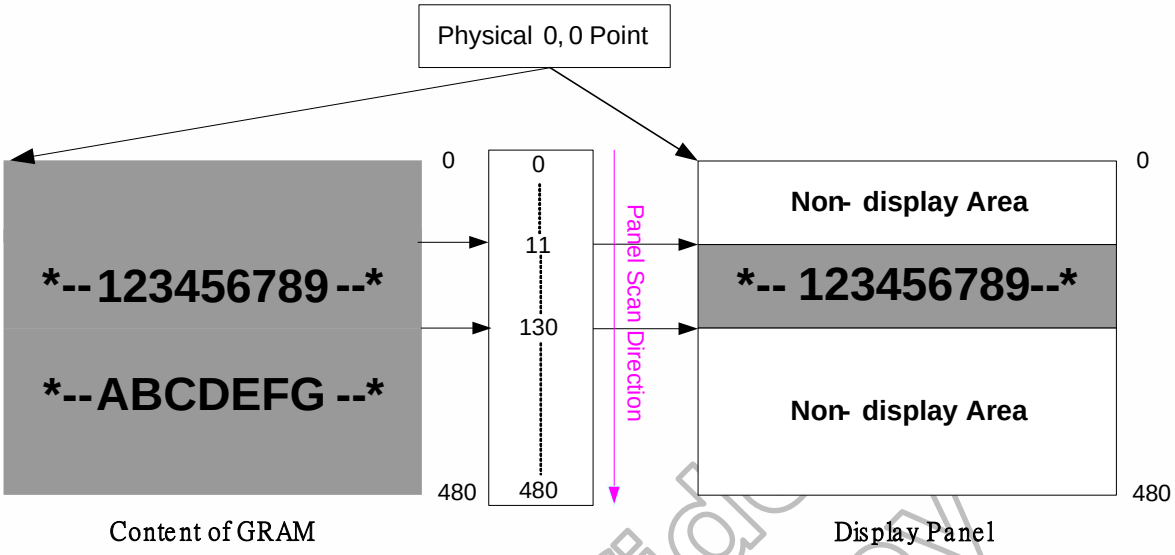


Figure 6. 5 Partial Display Area Setting (320x480 Panel)

The refresh gate scan cycle in the rest display area of the screen (non-display area) can be specified by **ISC[3:0]** bits. The scan cycle is set to an odd number from 0~13.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	3 frames	50ms
0	0	1	0	5 frames	83ms
0	0	1	1	7 frames	117ms
:	:	:	:	:	
1	1	0	0	25 frames	417ms
1	1	0	1	27 frames	450ms
1	1	1	0	29 frames	483ms
1	1	1	1	31 frames	517ms

Table 6. 9 ISC[3:0] Bits Definition

The rest display area (non-display area) will be the white display if the type of LCD is normally white **(INVON = "0")** and will be the black display if the type of LCD is normally black **(INVON = "1")** in refresh gate scan cycle.

6.3.2 Vertical scroll display mode

When **SCROL** bit is set to '1', the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA, BFA** bits (R0Eh ~R13h) and **VSP** bits (R14~R15h).

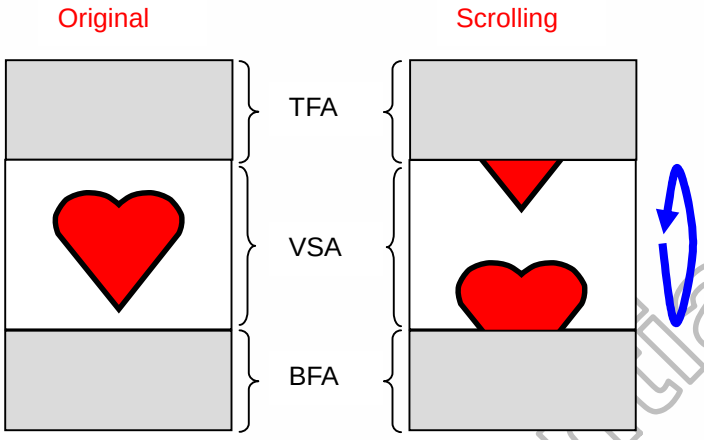


Figure 6. 6 Vertical Scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=320. In this case, scrolling is applied as shown below.

Example 1:

(1) TFA='2d', VSA='318d', BFA='0d', VSP='3d' (**SMX** = 'L', **SMY** = 'L')

(2) 320RGBx320 dot display mode.

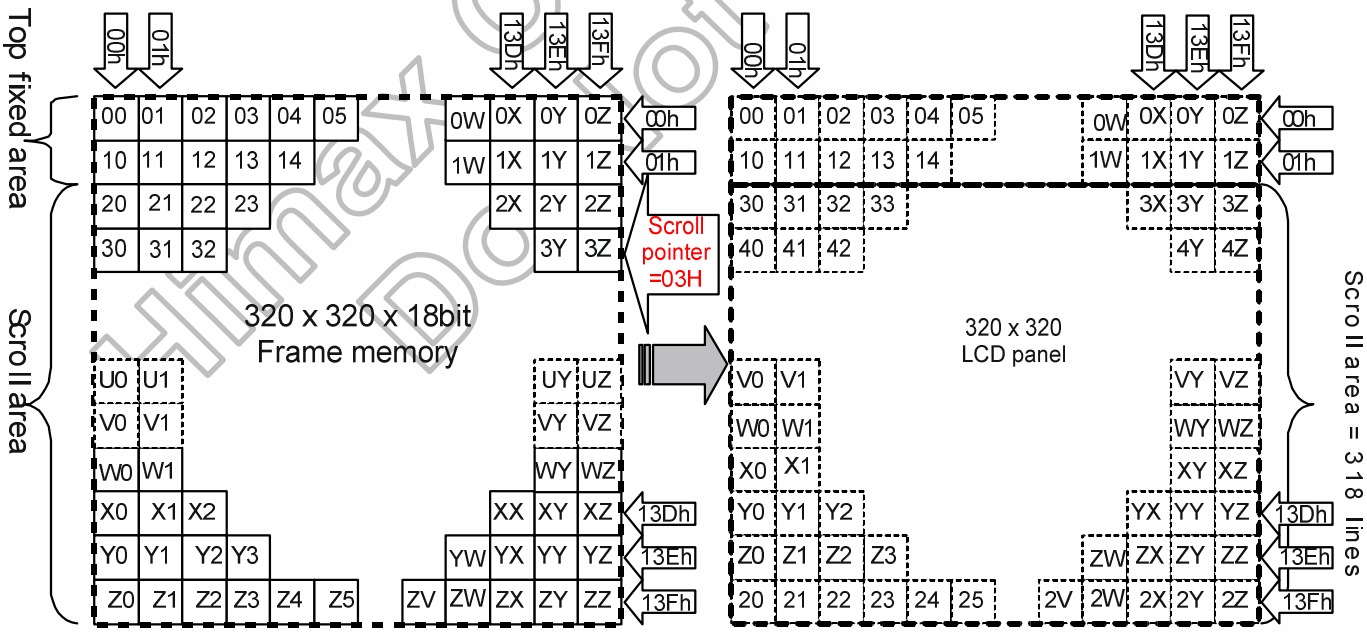


Figure 6. 7 Memory Map of Vertical Scrolling 1

Example 2:

(1) TFA='2d', VSA='316d', BFA='2d', VSP='3d' (**SMX** = 'L', **SMY** = 'L')
(2) 320RGBx320 dot display mode

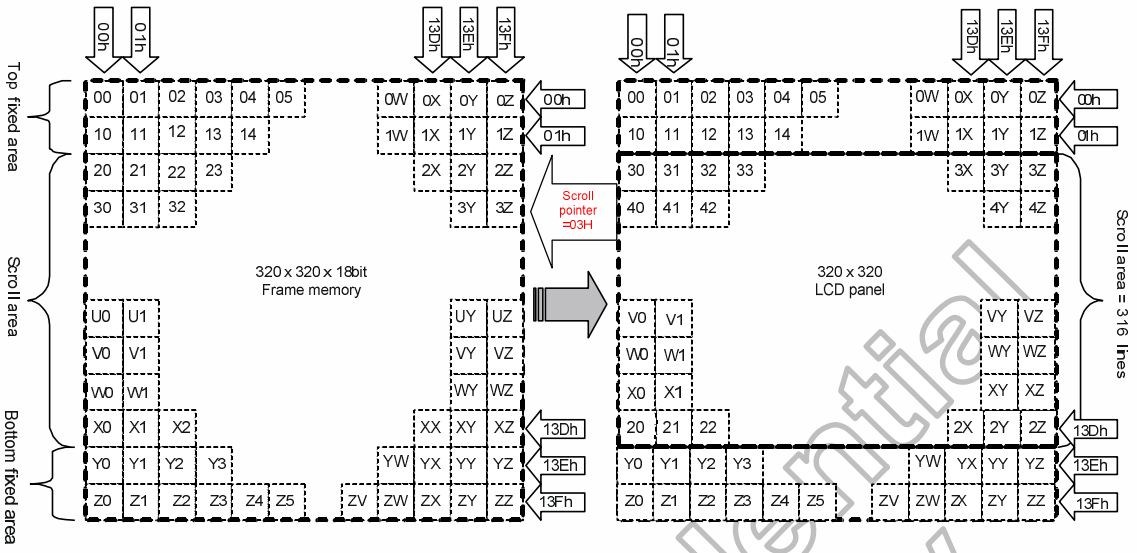


Figure 6. 8 Memory Map of Vertical Scrolling 2

Example 3:

(1) TFA='2d', VSA='316d', BFA='2d', VSP='5d' (**SMX** = 'L', **SMY** = 'L').
(2) 320RGBx320 dot display mode

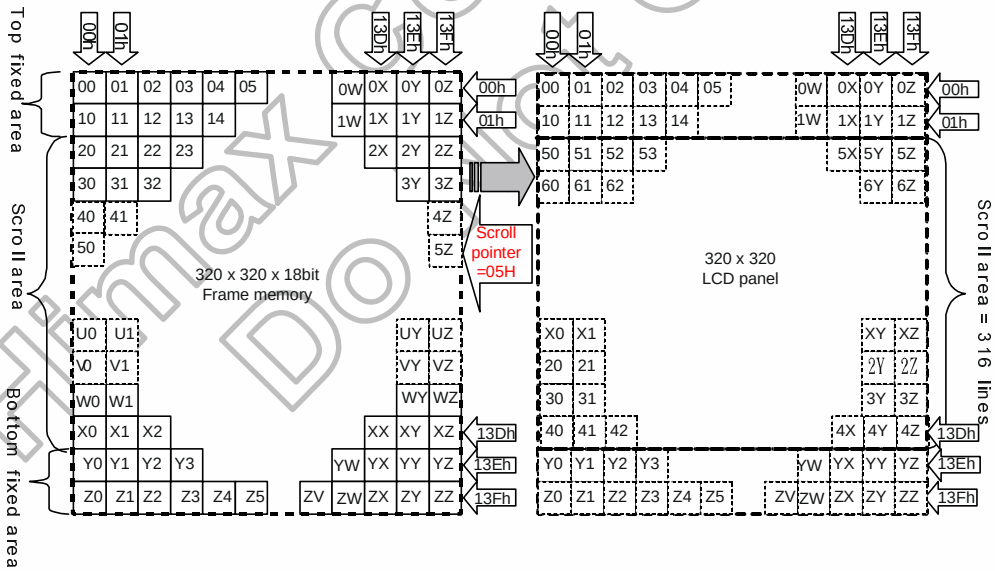


Figure 6. 9 Memory Map of Vertical Scrolling 3

Vertical scroll example

There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits (R0Eh ~R13h) and **VSP** bits (R14~R15h).

Case 1: TFA + VSA + BFA ≠ '320d'

N/A. Do not set TFA + VSA + BFA ≠ '320d'. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA = '320d' (Scrolling)

Example : (1) When TFA='0d', VSA='320d', BFA='0d' and VSP='40d' (**SMX** = 'L', **SMY** = 'L')
(2) 320RGBx320 dot display mode

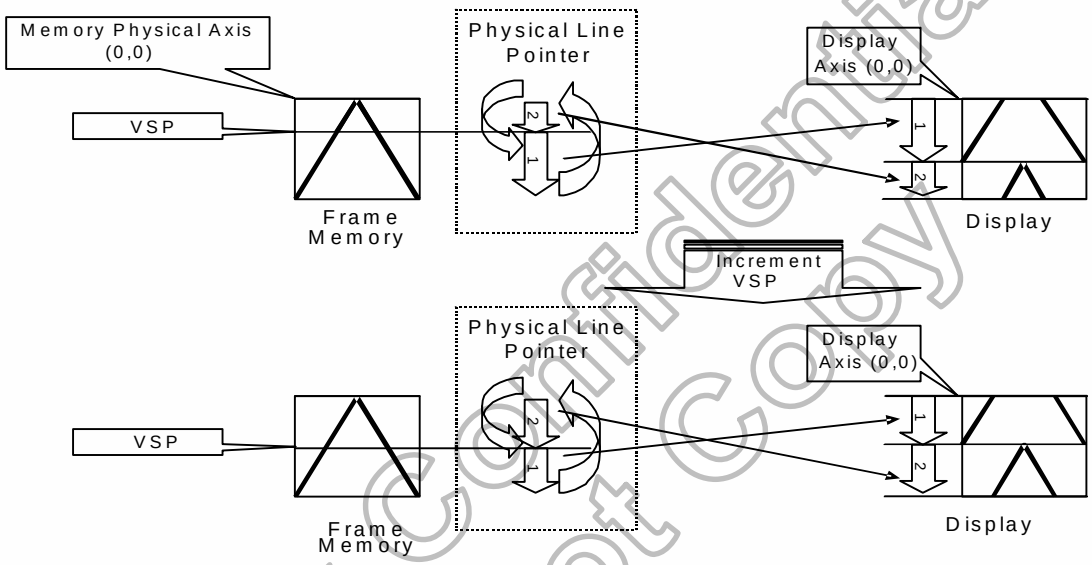


Figure 6. 10 Vertical Scrolling Example

6.3.3 Updating order on display active area in RGB interface mode

There is defined different kind of updating orders for display in RGB interface mode (**RCM[1:0]**='1x'). These updating are controlled by **MY** and **MX** bits.

Data streaming direction from the host to the display is described in the following figure.

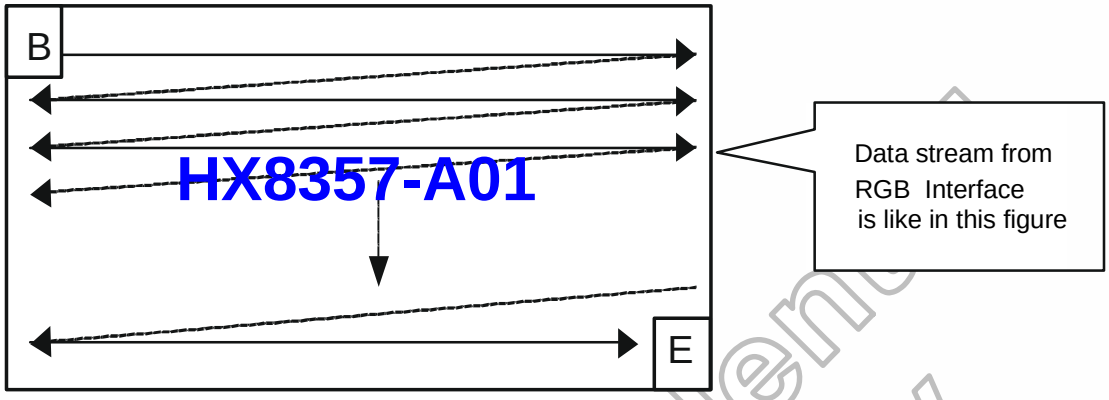


Figure 6. 11 Data Streaming Order in RGB I/F

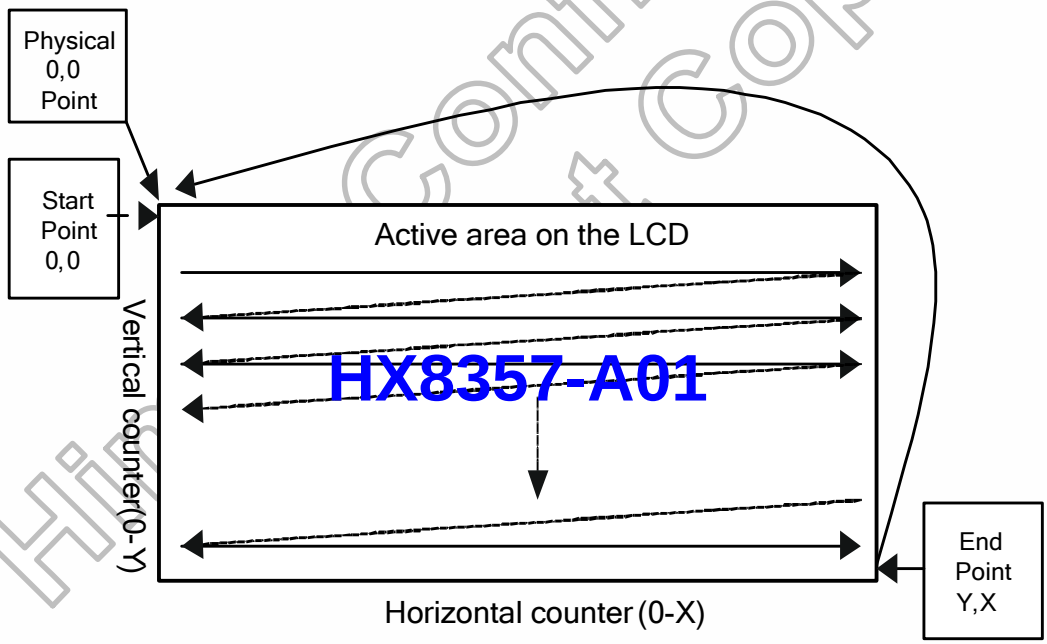


Figure 6. 12 Updating Order When MY = '0' and MX = '0'

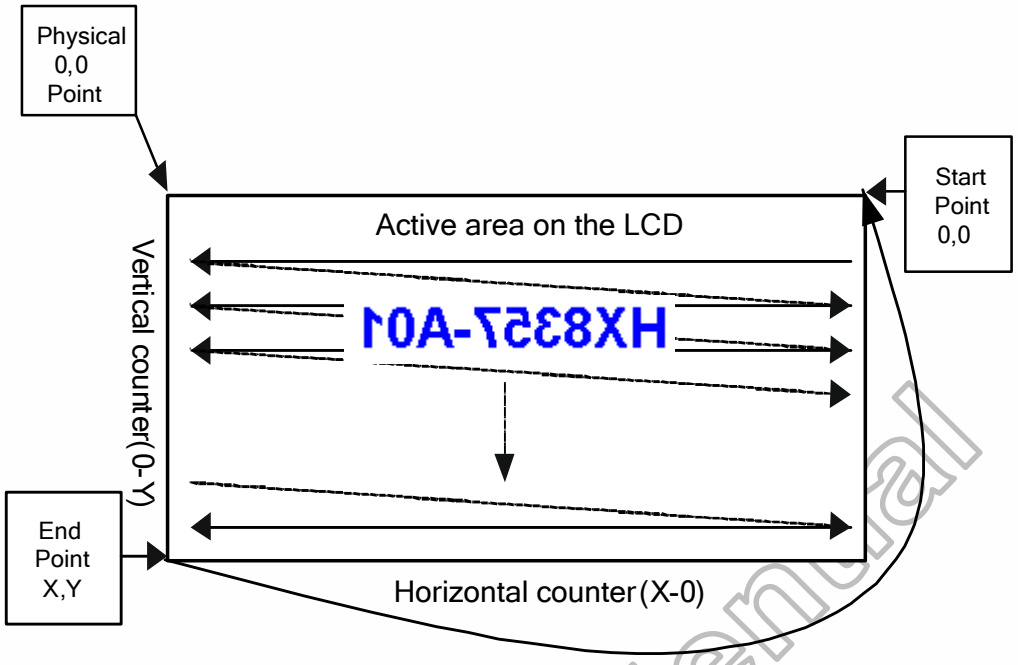


Figure 6. 13 Updating Order When MY = '0' and MX = '1'

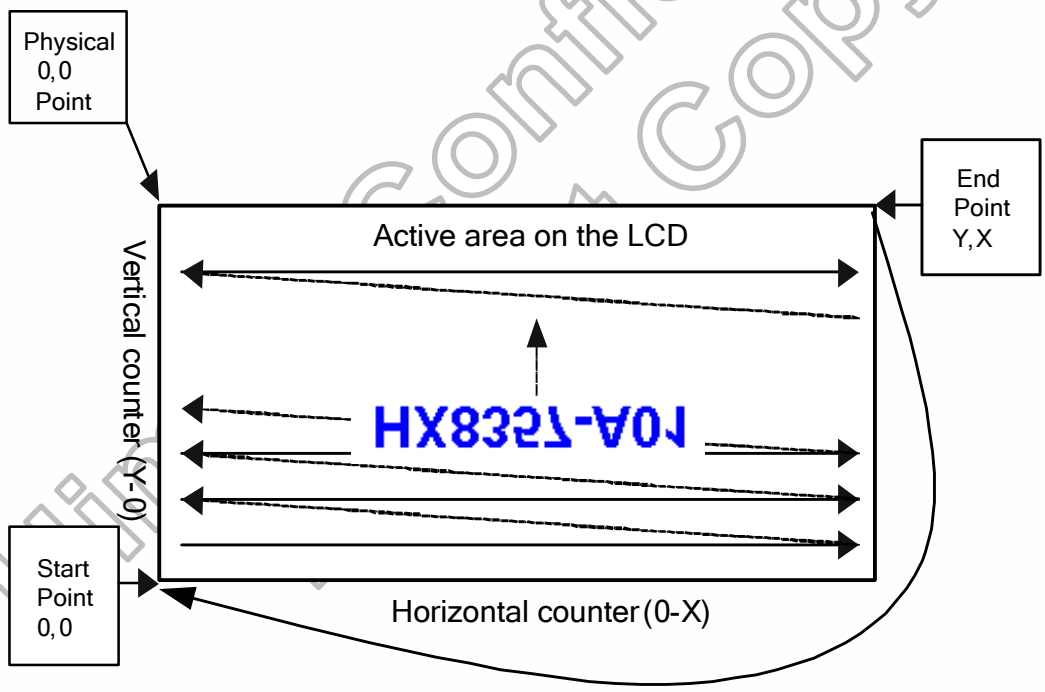


Figure 6. 14 Updating Order When MY = '1' and MX = '0'

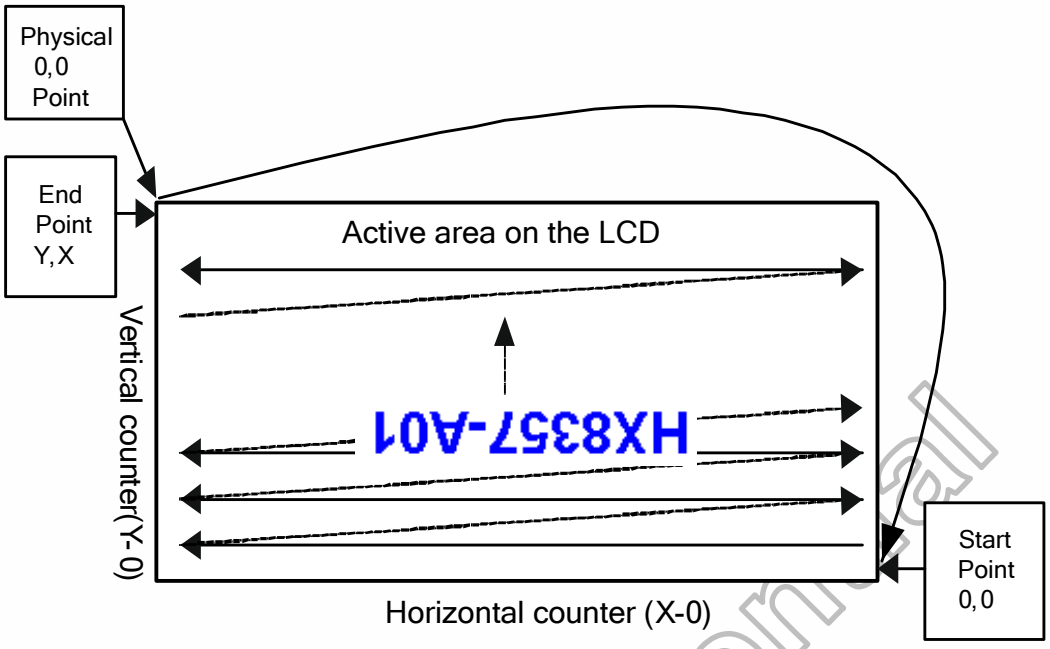


Figure 6. 15 Updating Order When MY = '1' and MX = '1'

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to "Start Column"	Return to "Start Page"

Note: Pixel order is RGB on the display.

Table 6. 10 Rules for Updating Order on Display Active Area in RGB Interface Display Mode

7. Functional Description

7.1 Internal oscillator

The HX8357-A can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is ±5%, **RADJ [3:0]** bits for initial 5.2MHz internal clock generation. With other dividers setting, the 5.2MHz internal clock can be used to generate clock for other part of the chip using.

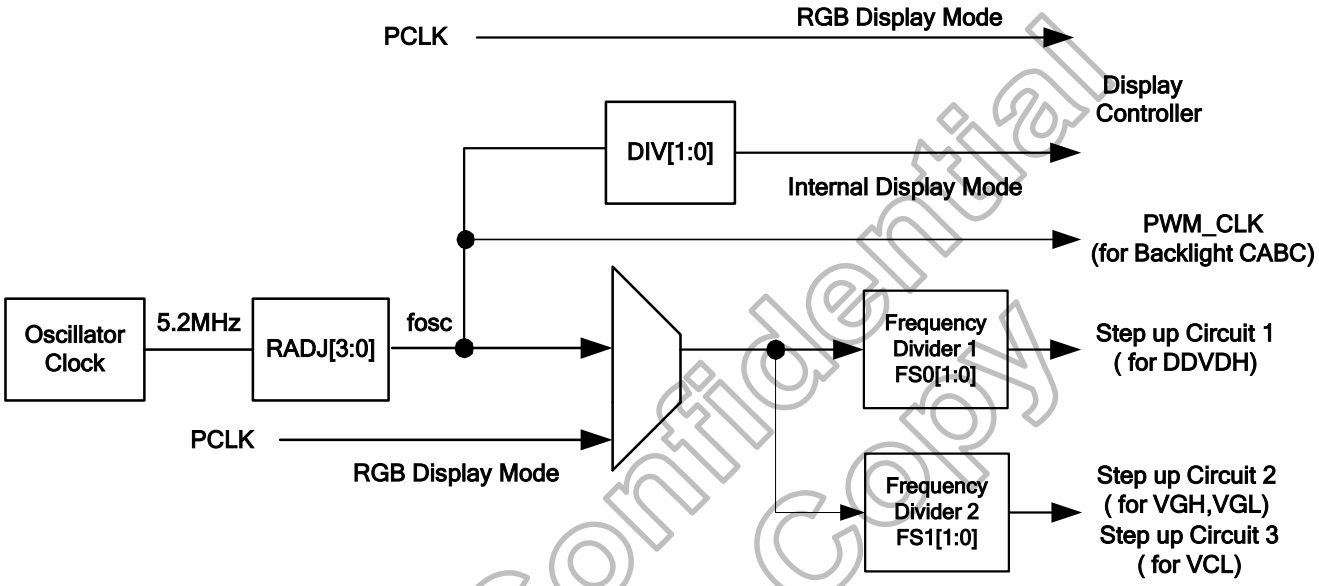
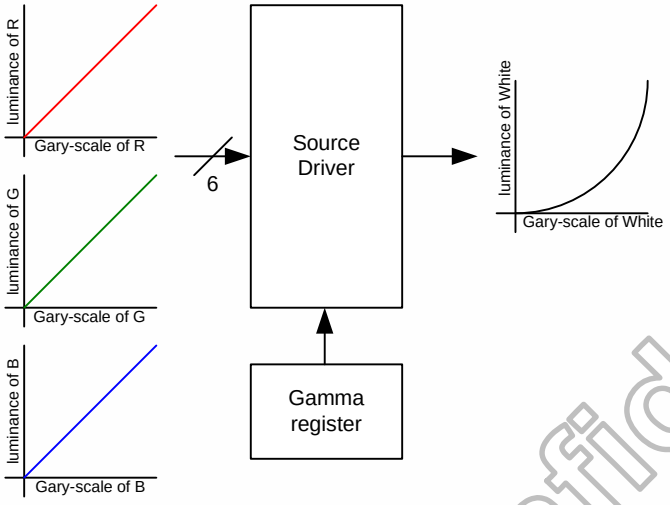


Figure 7. 1 HX8357-A Internal Clock Circuit

7.2 Gamma characteristic correction function

The HX8357-A offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is select by internal register DGC_EN bit.

A) Gamma adjustment of Source Driver



B) Gamma adjustment of Digital Gamma Correction

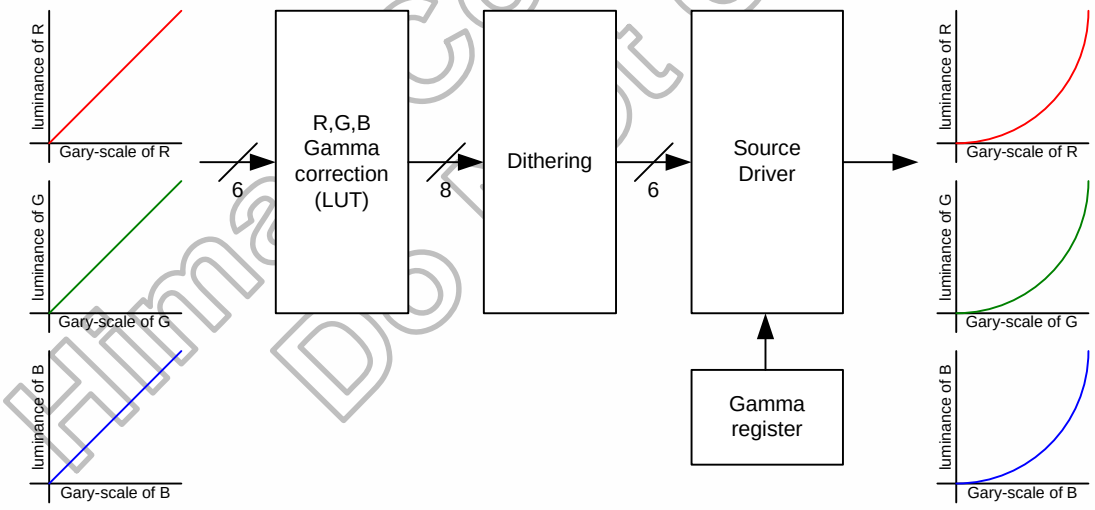


Figure 7. 2 Gamma Adjustments Different of Source Driver with Digital Gamma Correction

7.2.1 Gray voltage generator for source driver

The HX8357-A incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

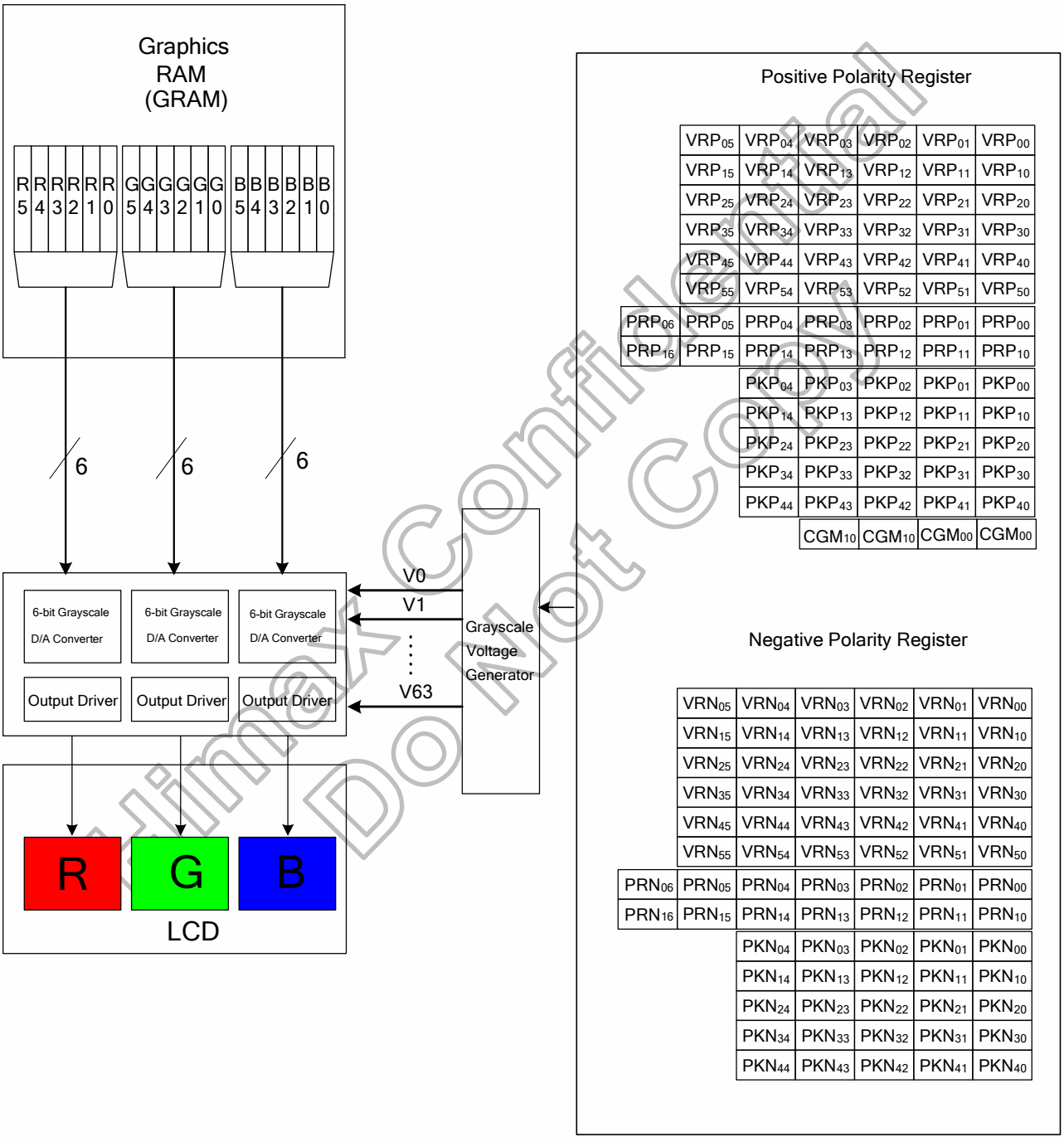


Figure 7. 3 Grayscale Control

7.2.1.1 Structure of grayscale voltage generator

Eight reference gamma voltages (RVP 0, 1, 8, 20, 43, 55, 62 and 63). For positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

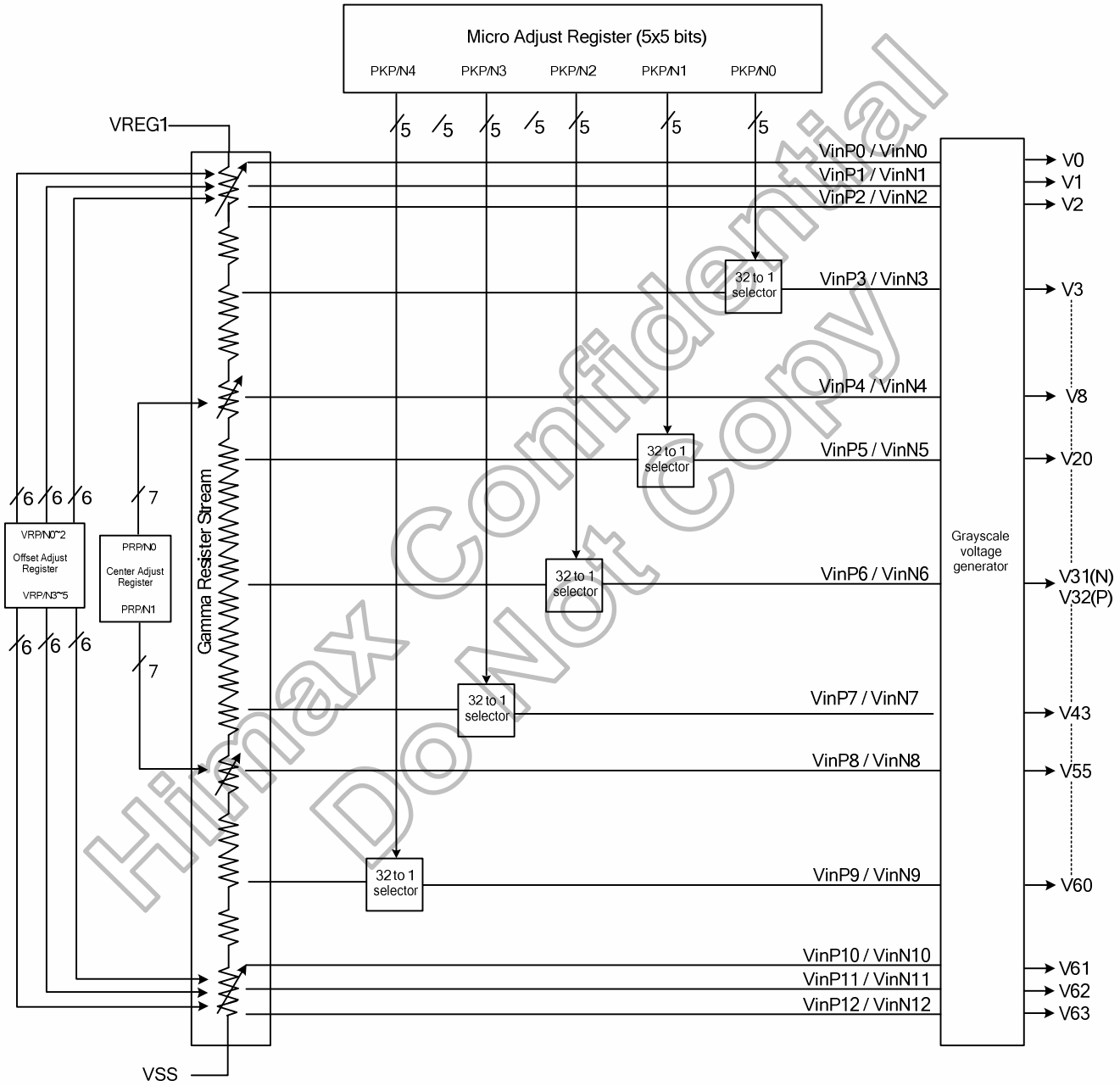


Figure 7. 4 Structure of Grayscale Voltage Generator

7.2.1.2 Gamma-characteristics adjustment register

This HX8357-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common).

Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 128-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

7.2.1.3 Gamma macro adjustment registers

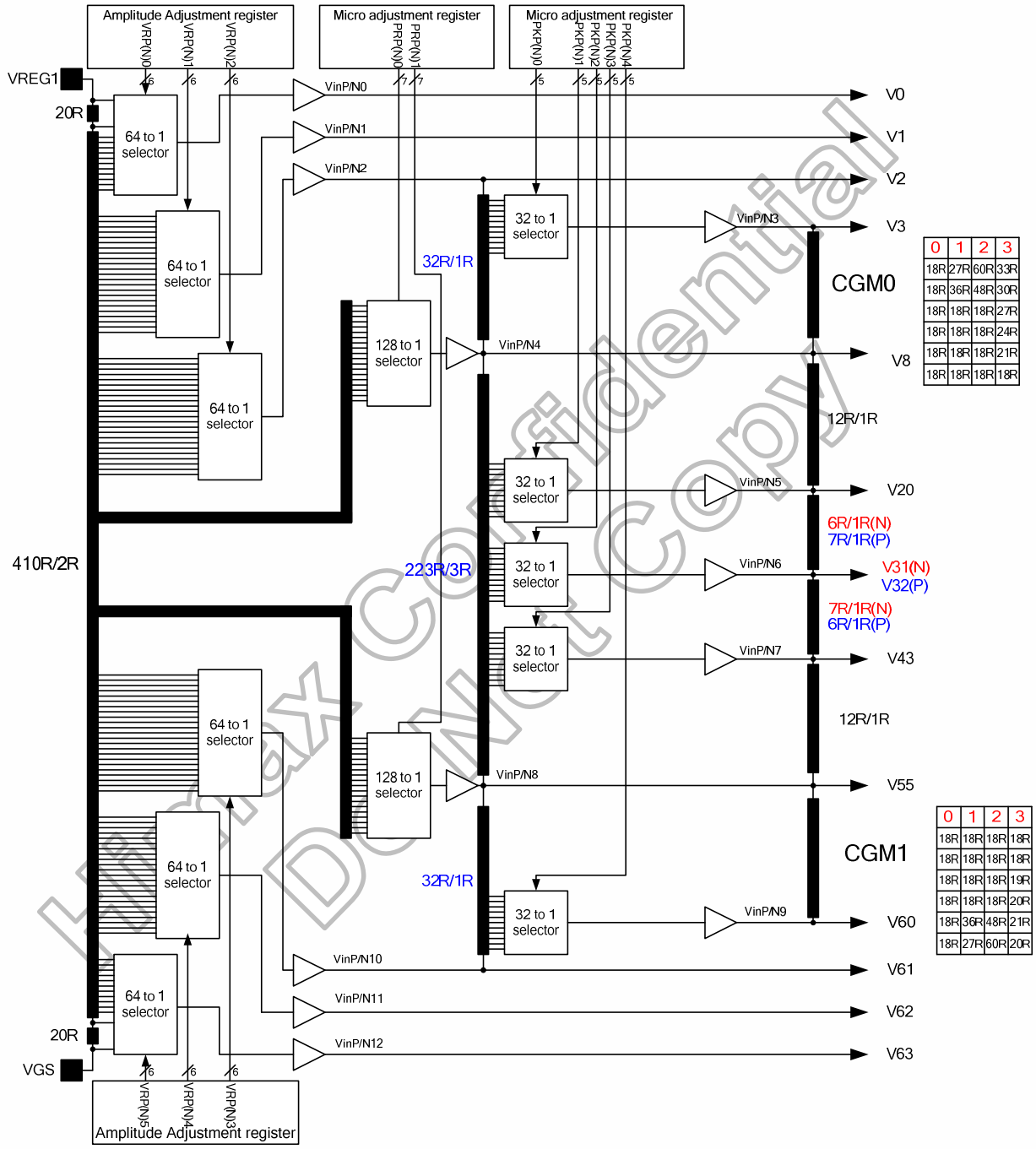
The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output (Vg(P/N) 3, 20, 32(31), 43, 60).

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor (PRP/N1)for center adjustment
Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 20)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 43)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment
	VRP1 5-0	VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment
	VRP5 5-0	VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment

Figure 7. 5 Gamma-Adjustment Registers

7.2.1.4 Gamma resister stream and 8 to 1 selector

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. VgP/N (0, 1, 2, 3, 8 20, 32(31), 43, 55, 60, 61, 62, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.



0	1	2	3
18R	27R	60R	33R
18R	36R	48R	30R
18R	18R	18R	27R
18R	18R	18R	24R
18R	18R	18R	21R
18R	18R	18R	18R

0	1	2	3
18R	18R	18R	18R
18R	18R	18R	18R
18R	18R	18R	19R
18R	18R	18R	20R
18R	36R	48R	21R
18R	27R	60R	20R

Figure 7. 6 Gamma Resister Stream and Gamma Reference Voltage

7.2.1.5 Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0
000000	0R
000001	20R
000010	22R
000011	24R
•	•
•	•
011101	76R
011110	78R
011111	80R
100000	84R
100001	88R
100010	92R
•	•
•	•
111101	200R
111110	204R
111111	208R

Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1
000000	0R
000001	2R
000010	4R
000011	6R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
•	•
•	•
111101	182R
111110	186R
111111	190R

Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
000011	6R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
•	•
•	•
111101	182R
111110	186R
111111	190R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3
000000	0R
000001	4R
000010	8R
•	•
•	•
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
•	•
•	•
111100	184R
111101	186R
111110	188R
111111	190R

Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4
000000	0R
000001	4R
000010	8R
•	•
•	•
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
•	•
•	•
111100	184R
111101	186R
111110	188R
111111	190R

Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R
000001	4R
000010	8R
•	•
•	•
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
•	•
•	•
111100	184R
111101	186R
111110	188R
111111	208R

Figure 7. 7 Offset Adjustment 0~5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0
0000000	0R
0000001	2R
0000010	4R
•	•
•	•
1111101	250R
1111110	252R
1111111	254R

Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R
0000001	2R
0000010	4R
•	•
•	•
1010101	250R
1111110	252R
1111111	254R

Table 7. 1 Center Adjustment

The grayscale levels are determined by the following formulas:

Reference Voltage	Macro Adjustment Value	VinP/N0 Formula
VinP/N0	VRP/N0 5-0 = 000000	VREG1
	VRP/N0 5-0 = 000001	((450R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000010	((450R - 22R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000011	((450R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000100	((450R - 26R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000101	((450R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000110	((450R - 30R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000111	((450R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001000	((450R - 34R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001001	((450R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001010	((450R - 38R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001011	((450R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001100	((450R - 42R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001101	((450R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001110	((450R - 46R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001111	((450R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010000	((450R - 50R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010001	((450R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010010	((450R - 54R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010011	((450R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010100	((450R - 58R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010101	((450R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010110	((450R - 62R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010111	((450R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011000	((450R - 66R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011001	((450R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011010	((450R - 70R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011011	((450R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011100	((450R - 74R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011101	((450R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011110	((450R - 78R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011111	((450R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100000	((450R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100001	((450R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100010	((450R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100011	((450R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100100	((450R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100101	((450R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100110	((450R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100111	((450R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101000	((450R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101001	((450R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101010	((450R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101011	((450R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101100	((450R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101101	((450R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101110	((450R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101111	((450R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110000	((450R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110001	((450R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110010	((450R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110011	((450R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110100	((450R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110101	((450R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110110	((450R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110111	((450R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111000	((450R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111001	((450R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111010	((450R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111011	((450R - 192R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111100	((450R - 196R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111101	((450R - 200R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111110	((450R - 204R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111111	((450R - 208R) / 450R) * (VREG1 - VGS) + VGS

Table 7. 2 Voltage Calculation Formula for VinP/N 0

The grayscale levels are determined by the following formulas:

Reference Voltage	Macro Adjustment Value	VinP/N0 Formula
VinP/N0	VRP/N0 5-0 = 000000	VREG1
	VRP/N0 5-0 = 000001	((450R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000010	((450R - 22R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000011	((450R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000100	((450R - 26R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000101	((450R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000110	((450R - 30R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 000111	((450R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001000	((450R - 34R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001001	((450R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001010	((450R - 38R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001011	((450R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001100	((450R - 42R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001101	((450R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001110	((450R - 46R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 001111	((450R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010000	((450R - 50R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010001	((450R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010010	((450R - 54R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010011	((450R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010100	((450R - 58R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010101	((450R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010110	((450R - 62R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 010111	((450R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011000	((450R - 66R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011001	((450R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011010	((450R - 70R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011011	((450R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011100	((450R - 74R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011101	((450R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011110	((450R - 78R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 011111	((450R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100000	((450R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100001	((450R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100010	((450R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100011	((450R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100100	((450R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100101	((450R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100110	((450R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 100111	((450R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101000	((450R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101001	((450R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101010	((450R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101011	((450R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101100	((450R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101101	((450R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101110	((450R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 101111	((450R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110000	((450R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110001	((450R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110010	((450R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110011	((450R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110100	((450R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110101	((450R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110110	((450R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 110111	((450R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111000	((450R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111001	((450R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111010	((450R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111011	((450R - 192R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111100	((450R - 196R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111101	((450R - 200R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111110	((450R - 204R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N0 5-0 = 111111	((450R - 208R) / 450R) * (VREG1 - VGS) + VGS

Table 7. 3 Voltage Calculation Formula for VinP/N 0

Reference Voltage	Macro Adjustment Value	VinP/N1 Formula
VinP/N1	VRP/N1 5-0 = 000000	(430R / 450R) * (VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000001	((430R - 2R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000010	((430R - 4R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000011	((430R - 6R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000100	((430R - 8R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000101	((430R - 10R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000110	((430R - 12R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 000111	((430R - 14R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001000	((430R - 16R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001001	((430R - 18R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001010	((430R - 20R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001011	((430R - 22R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001100	((430R - 24R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001101	((430R - 26R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001110	((430R - 28R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 001111	((430R - 30R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010000	((430R - 32R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010001	((430R - 34R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010010	((430R - 36R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010011	((430R - 38R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010100	((430R - 40R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010101	((430R - 42R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010110	((430R - 44R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 010111	((430R - 46R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011000	((430R - 48R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011001	((430R - 50R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011010	((430R - 52R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011011	((430R - 54R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011100	((430R - 56R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011101	((430R - 58R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011110	((430R - 60R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 011111	((430R - 62R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100000	((430R - 66R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100001	((430R - 70R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100010	((430R - 74R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100011	((430R - 78R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100100	((430R - 82R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100101	((430R - 86R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100110	((430R - 90R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 100111	((430R - 94R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101000	((430R - 98R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101001	((430R - 102R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101010	((430R - 106R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101011	((430R - 110R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101100	((430R - 114R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101101	((430R - 118R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101110	((430R - 122R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 101111	((430R - 126R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110000	((430R - 130R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110001	((430R - 134R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110010	((430R - 138R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110011	((430R - 142R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110100	((430R - 146R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110101	((430R - 150R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110110	((430R - 154R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 110111	((430R - 158R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111000	((430R - 162R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111001	((430R - 166R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111010	((430R - 170R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111011	((430R - 174R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111100	((430R - 178R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111101	((430R - 182R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111110	((430R - 186R) / 450R) *(VREG1 - VGS) + VGS
	VRP/N1 5-0 = 111111	((430R - 190R) / 450R) *(VREG1 - VGS) + VGS

Table 7. 4 Voltage Calculation Formula for VinP/N 1

Reference Voltage	Macro Adjustment Value	VinP/N2 Formula
VinP/N2	VRP/N2 5-0 = 000000	(410R / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000001	((410R - 2R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000010	((410R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000011	((410R - 6R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000100	((410R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000101	((410R - 10R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000110	((410R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 000111	((410R - 14R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001000	((410R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001001	((410R - 18R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001010	((410R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001011	((410R - 22R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001100	((410R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001101	((410R - 26R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001110	((410R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 001111	((410R - 30R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010000	((410R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010001	((410R - 34R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010010	((410R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010011	((410R - 38R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010100	((410R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010101	((410R - 42R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010110	((410R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 010111	((410R - 46R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011000	((410R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011001	((410R - 50R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011010	((410R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011011	((410R - 54R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011100	((410R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011101	((410R - 58R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011110	((410R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 011111	((410R - 62R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100000	((410R - 66R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100001	((410R - 70R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100010	((410R - 74R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100011	((410R - 78R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100100	((410R - 82R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100101	((410R - 86R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100110	((410R - 90R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 100111	((410R - 94R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101000	((410R - 98R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101001	((410R - 102R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101010	((410R - 106R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101011	((410R - 110R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101100	((410R - 114R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101101	((410R - 118R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101110	((410R - 122R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 101111	((410R - 126R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110000	((410R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110001	((410R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110010	((410R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110011	((410R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110100	((410R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110101	((410R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110110	((410R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 110111	((410R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111000	((410R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111001	((410R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111010	((410R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111011	((410R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111100	((410R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111101	((410R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111110	((410R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N2 5-0 = 111111	((410R - 190R) / 450R) * (VREG1 - VGS) + VGS

Table 7. 5 Voltage Calculation Formula for VinP/N 2

Reference Voltage	Macro Adjustment Value	VinP/N3 Formula
VinP/N3	PKP/N0 4-0 = 00000	(31R / 32R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00001	((31R – 1R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00010	((31R – 2R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00011	((31R – 3R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00100	((31R – 4R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00101	((31R – 5R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00110	((31R – 6R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00111	((31R – 7R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01000	((31R – 8R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01001	((31R – 9R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01010	((31R - 10R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01011	((31R - 11R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01100	((31R - 12R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01101	((31R - 13R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01110	((31R - 14R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01111	((31R - 15R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10000	((31R - 16R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10001	((31R - 17R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10010	((31R - 18R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10011	((31R - 19R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10100	((31R - 20R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10101	((31R - 21R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10110	((31R - 22R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10111	((31R - 23R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11000	((31R - 24R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11001	((31R - 25R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11010	((31R - 26R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11011	((31R - 27R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11100	((31R - 28R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11101	((31R - 29R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11110	((31R - 30R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11111	((31R - 31R) / 48R) * (VinP/N2 - VinP/N4) + VinP/N4

Table 7. 6 Voltage Calculation Formula for VinP/N 3

Reference Voltage	Macro Adjustment Value	VinP/N4 Formula
VinP/N4	PRP/N0 6-0 = 0000000	(350R / 450R) (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000001	((350R - 2R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000010	((350R - 4R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000011	((350R – 6R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000100	((350R – 8R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000101	((350R – 10R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000110	((350R – 12R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0000111	((350R - 14R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001000	((350R – 16R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001001	((350R – 18R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001010	((350R – 20R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001011	((350R – 22R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001100	((350R – 24R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001101	((350R – 26R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001110	((350R – 28R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0001111	((350R – 30R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010000	((350R – 32R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010001	((350R - 34R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010010	((350R – 36R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010011	((350R – 38R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010100	((350R – 40R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010101	((350R – 42R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010110	((350R – 44R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0010111	((350R – 46R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011000	((350R – 48R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011001	((350R – 50R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011010	((350R – 52R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011011	((350R - 54R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011100	((350R – 56R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011101	((350R – 58R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011110	((350R – 60R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0011111	((350R – 62R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100000	((350R - 64R) / 450R) * (VREG1 - VGS) + VGS

	PRP/N0 6-0 = 0100001	((350R – 66R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100010	((350R – 68R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100011	((350R – 70R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100100	((350R – 72R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100101	((350R – 74R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100110	((350R – 76R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0100111	((350R – 78R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101000	((350R – 80R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101001	((350R – 82R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101010	((350R - 84R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101011	((350R – 86R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101100	((350R – 88R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101101	((350R – 90R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101110	((350R – 92R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0101111	((350R – 94R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110000	((350R – 96R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110001	((350R – 98R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110010	((350R – 100R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110011	((350R – 102R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110100	((350R – 104R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110101	((350R – 106R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110110	((350R – 108R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0110111	((350R – 110R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111000	((350R – 112R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111001	((350R – 114R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111010	((350R – 116R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111011	((350R – 118R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111100	((350R – 120R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111101	((350R – 122R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111110	((350R - 124R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 0111111	((350R – 126R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000000	((350R – 128R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000001	((350R – 130R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000010	((350R - 132R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000011	((350R – 134R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000100	((350R – 136R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000101	((350R – 138R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000110	((350R – 140R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1000111	((350R – 142R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001000	((350R – 144R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001001	((350R – 146R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001010	((350R – 148R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001011	((350R – 150R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001100	((350R - 152R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001101	((350R – 154R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001110	((350R – 156R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1001111	((350R – 158R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010000	((350R – 160R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010001	((350R – 162R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010010	((350R – 164R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010011	((350R – 166R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010100	((350R – 168R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010101	((350R – 170R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010110	((350R – 172R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1010111	((350R - 174R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011000	((350R – 176R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011001	((350R – 178R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011010	((350R – 180R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011011	((350R – 182R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011100	((350R – 184R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011101	((350R – 186R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011110	((350R – 188R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1011111	((350R – 190R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100000	((350R – 192R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100001	((350R – 194R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100010	((350R – 196R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100011	((350R – 198R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100100	((350R – 200R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100101	((350R – 202R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100110	((350R – 204R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1100111	((350R – 206R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101000	((350R – 208R) / 450R) * (VREG1 - VGS) + VGS

	PRP/N0 6-0 = 1101001	((350R – 210R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101010	((350R – 212R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101011	((350R – 214R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101100	((350R – 216R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101101	((350R – 218R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101110	((350R – 220R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1101111	((350R – 223R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110000	((350R – 224R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110001	((350R – 226R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110010	((350R – 228R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110011	((350R – 230R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110100	((350R – 232R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110101	((350R – 234R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110110	((350R – 236R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1110111	((350R – 238R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111000	((350R – 240R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111001	((350R – 243R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111010	((350R – 244R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111011	((350R – 246R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111100	((350R – 248R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111101	((350R – 250R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111110	((350R – 252R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N0 6-0 = 1111111	((350R – 254R) / 450R) * (VREG1 - VGS) + VGS

Table 7. 7 Voltage Calculation Formula for VinP/N 4

Reference Voltage	Macro Adjustment Value	VinP/N5 Formula
VinP/N5	PKP/N3 4-0 = 00000	(193R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00001	((193R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00010	((193R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00011	((193R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00100	((193R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00101	((193R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00110	((193R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00111	((193R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01000	((193R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01001	((193R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01010	((193R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01011	((193R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01100	((193R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01101	((193R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01110	((193R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01111	((193R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10000	((193R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10001	((193R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10010	((193R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10011	((193R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10100	((193R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10101	((193R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10110	((193R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10111	((193R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11000	((193R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11001	((193R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11010	((193R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11011	((193R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11100	((193R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11101	((193R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11110	((193R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11111	((193R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 7. 8 Voltage Calculation Formula for VinP/N 5

Reference Voltage	Macro Adjustment Value	VinP/N6 Formula
VinP/N6	PKP/N4 4-0 = 00000	(158R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00001	((158R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00010	((158R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00011	((158R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00100	((158R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00101	((158R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 00110	((158R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

	PKP/N4 4-0 = 00111	((158R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01000	((158R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01001	((158R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01010	((158R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01011	((158R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01100	((158R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01101	((158R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01110	((158R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 01111	((158R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10000	((158R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10001	((158R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10010	((158R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10011	((158R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10100	((158R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10101	((158R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10110	((158R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 10111	((158R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11000	((158R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11001	((158R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11010	((158R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11011	((158R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11100	((158R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11101	((158R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11110	((158R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N4 4-0 = 11111	((158R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 7. 9 Voltage Calculation Formula for VinP/N 6

Reference Voltage	Macro Adjustment Value	VinP/N7 Formula
VinP/N7	PKP/N6 4-0 = 00000	(123R / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00001	((123R - 3R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00010	((123R - 6R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00011	((123R - 9R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00100	((123R - 12R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00101	((123R - 15R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00110	((123R - 18R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00111	((123R - 21R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01000	((123R - 24R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01001	((123R - 27R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01010	((123R - 30R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01011	((123R - 33R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01100	((123R - 36R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01101	((123R - 39R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01110	((123R - 42R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01111	((123R - 45R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10000	((123R - 48R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10001	((123R - 51R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10010	((123R - 54R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10011	((123R - 57R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10100	((123R - 60R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10101	((123R - 63R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10110	((123R - 66R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10111	((123R - 69R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11000	((123R - 72R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11001	((123R - 75R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11010	((123R - 78R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11011	((123R - 81R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11100	((123R - 84R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11101	((123R - 87R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11110	((123R - 90R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11111	((123R - 93R) / 223R) * (VinP/N4 - VinP/N8) + VinP/N8

Table 7. 10 Voltage Calculation Formula for VinP/N 7

Reference Voltage	Macro Adjustment Value	VinP/N8 Formula
VinP/N8	PRP/N1 6-0 = 0000000	(354R / 450R) (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000001	((354R - 2R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000010	((354R - 4R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000011	((354R – 6R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000100	((354R – 8R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000101	((354R – 10R) / 450R) * (VREG1 - VGS) + VGS

	PRP/N1 6-0 = 0000110	((354R – 12R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0000111	((354R - 14R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001000	((354R – 16R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001001	((354R – 18R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001010	((354R – 20R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001011	((354R – 22R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001100	((354R – 24R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001101	((354R – 26R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001110	((354R – 28R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0001111	((354R – 30R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010000	((354R – 32R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010001	((354R - 34R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010010	((354R – 36R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010011	((354R – 38R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010100	((354R – 40R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010101	((354R – 42R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010110	((354R – 44R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0010111	((354R – 46R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011000	((354R – 48R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011001	((354R – 50R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011010	((354R – 52R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011011	((354R - 54R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011100	((354R – 56R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011101	((354R – 58R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011110	((354R – 60R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0011111	((354R – 62R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100000	((354R - 64R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100001	((354R – 66R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100010	((354R – 68R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100011	((354R – 70R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100100	((354R – 72R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100101	((354R – 74R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100110	((354R – 76R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0100111	((354R – 78R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101000	((354R – 80R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101001	((354R – 82R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101010	((354R - 84R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101011	((354R – 86R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101100	((354R – 88R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101101	((354R – 90R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101110	((354R – 92R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0101111	((354R – 94R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110000	((354R – 96R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110001	((354R – 98R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110010	((354R – 100R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110011	((354R – 102R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110100	((354R – 104R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110101	((354R – 106R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110110	((354R – 108R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0110111	((354R – 110R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111000	((354R – 112R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111001	((354R – 114R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111010	((354R – 116R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111011	((354R – 118R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111100	((354R – 120R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111101	((354R – 122R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111110	((354R - 124R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 0111111	((354R – 126R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000000	((354R – 128R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000001	((354R – 130R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000010	((354R - 132R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000011	((354R – 134R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000100	((354R – 136R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000101	((354R – 138R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000110	((354R – 140R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1000111	((354R – 142R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001000	((354R – 144R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001001	((354R – 146R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001010	((354R – 148R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001011	((354R – 150R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001100	((354R - 152R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001101	((354R – 154R) / 450R) * (VREG1 - VGS) + VGS

	PRP/N1 6-0 = 1001110	((354R – 156R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1001111	((354R – 158R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010000	((354R – 160R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010001	((354R – 162R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010010	((354R – 164R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010011	((354R – 166R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010100	((354R – 168R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010101	((354R – 170R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010110	((354R – 172R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1010111	((354R - 174R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011000	((354R – 176R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011001	((354R - 178R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011010	((354R – 180R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011011	((354R – 182R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011100	((354R - 184R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011101	((354R – 186R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011110	((354R - 188R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1011111	((354R – 190R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100000	((354R – 192R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100001	((354R - 194R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100010	((354R – 196R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100011	((354R - 198R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100100	((354R – 200R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100101	((354R – 202R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100110	((354R - 204R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1100111	((354R – 206R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101000	((354R - 208R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101001	((354R – 210R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101010	((354R – 212R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101011	((354R - 214R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101100	((354R – 216R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101101	((354R - 218R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101110	((354R – 220R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1101111	((354R - 222R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110000	((354R - 224R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110001	((354R – 226R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110010	((354R - 228R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110011	((354R – 230R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110100	((354R – 232R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110101	((354R - 234R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110110	((354R – 236R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1110111	((354R - 238R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111000	((354R – 240R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111001	((354R – 242R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111010	((354R - 244R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111011	((354R – 246R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111100	((354R - 248R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111101	((354R – 250R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111110	((354R – 252R) / 450R) * (VREG1 - VGS) + VGS
	PRP/N1 6-0 = 1111111	((354R - 254R) / 450R) * (VREG1 - VGS) + VGS

Table 7. 11 Voltage Calculation Formula for VinP/N 8

Reference Voltage	Macro Adjustment Value	VinP/N9 Formula
VinP/N9	PKP/N7 4-0 = 00000	(31R / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00001	((31R - 1R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00010	((31R - 2R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00011	((31R - 3R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00100	((31R - 4R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00101	((31R - 5R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00110	((31R - 6R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 00111	((31R - 7R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01000	((31R - 8R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01001	((31R - 9R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01010	((31R - 10R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01011	((31R - 11R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01100	((31R - 12R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01101	((31R - 13R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01110	((31R - 14R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 01111	((31R - 15R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10000	((31R - 16R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10001	((31R - 17R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10010	((31R - 18R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10011	((31R - 19R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10100	((31R - 20R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10101	((31R - 21R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10110	((31R - 22R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 10111	((31R - 23R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11000	((31R - 24R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11001	((31R - 25R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11010	((31R - 26R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11011	((31R - 27R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11100	((31R - 28R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11101	((31R - 29R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11110	((31R - 30R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10
	PKP/N7 4-0 = 11111	((31R - 31R) / 32R) * (VinP/N8 - VinP/N10) + VinP/N10

Table 7. 12 Voltage Calculation Formula for VinP/N 9

Reference Voltage	Macro Adjustment Value	VinP/N10 Formula
VinP/N10	VRP/N3 5-0 = 000000	(230R / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000001	((230R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000010	((230R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000011	((230R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000100	((230R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000101	((230R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000110	((230R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 000111	((230R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001000	((230R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001001	((230R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001010	((230R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001011	((230R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001100	((230R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001101	((230R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001110	((230R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 001111	((230R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010000	((230R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010001	((230R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010010	((230R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010011	((230R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010100	((230R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010101	((230R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010110	((230R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 010111	((230R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011000	((230R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011001	((230R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011010	((230R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011011	((230R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011100	((230R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011101	((230R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011110	((230R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 011111	((230R - 124R) / 450R) * (VREG1 - VGS) + VGS

	VRP/N3 5-0 = 100000	((230R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100001	((230R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100010	((230R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100011	((230R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100100	((230R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100101	((230R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100110	((230R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 100111	((230R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101000	((230R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101001	((230R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101010	((230R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101011	((230R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101100	((230R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101101	((230R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101110	((230R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 101111	((230R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110000	((230R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110001	((230R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110010	((230R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110011	((230R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110100	((230R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110101	((230R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110110	((230R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 110111	((230R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111000	((230R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111001	((230R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111010	((230R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111011	((230R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111100	((230R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111101	((230R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111110	((230R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N3 5-0 = 111111	((230R - 190R) / 450R) * (VREG1 - VGS) + VGS

Table 7. 13 Voltage Calculation Formula for VinP/N 10

Reference Voltage	Macro Adjustment Value	VinP/N11 Formula
VinP/N11	VRP/N4 5-0 = 000000	(210R / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000001	((210R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000010	((210R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000011	((210R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000100	((210R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000101	((210R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000110	((210R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 000111	((210R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001000	((210R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001001	((210R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001010	((210R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001011	((210R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001100	((210R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001101	((210R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001110	((210R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 001111	((210R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010000	((210R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010001	((210R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010010	((210R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010011	((210R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010100	((210R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010101	((210R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010110	((210R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 010111	((210R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011000	((210R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011001	((210R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011010	((210R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011011	((210R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011100	((210R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011101	((210R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011110	((210R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 011111	((210R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100000	((210R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100001	((210R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100010	((210R - 132R) / 450R) * (VREG1 - VGS) + VGS

	VRP/N4 5-0 = 100011	((210R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100100	((210R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100101	((210R - 138R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100110	((210R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 100111	((210R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101000	((210R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101001	((210R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101010	((210R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101011	((210R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101100	((210R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101101	((210R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101110	((210R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 101111	((210R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110000	((210R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110001	((210R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110010	((210R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110011	((210R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110100	((210R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110101	((210R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110110	((210R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 110111	((210R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111000	((210R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111001	((210R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111010	((210R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111011	((210R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111100	((210R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111101	((210R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111110	((210R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N4 5-0 = 111111	((210R - 190R) / 450R) * (VREG1 - VGS) + VGS

Table 7. 14 Voltage Calculation Formula for VinP/N 11

Reference Voltage	Macro Adjustment Value	VinP/N12 Formula
VinP/N12	VRP/N5 5-0 = 000000	(210R / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000001	((208R - 4R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000010	((208R - 8R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000011	((208R - 12R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000100	((208R - 16R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000101	((208R - 20R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000110	((208R - 24R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 000111	((208R - 28R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001000	((208R - 32R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001001	((208R - 36R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001010	((208R - 40R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001011	((208R - 44R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001100	((208R - 48R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001101	((208R - 52R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001110	((208R - 56R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 001111	((208R - 60R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010000	((208R - 64R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010001	((208R - 68R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010010	((208R - 72R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010011	((208R - 76R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010100	((208R - 80R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010101	((208R - 84R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010110	((208R - 88R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 010111	((208R - 92R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011000	((208R - 96R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011001	((208R - 100R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011010	((208R - 104R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011011	((208R - 108R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011100	((208R - 112R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011101	((208R - 116R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011110	((208R - 120R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 011111	((208R - 124R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100000	((208R - 128R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100001	((208R - 130R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100010	((208R - 132R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100011	((208R - 134R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100100	((208R - 136R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100101	((208R - 138R) / 450R) * (VREG1 - VGS) + VGS

	VRP/N5 5-0 = 100110	((208R - 140R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 100111	((208R - 142R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101000	((208R - 144R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101001	((208R - 146R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101010	((208R - 148R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101011	((208R - 150R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101100	((208R - 152R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101101	((208R - 154R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101110	((208R - 156R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 101111	((208R - 158R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110000	((208R - 160R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110001	((208R - 162R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110010	((208R - 164R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110011	((208R - 166R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110100	((208R - 168R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110101	((208R - 170R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110110	((208R - 172R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 110111	((208R - 174R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111000	((208R - 176R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111001	((208R - 178R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111010	((208R - 180R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111011	((208R - 182R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111100	((208R - 184R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111101	((208R - 186R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111110	((208R - 188R) / 450R) * (VREG1 - VGS) + VGS
	VRP/N5 5-0 = 111111	VGS

Table 7. 15 Voltage Calculation Formula for VinP/N 12

Grayscale Voltage	Formula
V0	VinP0
V1	VinP1
V2	VinP2
V3	VinP3
V4	VinP4+ (VinP3 - VinP4)*CT1
V5	VinP4+ (VinP3 - VinP4)*CT2
V6	VinP4+ (VinP3 - VinP4)*CT3
V7	VinP4+ (VinP3 - VinP4)*CT4
V8	VinP4
V9	VinP5+(VinP4- VinP5)*(22R/24R)
V10	VinP5+(VinP4- VinP5)*(20R/24R)
V11	VinP5+(VinP4- VinP5)*(18R/24R)
V12	VinP5+(VinP4- VinP5)*(16R/24R)
V13	VinP5+(VinP4- VinP5)*(14R/24R)
V14	VinP5+(VinP4- VinP5)*(12R/24R)
V15	VinP5+(VinP4- VinP5)*(10R/24R)
V16	VinP5+(VinP4- VinP5)*(8R/24R)
V17	VinP5+(VinP4- VinP5)*(6R/24R)
V18	VinP5+(VinP4- VinP5)*(4R/24R)
V19	VinP5+(VinP4- VinP5)*(2R/24R)
V20	VinP5
V21	VinP6+(VinP5- VinP6)*(22R/24R)
V22	VinP6+(VinP5- VinP6)*(20R/24R)
V23	VinP6+(VinP5- VinP6)*(18R/24R)
V24	VinP6+(VinP5- VinP6)*(16R/24R)
V25	VinP6+(VinP5- VinP6)*(14R/24R)
V26	VinP6+(VinP5- VinP6)*(12R/24R)
V27	VinP6+(VinP5- VinP6)*(10R/24R)
V28	VinP6+(VinP5- VinP6)*(8R/24R)
V29	VinP6+(VinP5- VinP6)*(6R/24R)
V30	VinP6+(VinP5- VinP6)*(4R/24R)
V31	VinP6+(VinP5- VinP6)*(2R/24R)

Grayscale Voltage	Formula
V32	VinP6
V33	VinP7+(VinP6- VinP7)*(20R/22R)
V34	VinP7+(VinP6- VinP7)*(18R/22R)
V35	VinP7+(VinP6- VinP7)*(16R/22R)
V36	VinP7+(VinP6- VinP7)*(14R/22R)
V37	VinP7+(VinP6- VinP7)*(12R/22R)
V38	VinP7+(VinP6- VinP7)*(10R/22R)
V39	VinP7+(VinP6- VinP7)*(8R/22R)
V40	VinP7+(VinP6- VinP7)*(6R/22R)
V41	VinP7+(VinP6- VinP7)*(4R/22R)
V42	VinP7+(VinP6- VinP7)*(2R/22R)
V43	VinP7
V44	VinP8+(VinP7- VinP8)*(22R/24R)
V45	VinP8+(VinP7- VinP8)*(20R/24R)
V46	VinP8+(VinP7- VinP8)*(18R/24R)
V47	VinP8+(VinP7- VinP8)*(16R/24R)
V48	VinP8+(VinP7- VinP8)*(14R/24R)
V49	VinP8+(VinP7- VinP8)*(12R/24R)
V50	VinP8+(VinP7- VinP8)*(10R/24R)
V51	VinP8+(VinP7- VinP8)*(8R/24R)
V52	VinP8+(VinP7- VinP8)*(6R/24R)
V53	VinP8+(VinP7- VinP8)*(4R/24R)
V54	VinP8+(VinP7- VinP8)*(2R/24R)
V55	VinP8
V56	VinP9+ (VinP8 – VinP9)*CB1
V57	VinP9+ (VinP8 – VinP9)*CB2
V58	VinP9+ (VinP8 – VinP9)*CB3
V59	VinP9+ (VinP8 – VinP9)*CB4
V60	VinP9
V61	VinP10
V62	VinP11
V63	VinP12

Table 7. 16 Voltage Calculation Formula of 64-Grayscale Voltage (Positive Polarity)

CGMP0[1:0]	“00”	“01”	“10”	“11”
CT1	4/5	2/3	3/5	31/41
CT2	3/5	1/2	9/20	22/41
CT3	2/5	1/3	3/10	14/41
CT4	1/5	1/6	3/20	6/41

CGMP1[1:0]	“00”	“01”	“10”	“11”
CB1	4/5	5/6	17/20	13/16
CB2	3/5	2/3	7/10	5/8
CB3	2/5	1/2	11/20	41/96
CB4	1/5	1/3	2/5	7/32

Table 7. 17 Voltage Calculation Formula of Grayscale Voltage V2~V7 and V56~V61

Grayscale Voltage	Formula
V0	VinN0
V1	VinN1
V2	VinN2
V3	VinN3
V4	VinN4+ (VinN3 - VinN4)*CT1
V5	VinN4+ (VinN3 - VinN4)*CT2
V6	VinN4+ (VinN3 - VinN4)*CT3
V7	VinN4+ (VinN3 - VinN4)*CT4
V8	VinN4
V9	VinN5+(VinN4- VinN5)*(22R/24R)
V10	VinN5+(VinN4- VinN5)*(20R/24R)
V11	VinN5+(VinN4- VinN5)*(18R/24R)
V12	VinN5+(VinN4- VinN5)*(16R/24R)
V13	VinN5+(VinN4- VinN5)*(14R/24R)
V14	VinN5+(VinN4- VinN5)*(12R/24R)
V15	VinN5+(VinN4- VinN5)*(10R/24R)
V16	VinN5+(VinN4- VinN5)*(8R/24R)
V17	VinN5+(VinN4- VinN5)*(6R/24R)
V18	VinN5+(VinN4- VinN5)*(4R/24R)
V19	VinN5+(VinN4- VinN5)*(2R/24R)
V20	VinN5
V21	VinN6+(VinN5- VinN6)*(20R/22R)
V22	VinN6+(VinN5- VinN6)*(18R/22R)
V23	VinN6+(VinN5- VinN6)*(16R/22R)
V24	VinN6+(VinN5- VinN6)*(14R/22R)
V25	VinN6+(VinN5- VinN6)*(12R/22R)
V26	VinN6+(VinN5- VinN6)*(10R/22R)
V27	VinN6+(VinN5- VinN6)*(8R/22R)
V28	VinN6+(VinN5- VinN6)*(6R/22R)
V29	VinN6+(VinN5- VinN6)*(4R/22R)
V30	VinN6+(VinN5- VinN6)*(2R/22R)
V31	VinN6

Grayscale Voltage	Formula
V32	VinN7+(VinN6- VinN7)*(22R/24R)
V33	VinN7+(VinN6- VinN7)*(20R/24R)
V34	VinN7+(VinN6- VinN7)*(18R/24R)
V35	VinN7+(VinN6- VinN7)*(16R/24R)
V36	VinN7+(VinN6- VinN7)*(14R/24R)
V37	VinN7+(VinN6- VinN7)*(12R/24R)
V38	VinN7+(VinN6- VinN7)*(10R/24R)
V39	VinN7+(VinN6- VinN7)*(8R/24R)
V40	VinN7+(VinN6- VinN7)*(6R/24R)
V41	VinN7+(VinN6- VinN7)*(4R/24R)
V42	VinN7+(VinN6- VinN7)*(2R/24R)
V43	VinN7
V44	VinN8+(VinN7- VinN8)*(22R/24R)
V45	VinN8+(VinN7- VinN8)*(20R/24R)
V46	VinN8+(VinN7- VinN8)*(18R/24R)
V47	VinN8+(VinN7- VinN8)*(16R/24R)
V48	VinN8+(VinN7- VinN8)*(14R/24R)
V49	VinN8+(VinN7- VinN8)*(12R/24R)
V50	VinN8+(VinN7- VinN8)*(10R/24R)
V51	VinN8+(VinN7- VinN8)*(8R/24R)
V52	VinN8+(VinN7- VinN8)*(6R/24R)
V53	VinN8+(VinN7- VinN8)*(4R/24R)
V54	VinN8+(VinN7- VinN8)*(2R/24R)
V55	VinN8
V56	VinN9+ (VinN8 – VinN9)*CB1
V57	VinN9+ (VinN8 – VinN9)*CB2
V58	VinN9+ (VinN8 – VinN9)*CB3
V59	VinN9+ (VinN8 – VinN9)*CB4
V60	VinN9
V61	VinN10
V62	VinN11
V63	VinN12

Table 7. 18 Voltage Calculation Formula of 64-Grayscale Voltage (Negative Polarity)

CGMN0[1:0]	“00”	“01”	“10”	“11”
CT1	4/5	2/3	3/5	31/41
CT2	3/5	1/2	9/20	22/41
CT3	2/5	1/3	3/10	14/41
CT4	1/5	1/6	3/20	6/41

CGMN1[1:0]	“00”	“01”	“10”	“11”
CB1	4/5	5/6	17/20	13/16
CB2	3/5	2/3	7/10	5/8
CB3	2/5	1/2	11/20	41/96
CB4	1/5	1/3	2/5	7/32

Table 7. 19 Voltage Calculation Formula of Grayscale Voltage V2~V7 and V56~V61

Relationship between GRAM Data and Output Level (INVON = 0 “Normally White Panel”, GRAM data=0)

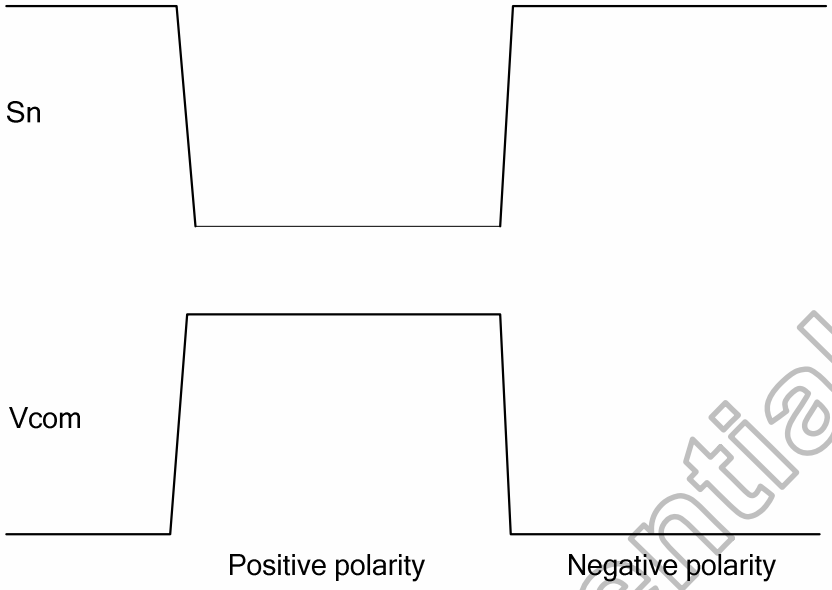
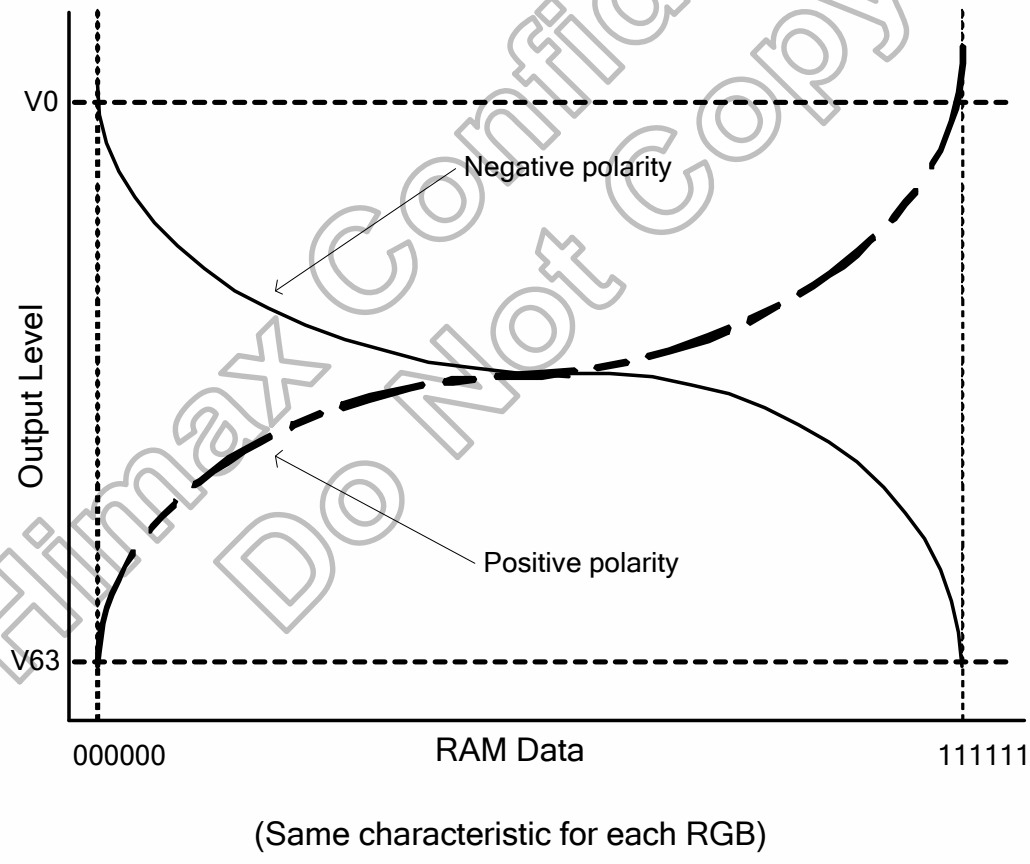


Figure 7. 8 Relationship between Source Output and Vcom



(Same characteristic for each RGB)

Figure 7. 9 Relationship between GRAM Data and Output Level (Normal White Panel REV_Panel=“0”)

7.2.2 Gray voltage generator for digital gamma correction

The HX8357-A digital gamma correction can reach the independent GAMMA curve of RGB. HX8357-A utilizes DGC_LUT (Digital Gamma Correction Look Up Table) to change input data from 6-bit into 8-bit and sends 8-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

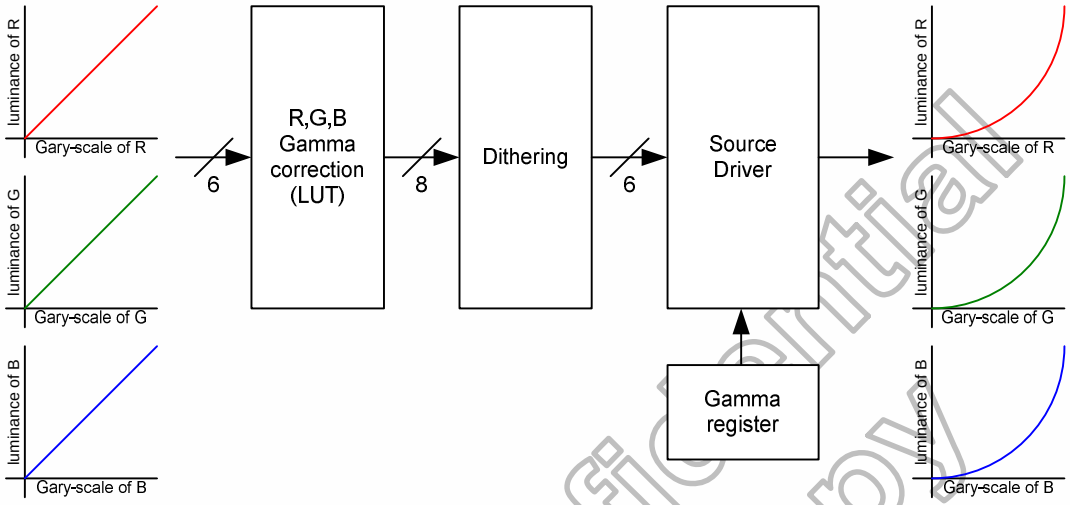


Figure 7. 10 Block Diagram of Digital Gamma Correction

The HX8357-A builds one 192-bytes DGC_LUT (Digital Gamma Correction Look Up Table) to transfer every display data of Dithering circuit input and setting by DGLUT register.

DGC_LUT Parameter byte	Command set		R input (6 bit)	R output (8bit)
	Page	Address		
1	01h	R01h	000000	R_{007} $R_{006}R_{005}$ $R_{004}R_{003}R_{002}R_{001}R_{000}$
2	01h	R02h	000001	$R_{017}R_{016}R_{015}R_{014}R_{013}R_{012}R_{011}R_{010}$
3	01h	R03h	000010	$R_{027}R_{026}R_{025}R_{024}R_{023}R_{022}R_{021}R_{020}$
4	01h	R04h	000011	$R_{037}R_{036}R_{035}R_{034}R_{033}R_{032}R_{031}R_{030}$
5	01h	R05h	000100	$R_{047}R_{046}R_{045}R_{044}R_{043}R_{042}R_{041}R_{040}$
6	01h	R06h	000101	$R_{057}R_{056}R_{055}R_{054}R_{053}R_{052}R_{051}R_{050}$
7	01h	R07h	000110	$R_{067}R_{066}R_{065}R_{064}R_{063}R_{062}R_{061}R_{060}$
8	01h	R08h	000111	$R_{077}R_{076}R_{075}R_{074}R_{073}R_{072}R_{071}R_{070}$
9	01h	R09h	001000	$R_{087}R_{086}R_{085}R_{084}R_{083}R_{082}R_{081}R_{080}$
10	01h	R0Ah	001001	$R_{097}R_{096}R_{095}R_{094}R_{093}R_{092}R_{091}R_{090}$
11	01h	R0Bh	001010	$R_{107}R_{106}R_{105}R_{104}R_{103}R_{102}R_{101}R_{100}$
12	01h	R0Ch	001011	$R_{117}R_{116}R_{115}R_{114}R_{113}R_{112}R_{111}R_{110}$
13	01h	R0Dh	001100	$R_{127}R_{126}R_{125}R_{124}R_{123}R_{122}R_{121}R_{120}$
14	01h	R0Eh	001101	$R_{137}R_{136}R_{135}R_{134}R_{133}R_{132}R_{131}R_{130}$
15	01h	R0Fh	001110	$R_{147}R_{146}R_{145}R_{144}R_{143}R_{142}R_{141}R_{140}$
16	01h	R10h	001111	$R_{157}R_{156}R_{155}R_{154}R_{153}R_{152}R_{151}R_{150}$
17	01h	R11h	010000	R_{167} $R_{166}R_{165}$ $R_{164}R_{163}R_{162}R_{161}R_{160}$
18	01h	R12h	010001	$R_{177}R_{176}R_{175}R_{174}R_{173}R_{172}R_{171}R_{170}$
19	01h	R13h	010010	$R_{187}R_{186}R_{185}R_{184}R_{183}R_{182}R_{181}R_{180}$
20	01h	R14h	010011	$R_{197}R_{196}R_{195}R_{194}R_{193}R_{192}R_{191}R_{190}$
21	01h	R15h	010100	$R_{207}R_{206}R_{205}R_{204}R_{203}R_{202}R_{201}R_{200}$
22	01h	R16h	010101	$R_{217}R_{216}R_{215}R_{214}R_{213}R_{212}R_{211}R_{210}$
23	01h	R17h	010110	$R_{227}R_{226}R_{225}R_{224}R_{223}R_{222}R_{221}R_{220}$
24	01h	R18h	010111	$R_{237}R_{236}R_{235}R_{234}R_{233}R_{232}R_{231}R_{230}$
25	01h	R19h	011000	$R_{247}R_{246}R_{245}R_{244}R_{243}R_{242}R_{241}R_{240}$
26	01h	R1Ah	011001	$R_{257}R_{256}R_{255}R_{254}R_{253}R_{252}R_{251}R_{250}$
27	01h	R1Bh	011010	$R_{267}R_{266}R_{265}R_{264}R_{263}R_{262}R_{261}R_{260}$
28	01h	R1Ch	011011	$R_{277}R_{276}R_{275}R_{274}R_{273}R_{272}R_{271}R_{270}$
29	01h	R1Dh	011100	$R_{287}R_{286}R_{285}R_{284}R_{283}R_{282}R_{281}R_{280}$
30	01h	R1Eh	011101	$R_{297}R_{296}R_{295}R_{294}R_{293}R_{292}R_{291}R_{290}$
31	01h	R1Fh	011110	$R_{307}R_{306}R_{305}R_{304}R_{303}R_{302}R_{301}R_{300}$
32	01h	R20h	011111	$R_{317}R_{316}R_{315}R_{314}R_{313}R_{312}R_{311}R_{310}$

Table 7. 20 DGLUT for Red Color (1)

DGC_LUT Parameter byte	Command		R input (6 bit)	R output (8bit)
	Page	Address		
33	01h	R21h	100000	R327 R326R325 R324R323R322R321R320
34	01h	R22h	100001	R337R336R335R334R333R332R331R330
35	01h	R23h	100010	R347R346R345R344R343R342R341R340
36	01h	R24h	100011	R357R356R355R354R353R352R351R350
37	01h	R25h	100100	R367R366R365R364R363R362R361R360
38	01h	R26h	100101	R377R376R375R374R373R372R371R370
39	01h	R27h	100110	R387R386R385R384R383R382R381R380
40	01h	R28h	100111	R397R396R395R394R393R392R391R390
41	01h	R29h	101000	R407R406R405R404R403R402R401R400
42	01h	R2Ah	101001	R417R416R415R414R413R412R411R410
43	01h	R2Bh	101010	R427R426R425R424R423R422R421R420
44	01h	R2Ch	101011	R437R436R435R434R433R432R431R430
45	01h	R2Dh	101100	R447R446R445R444R443R442R441R440
46	01h	R2Eh	101101	R457R456R455R454R453R452R451R450
47	01h	R2Fh	101110	R467R466R465R464R463R462R461R460
48	01h	R30h	101111	R477R476R475R474R473R472R471R470
49	01h	R31h	110000	R487 R486R485 R484R483R482R481R480
50	01h	R32h	110001	R497R496R495R494R493R492R491R490
51	01h	R33h	110010	R507R506R505R504R503R502R501R500
52	01h	R34h	110011	R517R516R515R514R513R512R511R510
53	01h	R35h	110100	R527R526R525R524R523R522R521R520
54	01h	R36h	110101	R537R536R535R534R533R532R531R530
55	01h	R37h	110110	R547R546R545R544R543R542R541R540
56	01h	R38h	110111	R557R556R555R554R553R552R551R550
57	01h	R39h	111000	R567R566R565R564R563R562R561R560
58	01h	R3Ah	111001	R577R576R575R574R573R572R571R570
59	01h	R3Bh	111010	R587R586R585R584R583R582R581R580
60	01h	R3Ch	111011	R597R596R595R594R593R592R591R590
61	01h	R3Dh	111100	R607R606R605R604R603R602R601R600
62	01h	R3Eh	111101	R617R616R615R614R613R612R611R610
63	01h	R3Fh	111110	R627R626R625R624R623R622R621R620
64	01h	R40h	111111	R637R636R635R634R633R632R631R630

Table 7. 21 DGLUT for Red Color (2)

DGC_LUT Parameter byte	Command		G input (6 bit)	G output (8bit)
	Page	Address		
65	01h	R41h	000000	G_{007} $G_{006}G_{005}$ $G_{004}G_{003}G_{002}G_{001}G_{000}$
66	01h	R42h	000001	$G_{017}G_{016}G_{015}G_{014}G_{013}G_{012}G_{011}G_{010}$
67	01h	R43h	000010	$G_{027}G_{026}G_{025}G_{024}G_{023}G_{022}G_{021}G_{020}$
68	01h	R44h	000011	$G_{037}G_{036}G_{035}G_{034}G_{033}G_{032}G_{031}G_{030}$
69	01h	R45h	000100	$G_{047}G_{046}G_{045}G_{044}G_{043}G_{042}G_{041}G_{040}$
70	01h	R46h	000101	$G_{057}G_{056}G_{055}G_{054}G_{053}G_{052}G_{051}G_{050}$
71	01h	R47h	000110	$G_{067}G_{066}G_{065}G_{064}G_{063}G_{062}G_{061}G_{060}$
72	01h	R48h	000111	$G_{077}G_{076}G_{075}G_{074}G_{073}G_{072}G_{071}G_{070}$
73	01h	R49h	001000	$G_{087}G_{086}G_{085}G_{084}G_{083}G_{082}G_{081}G_{080}$
74	01h	R4Ah	001001	$G_{097}G_{096}G_{095}G_{094}G_{093}G_{092}G_{091}G_{090}$
75	01h	R4Bh	001010	$G_{107}G_{106}G_{105}G_{104}G_{103}G_{102}G_{101}G_{100}$
76	01h	R4Ch	001011	$G_{117}G_{116}G_{115}G_{114}G_{113}G_{112}G_{111}G_{110}$
77	01h	R4Dh	001100	$G_{127}G_{126}G_{125}G_{124}G_{123}G_{122}G_{121}G_{120}$
78	01h	R4Eh	001101	$G_{137}G_{136}G_{135}G_{134}G_{133}G_{132}G_{131}G_{130}$
79	01h	R4Fh	001110	$G_{147}G_{146}G_{145}G_{144}G_{143}G_{142}G_{141}G_{140}$
80	01h	R50h	001111	$G_{157}G_{156}G_{155}G_{154}G_{153}G_{152}G_{151}G_{150}$
81	01h	R51h	010000	G_{167} $G_{166}G_{165}$ $G_{164}G_{163}G_{162}G_{161}G_{160}$
82	01h	R52h	010001	$G_{177}G_{176}G_{175}G_{174}G_{173}G_{172}G_{171}G_{170}$
83	01h	R53h	010010	$G_{187}G_{186}G_{185}G_{184}G_{183}G_{182}G_{181}G_{180}$
84	01h	R54h	010011	$G_{197}G_{196}G_{195}G_{194}G_{193}G_{192}G_{191}G_{190}$
85	01h	R55h	010100	$G_{207}G_{206}G_{205}G_{204}G_{203}G_{202}G_{201}G_{200}$
86	01h	R56h	010101	$G_{217}G_{216}G_{215}G_{214}G_{213}G_{212}G_{211}G_{210}$
87	01h	R57h	010110	$G_{227}G_{226}G_{225}G_{224}G_{223}G_{222}G_{221}G_{220}$
88	01h	R58h	010111	$G_{237}G_{236}G_{235}G_{234}G_{233}G_{232}G_{231}G_{230}$
89	01h	R59h	011000	$G_{247}G_{246}G_{245}G_{244}G_{243}G_{242}G_{241}G_{240}$
90	01h	R5Ah	011001	$G_{257}G_{256}G_{255}G_{254}G_{253}G_{252}G_{251}G_{250}$
91	01h	R5Bh	011010	$G_{267}G_{266}G_{265}G_{264}G_{263}G_{262}G_{261}G_{260}$
92	01h	R5Ch	011011	$G_{277}G_{276}G_{275}G_{274}G_{273}G_{272}G_{271}G_{270}$
93	01h	R5Dh	011100	$G_{287}G_{286}G_{285}G_{284}G_{283}G_{282}G_{281}G_{280}$
94	01h	R5Eh	011101	$G_{297}G_{296}G_{295}G_{294}G_{293}G_{292}G_{291}G_{290}$
95	01h	R5Fh	011110	$G_{307}G_{306}G_{305}G_{304}G_{303}G_{302}G_{301}G_{300}$
96	01h	R60h	011111	$G_{317}G_{316}G_{315}G_{314}G_{313}G_{312}G_{311}G_{310}$

Table 7. 22 DGLUT for Green Color (1)

DGC_LUT Parameter byte	Command		G input (6 bit)	G output (8bit)
	Page	Address		
97	01h	R61h	100000	G_{327} $G_{326}G_{325}$ $G_{324}G_{323}G_{322}G_{321}G_{320}$
98	01h	R62h	100001	$G_{337}G_{336}G_{335}G_{334}G_{333}G_{332}G_{331}G_{330}$
99	01h	R63h	100010	$G_{347}G_{346}G_{345}G_{344}G_{343}G_{342}G_{341}G_{340}$
100	01h	R64h	100011	$G_{357}G_{356}G_{355}G_{354}G_{353}G_{352}G_{351}G_{350}$
101	01h	R65h	100100	$G_{367}G_{366}G_{365}G_{364}G_{363}G_{362}G_{361}G_{360}$
102	01h	R66h	100101	$G_{377}G_{376}G_{375}G_{374}G_{373}G_{372}G_{371}G_{370}$
103	01h	R67h	100110	$G_{387}G_{386}G_{385}G_{384}G_{383}G_{382}G_{381}G_{380}$
104	01h	R68h	100111	$G_{397}G_{396}G_{395}G_{394}G_{393}G_{392}G_{391}G_{390}$
105	01h	R69h	101000	$G_{407}G_{406}G_{405}G_{404}G_{403}G_{402}G_{401}G_{400}$
106	01h	R6Ah	101001	$G_{417}G_{416}G_{415}G_{414}G_{413}G_{412}G_{411}G_{410}$
107	01h	R6Bh	101010	$G_{427}G_{426}G_{425}G_{424}G_{423}G_{422}G_{421}G_{420}$
108	01h	R6Ch	101011	$G_{437}G_{436}G_{435}G_{434}G_{433}G_{432}G_{431}G_{430}$
109	01h	R6Dh	101100	$G_{447}G_{446}G_{445}G_{444}G_{443}G_{442}G_{441}G_{440}$
110	01h	R6Eh	101101	$G_{457}G_{456}G_{455}G_{454}G_{453}G_{452}G_{451}G_{450}$
111	01h	R6Fh	101110	$G_{467}G_{466}G_{465}G_{464}G_{463}G_{462}G_{461}G_{460}$
112	01h	R70h	101111	$G_{477}G_{476}G_{475}G_{474}G_{473}G_{472}G_{471}G_{470}$
113	01h	R71h	110000	G_{487} $G_{486}G_{485}$ $G_{484}G_{483}G_{482}G_{481}G_{480}$
114	01h	R72h	110001	$G_{497}G_{496}G_{495}G_{494}G_{493}G_{492}G_{491}G_{490}$
115	01h	R73h	110010	$G_{507}G_{506}G_{505}G_{504}G_{503}G_{502}G_{501}G_{500}$
116	01h	R74h	110011	$G_{517}G_{516}G_{515}G_{514}G_{513}G_{512}G_{511}G_{510}$
117	01h	R75h	110100	$G_{527}G_{526}G_{525}G_{524}G_{523}G_{522}G_{521}G_{520}$
118	01h	R76h	110101	$G_{537}G_{536}G_{535}G_{534}G_{533}G_{532}G_{531}G_{530}$
119	01h	R77h	110110	$G_{547}G_{546}G_{545}G_{544}G_{543}G_{542}G_{541}G_{540}$
120	01h	R78h	110111	$G_{557}G_{556}G_{555}G_{554}G_{553}G_{552}G_{551}G_{550}$
121	01h	R79h	111000	$G_{567}G_{566}G_{565}G_{564}G_{563}G_{562}G_{561}G_{560}$
122	01h	R7Ah	111001	$G_{577}G_{576}G_{575}G_{574}G_{573}G_{572}G_{571}G_{570}$
123	01h	R7Bh	111010	$G_{587}G_{586}G_{585}G_{584}G_{583}G_{582}G_{581}G_{580}$
124	01h	R7Ch	111011	$G_{597}G_{596}G_{595}G_{594}G_{593}G_{592}G_{591}G_{590}$
125	01h	R7Dh	111100	$G_{607}G_{606}G_{605}G_{604}G_{603}G_{602}G_{601}G_{600}$
126	01h	R7Eh	111101	$G_{617}G_{616}G_{615}G_{614}G_{613}G_{612}G_{611}G_{610}$
127	01h	R7Fh	111110	$G_{627}G_{626}G_{625}G_{624}G_{623}G_{622}G_{621}G_{620}$
128	01h	R80h	111111	$G_{637}G_{636}G_{635}G_{634}G_{633}G_{632}G_{631}G_{630}$

Table 7. 23 DGLUT for Green Color (2)

DGC_LUT Parameter byte	Command		B input (6 bit)	B output (8bit)
	Page	Address		
129	01h	R81h	000000	B_{007} $B_{006}B_{005}$ $B_{004}B_{003}B_{002}B_{001}B_{000}$
130	01h	R82h	000001	$B_{017}B_{016}B_{015}B_{014}B_{013}B_{012}B_{011}B_{010}$
131	01h	R83h	000010	$B_{027}B_{026}B_{025}B_{024}B_{023}B_{022}B_{021}B_{020}$
132	01h	R84h	000011	$B_{037}B_{036}B_{035}B_{034}B_{033}B_{032}B_{031}B_{030}$
133	01h	R85h	000100	$B_{047}B_{046}B_{045}B_{044}B_{043}B_{042}B_{041}B_{040}$
134	01h	R86h	000101	$B_{057}B_{056}B_{055}B_{054}B_{053}B_{052}B_{051}B_{050}$
135	01h	R87h	000110	$B_{067}B_{066}B_{065}B_{064}B_{063}B_{062}B_{061}B_{060}$
136	01h	R88h	000111	$B_{077}B_{076}B_{075}B_{074}B_{073}B_{072}B_{071}B_{070}$
137	01h	R89h	001000	$B_{087}B_{086}B_{085}B_{084}B_{083}B_{082}B_{081}B_{080}$
138	01h	R8Ah	001001	$B_{097}B_{096}B_{095}B_{094}B_{093}B_{092}B_{091}B_{090}$
139	01h	R8Bh	001010	$B_{107}B_{106}B_{105}B_{104}B_{103}B_{102}B_{101}B_{100}$
140	01h	R8Ch	001011	$B_{117}B_{116}B_{115}B_{114}B_{113}B_{112}B_{111}B_{110}$
141	01h	R8Dh	001100	$B_{127}B_{126}B_{125}B_{124}B_{123}B_{122}B_{121}B_{120}$
142	01h	R8Eh	001101	$B_{137}B_{136}B_{135}B_{134}B_{133}B_{132}B_{131}B_{130}$
143	01h	R8Fh	001110	$B_{147}B_{146}B_{145}B_{144}B_{143}B_{142}B_{141}B_{140}$
144	01h	R90h	001111	$B_{157}B_{156}B_{155}B_{154}B_{153}B_{152}B_{151}B_{150}$
145	01h	R91h	010000	B_{167} $B_{166}B_{165}$ $B_{164}B_{163}B_{162}B_{161}B_{160}$
146	01h	R92h	010001	$B_{177}B_{176}B_{175}B_{174}B_{173}B_{172}B_{171}B_{170}$
147	01h	R93h	010010	$B_{187}B_{186}B_{185}B_{184}B_{183}B_{182}B_{181}B_{180}$
148	01h	R94h	010011	$B_{197}B_{196}B_{195}B_{194}B_{193}B_{192}B_{191}B_{190}$
149	01h	R95h	010100	$B_{207}B_{206}B_{205}B_{204}B_{203}B_{202}B_{201}B_{200}$
150	01h	R96h	010101	$B_{217}B_{216}B_{215}B_{214}B_{213}B_{212}B_{211}B_{210}$
151	01h	R97h	010110	$B_{227}B_{226}B_{225}B_{224}B_{223}B_{222}B_{221}B_{220}$
152	01h	R98h	010111	$B_{237}B_{236}B_{235}B_{234}B_{233}B_{232}B_{231}B_{230}$
153	01h	R99h	011000	$B_{247}B_{246}B_{245}B_{244}B_{243}B_{242}B_{241}B_{240}$
154	01h	R9Ah	011001	$B_{257}B_{256}B_{255}B_{254}B_{253}B_{252}B_{251}B_{250}$
155	01h	R9Bh	011010	$B_{267}B_{266}B_{265}B_{264}B_{263}B_{262}B_{261}B_{260}$
156	01h	R9Ch	011011	$B_{277}B_{276}B_{275}B_{274}B_{273}B_{272}B_{271}B_{270}$
157	01h	R9Dh	011100	$B_{287}B_{286}B_{285}B_{284}B_{283}B_{282}B_{281}B_{280}$
158	01h	R9Eh	011101	$B_{297}B_{296}B_{295}B_{294}B_{293}B_{292}B_{291}B_{290}$
159	01h	R9Fh	011110	$B_{307}B_{306}B_{305}B_{304}B_{303}B_{302}B_{301}B_{300}$
160	01h	RA0h	011111	$B_{317}B_{316}B_{315}B_{314}B_{313}B_{312}B_{311}B_{310}$

Table 7. 24 DGLUT for Blue Color (1)

DGC_LUT Parameter byte	Command		B input (6 bit)	B output (8bit)
	Page	Address		
161	01h	RA1h	100000	B_{327} $B_{326}B_{325}$ $B_{324}B_{323}B_{322}B_{321}B_{320}$
162	01h	RA2h	100001	$B_{337}B_{336}B_{335}B_{334}B_{333}B_{332}B_{331}B_{330}$
163	01h	RA3h	100010	$B_{347}B_{346}B_{345}B_{344}B_{343}B_{342}B_{341}B_{340}$
164	01h	RA4h	100011	$B_{357}B_{356}B_{355}B_{354}B_{353}B_{352}B_{351}B_{350}$
165	01h	RA5h	100100	$B_{367}B_{366}B_{365}B_{364}B_{363}B_{362}B_{361}B_{360}$
166	01h	RA6h	100101	$B_{377}B_{376}B_{375}B_{374}B_{373}B_{372}B_{371}B_{370}$
167	01h	RA7h	100110	$B_{387}B_{386}B_{385}B_{384}B_{383}B_{382}B_{381}B_{380}$
168	01h	RA8h	100111	$B_{397}B_{396}B_{395}B_{394}B_{393}B_{392}B_{391}B_{390}$
169	01h	RA9h	101000	$B_{407}B_{406}B_{405}B_{404}B_{403}B_{402}B_{401}B_{400}$
170	01h	RAAh	101001	$B_{417}B_{416}B_{415}B_{414}B_{413}B_{412}B_{411}B_{410}$
171	01h	RABh	101010	$B_{427}B_{426}B_{425}B_{424}B_{423}B_{422}B_{421}B_{420}$
172	01h	RACh	101011	$B_{437}B_{436}B_{435}B_{434}B_{433}B_{432}B_{431}B_{430}$
173	01h	RADh	101100	$B_{447}B_{446}B_{445}B_{444}B_{443}B_{442}B_{441}B_{440}$
174	01h	RAEh	101101	$B_{457}B_{456}B_{455}B_{454}B_{453}B_{452}B_{451}B_{450}$
175	01h	RAFh	101110	$B_{467}B_{466}B_{465}B_{464}B_{463}B_{462}B_{461}B_{460}$
176	01h	RB0h	101111	$B_{477}B_{476}B_{475}B_{474}B_{473}B_{472}B_{471}B_{470}$
177	01h	RB1h	110000	B_{487} $B_{486}B_{485}$ $B_{484}B_{483}B_{482}B_{481}B_{480}$
178	01h	RB2h	110001	$B_{497}B_{496}B_{495}B_{494}B_{493}B_{492}B_{491}B_{490}$
179	01h	RB3h	110010	$B_{507}B_{506}B_{505}B_{504}B_{503}B_{502}B_{501}B_{500}$
180	01h	RB4h	110011	$B_{517}B_{516}B_{515}B_{514}B_{513}B_{512}B_{511}B_{510}$
181	01h	RB5h	110100	$B_{527}B_{526}B_{525}B_{524}B_{523}B_{522}B_{521}B_{520}$
182	01h	RB6h	110101	$B_{537}B_{536}B_{535}B_{534}B_{533}B_{532}B_{531}B_{530}$
183	01h	RB7h	110110	$B_{547}B_{546}B_{545}B_{544}B_{543}B_{542}B_{541}B_{540}$
184	01h	RB8h	110111	$B_{557}B_{556}B_{555}B_{554}B_{553}B_{552}B_{551}B_{550}$
185	01h	RB9h	111000	$B_{567}B_{566}B_{565}B_{564}B_{563}B_{562}B_{561}B_{560}$
186	01h	RBAh	111001	$B_{577}B_{576}B_{575}B_{574}B_{573}B_{572}B_{571}B_{570}$
187	01h	RBBh	111010	$B_{587}B_{586}B_{585}B_{584}B_{583}B_{582}B_{581}B_{580}$
188	01h	RBCh	111011	$B_{597}B_{596}B_{595}B_{594}B_{593}B_{592}B_{591}B_{590}$
189	01h	RBDh	111100	$B_{607}B_{606}B_{605}B_{604}B_{603}B_{602}B_{601}B_{600}$
190	01h	RBEh	111101	$B_{617}B_{616}B_{615}B_{614}B_{613}B_{612}B_{611}B_{610}$
191	01h	RBFh	111110	$B_{627}B_{626}B_{625}B_{624}B_{623}B_{622}B_{621}B_{620}$
192	01h	RC0h	111111	$B_{637}B_{636}B_{635}B_{634}B_{633}B_{632}B_{631}B_{630}$

Table 7. 25 DGLUT for Blue Color (2)

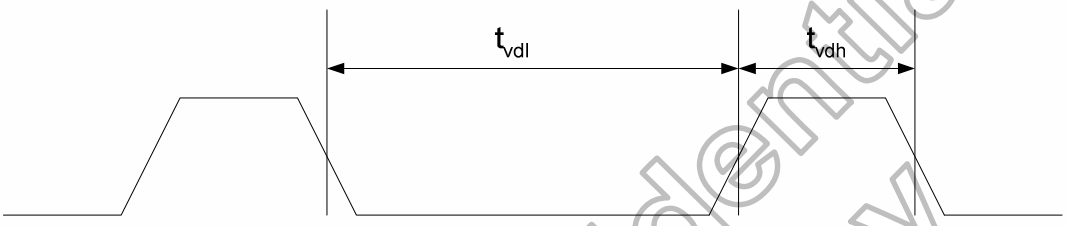
7.3 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

Tearing effect function is not support when in RGB interface mode

7.3.1 Tearing effect line modes

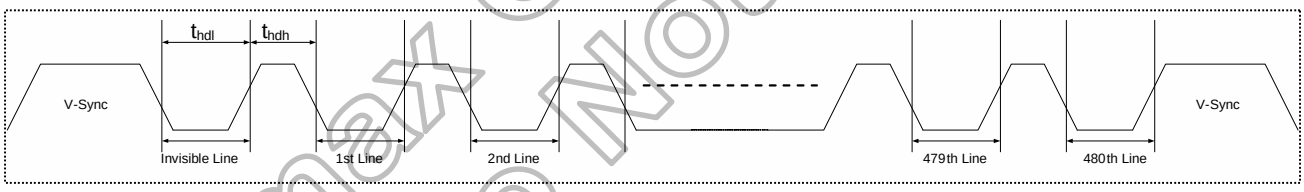
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh}= The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

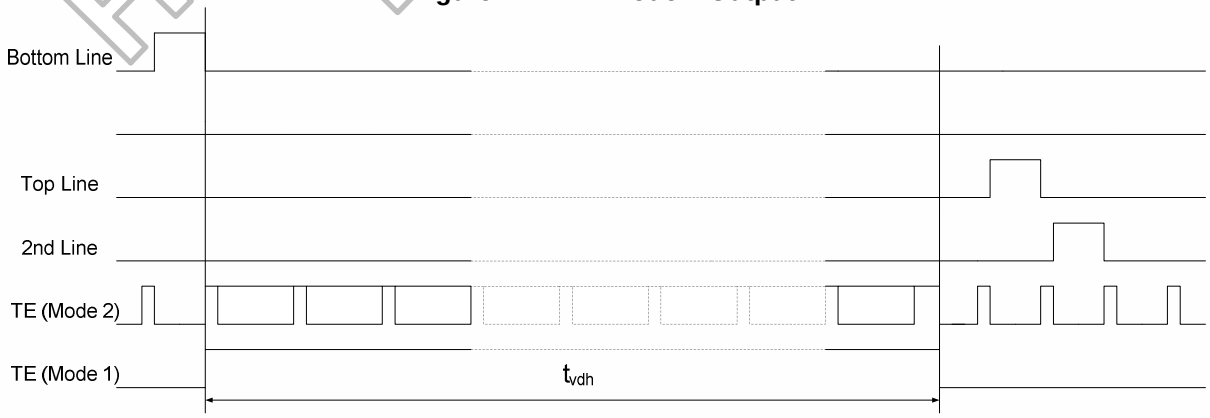
Figure 7. 11 TE Mode 1 Output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Figure 7. 12 TE Mode 2 Output



Note: During Sleep in Mode, the Tearing Output Pin is active Low

Figure 7. 13 TE Output Waveform

7.3.2 Tearing effect line timing

The Tearing Effect signal is described below.

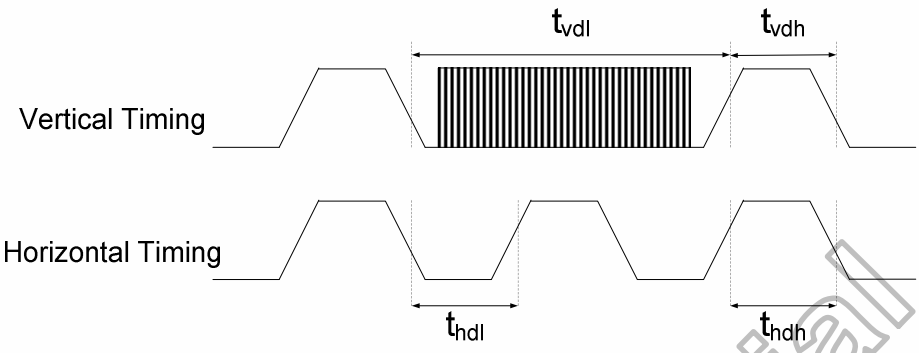


Figure 7. 14 Waveform of Tearing Effect Signal

Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Table 7. 26 AC characteristics of Tearing Effect Signal

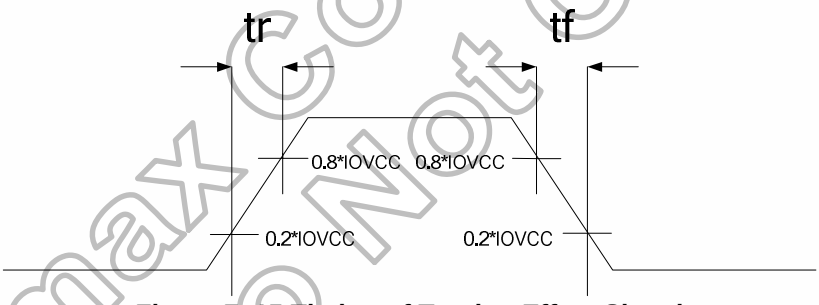


Figure 7. 15 Timing of Tearing Effect Signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

7.3.3 Example 1: MPU write is faster than panel read

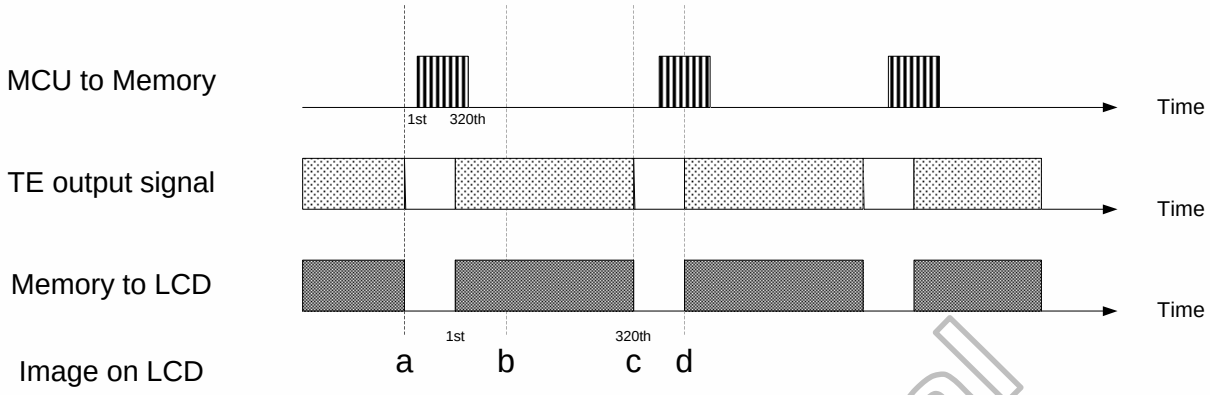


Figure 7. 16 Timing of MPU Write is faster than Panel Read

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image.

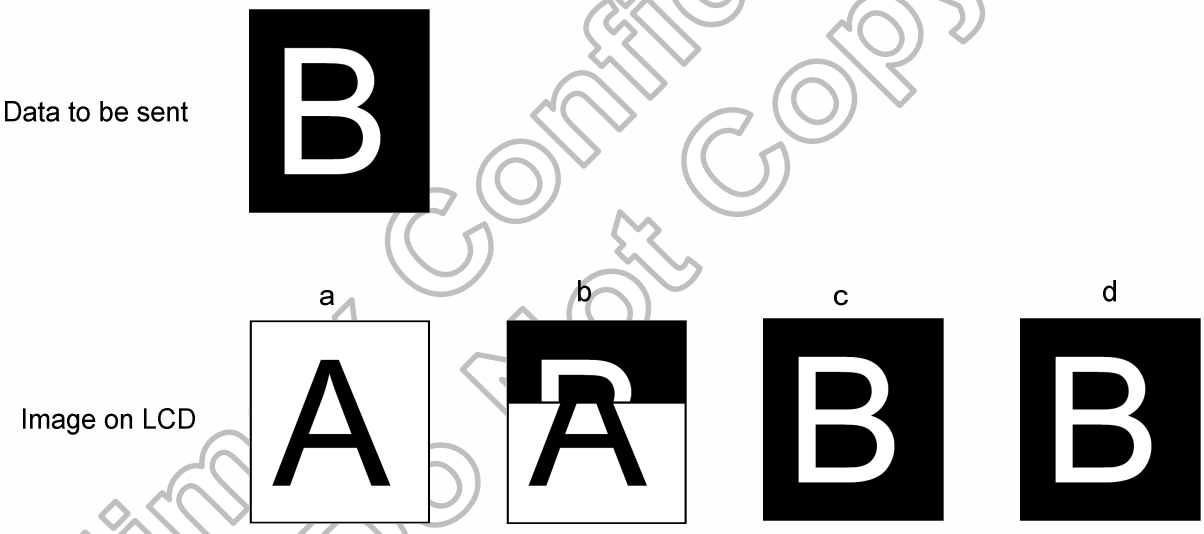


Figure 7. 17 Display of MPU Write is faster than Panel Read

7.3.4 Example 2: MPU write is slower than panel read

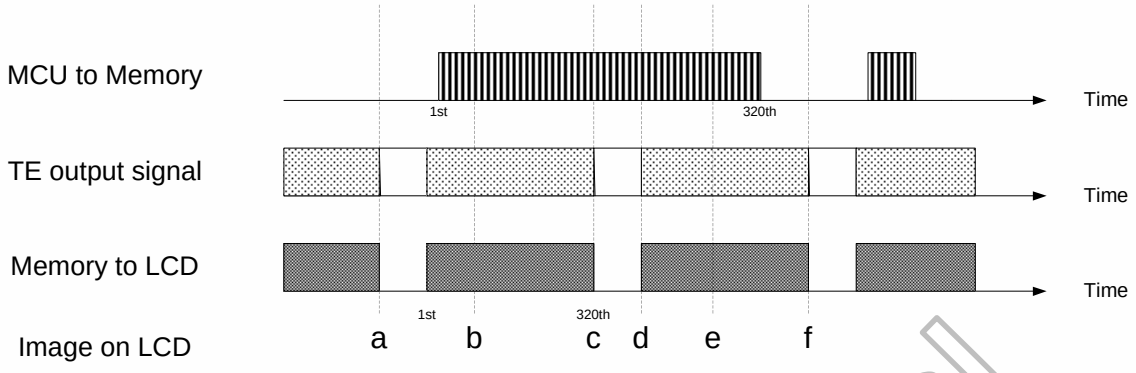


Figure 7. 18 Timing of MPU Write is slower than Panel Read

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

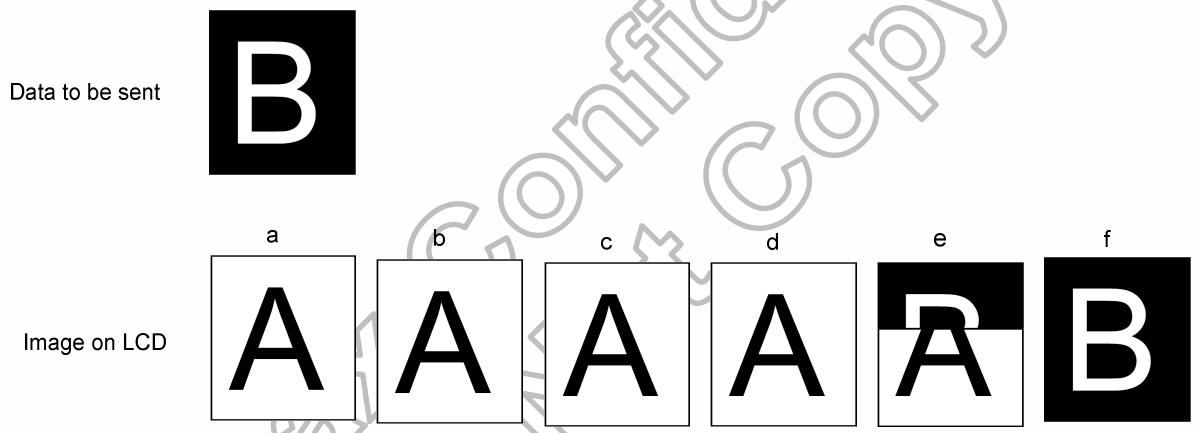


Figure 7. 19 Display of MPU Write is slower than Panel Read

7.4 Content adaptive brightness control (CABC) function

The HX8357-A has support Content Adaptive Brightness Control (CABC) Function and will output one PWM signal to external LED Driver IC. The PWM signal is automatics adjust output duty by display image for saving LED backlight power consumption.

Example:

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -10% brightness reduction

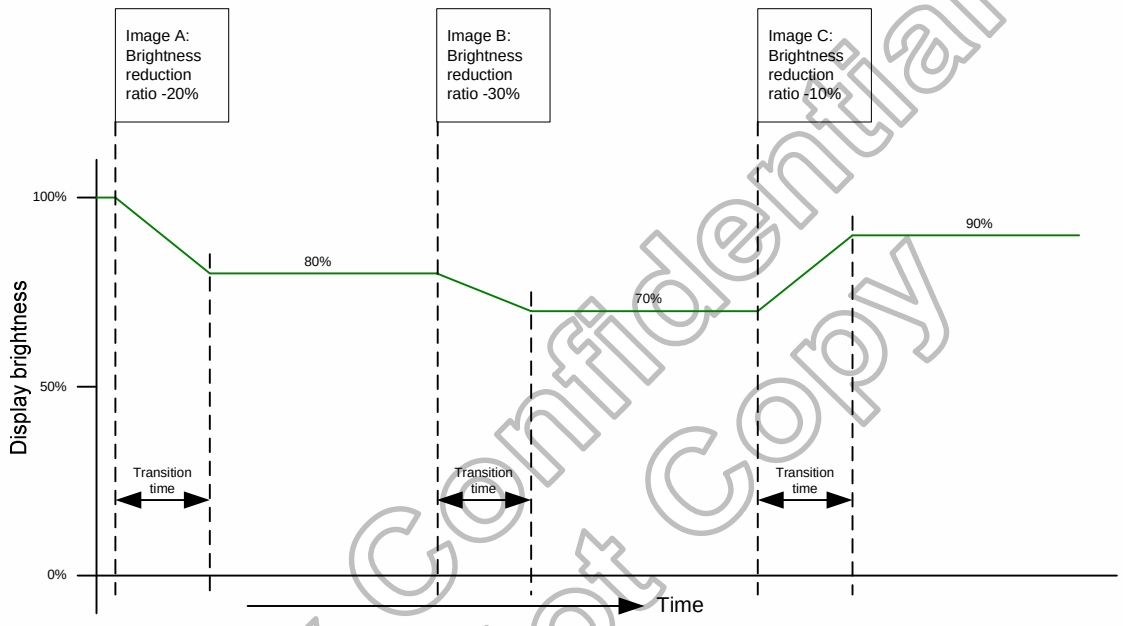


Figure 7. 20 Example of CABC Function

The general block diagram of the CABC and the brightness control is illustrated below:

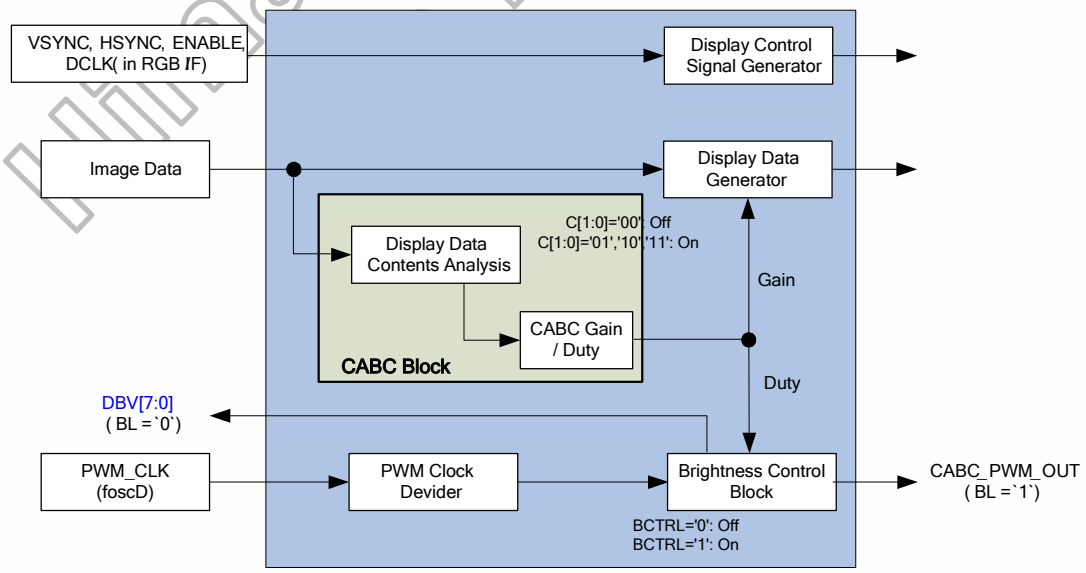
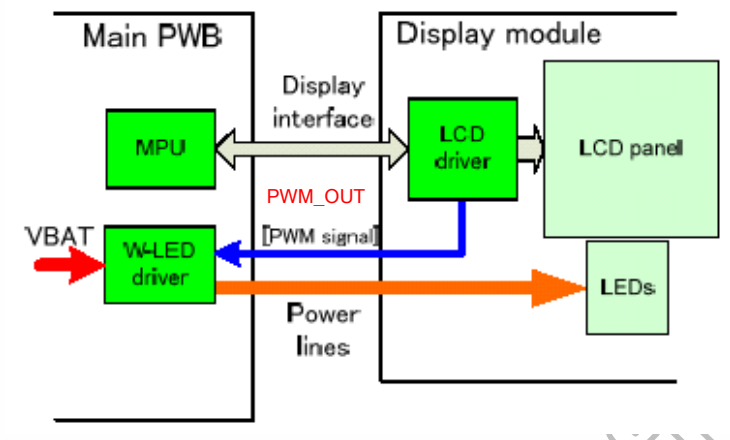


Figure 7. 21 CABC Block Diagram

7.4.1 Module architectures

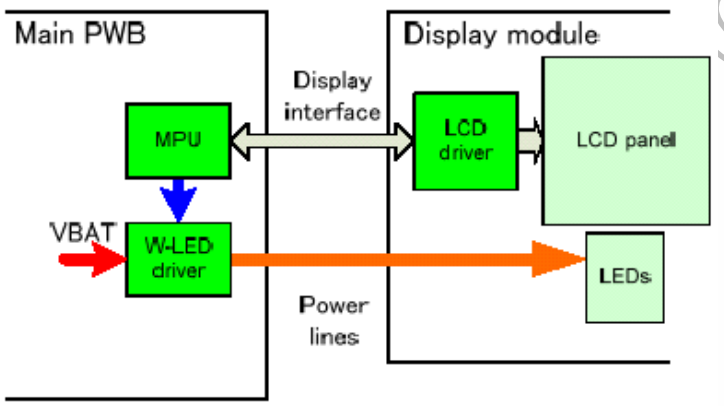
HX8357-A can support two module architectures for CABC operation. The **BL** bit setting of R3Dh can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- Architecture I



1. **BL** =`1` of R3Dh
2. LED backlight brightness for the display is controlled by external output “PWM_OUT”.

- Architecture II



1. **BL** =`0` of R3Dh
2. LED backlight brightness data for the display is read with DBV[7:0] bits of R3Ch.
3. Read commands R3Dh should be synchronized with V-sync.

7.4.2 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R3Ch, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as (DBV[7:0])/255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period = 2.95 ms, and DBV[7:0](R3Ch) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM_OUT duty = (228) / 255 x 74.42% ≡ 66.54%. Correspond to the CABC_PWM_OUT period = 2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.96ms, and the low-level of CABC_PWM_OUT = 0.99ms.

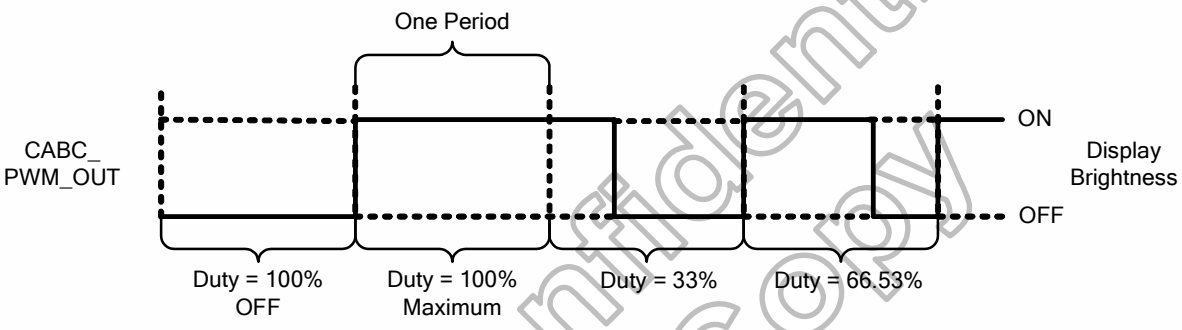


Figure 7. 22 CABC_PWM_OUT Output Duty

When Architecture II module is used (**BL**='0') with the example below, the CABC_PWM_OUT is always output low and the DBV[7:0](R3Ch) will be read a value as 169_{DEC} ((169)/255≡ 66.27%).

7.4.3 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of R3Fh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (**BCTRL='0'** of R3D), CABC minimum brightness setting is ignored. Read CABC minimum brightness **CMB[7:0]** (R3Fh) always read the setting value.

7.4.4 Display dimming

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another to avoid flicker in the actual display module. This dimming function curve is the same in increment and decrement directions.

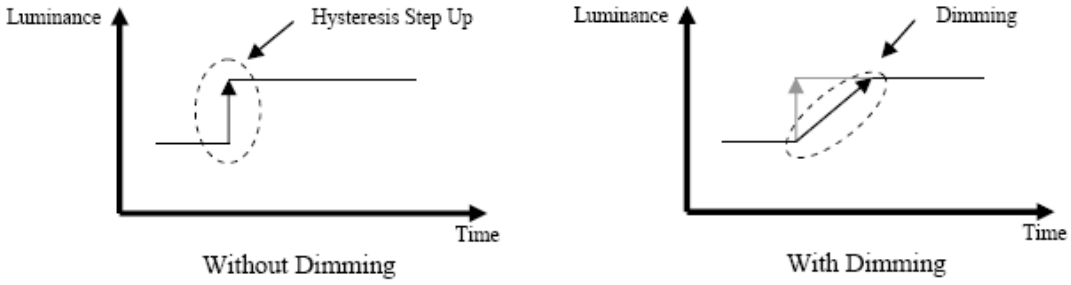


Figure 7. 23 Dimming Function

7.5 Scan mode setting

The HX8357-A can set internal register SM_PANEL and GS bits to determine the pin assignment of gate. The combination of SM_PANEL and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8357-A.

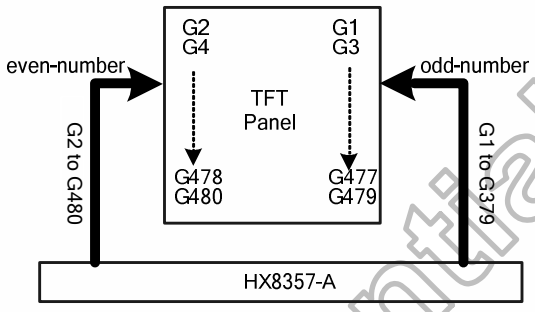
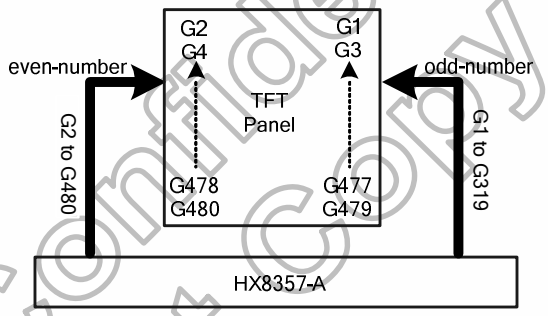
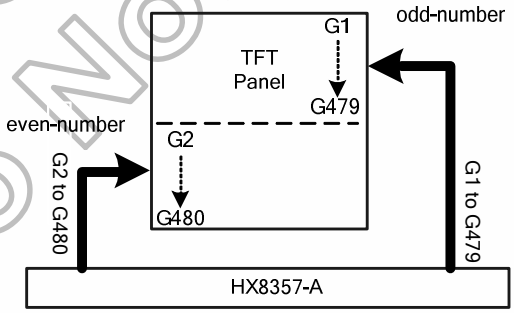
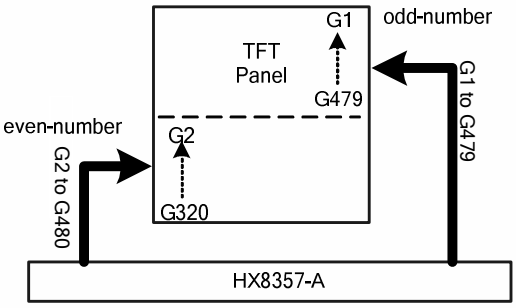
SM_PANEL	GS	Scan direction
0	0	 G1,G2,G3,... G157,G158,... G479,G480
0	1	 G480,G479,G478,... G158,G157,... G2,G1
1	0	 G1,G3... G477,G479,G2,G4,G56.. G480
1	1	 G480,G478... G4,G2,G479,G477,... G1

Figure 7. 24 Gate Scan Mode

7.6 System Power On/Off Sequence

IOVCC, VCC, VCI and MDDI_VDD can be applied in any order. IOVCC, VCC, VCI and MDDI_VDD can be powered down in any order. During power off, if LCD is in the Standby Out mode, IOVCC and VCC must be powered down minimum 120msec after RESX has been released. During power off, if LCD is in the Standby In mode, IOVCC, VCC and VCI can be powered down minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving STB Out command. Also between receiving STB In command and Power Off Sequence. If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.6.1 and 7.6.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The system power on/off sequence is illustrated below.

7.6.1 Case 1 – NRESET line is held High or Unstable by Host at Power On

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both IOVCC, VCC and VCI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

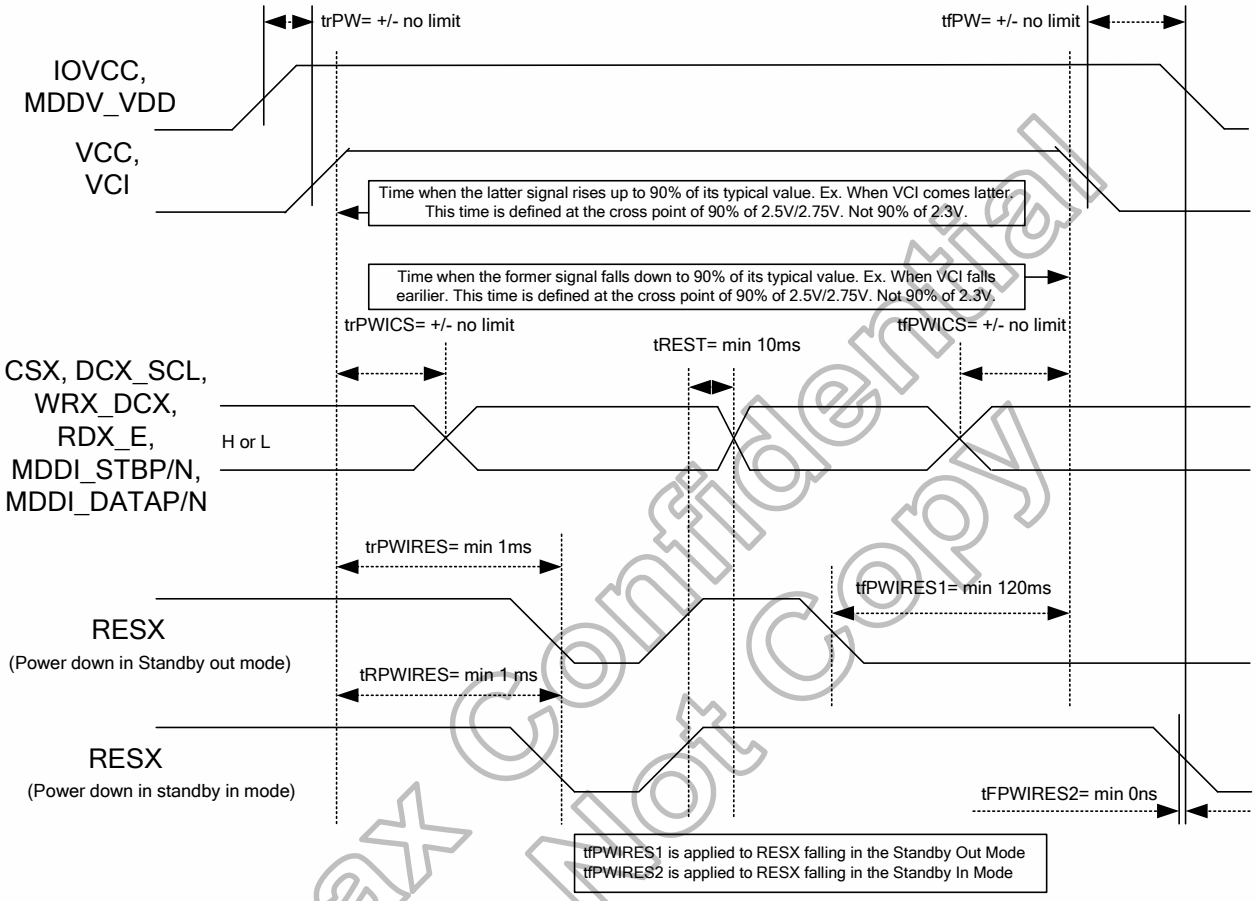


Figure 7. 25 Case 1 –RESX line is held High or Unstable by Host at Power On

7.6.2 Case 2 – NRESET line is held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 5msec after both IOVCC, VCC and VCI have been applied.

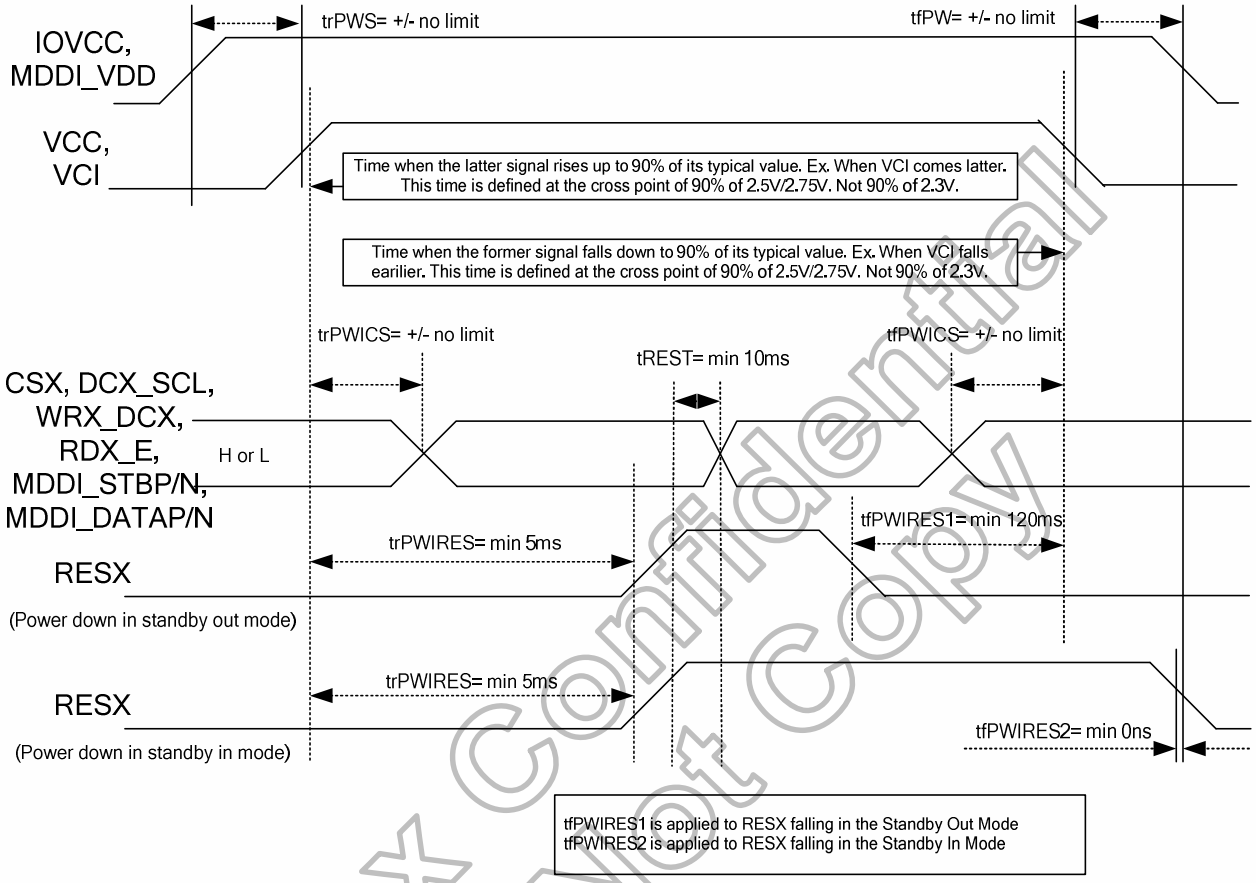


Figure 7. 26 Case 2 – RESX line is held Low by Host at Power On

7.7 LCD power generation circuit

7.7.1 Power supply circuit

The power circuit of HX8357-A is used to generate supply voltages for LCD panel driving.

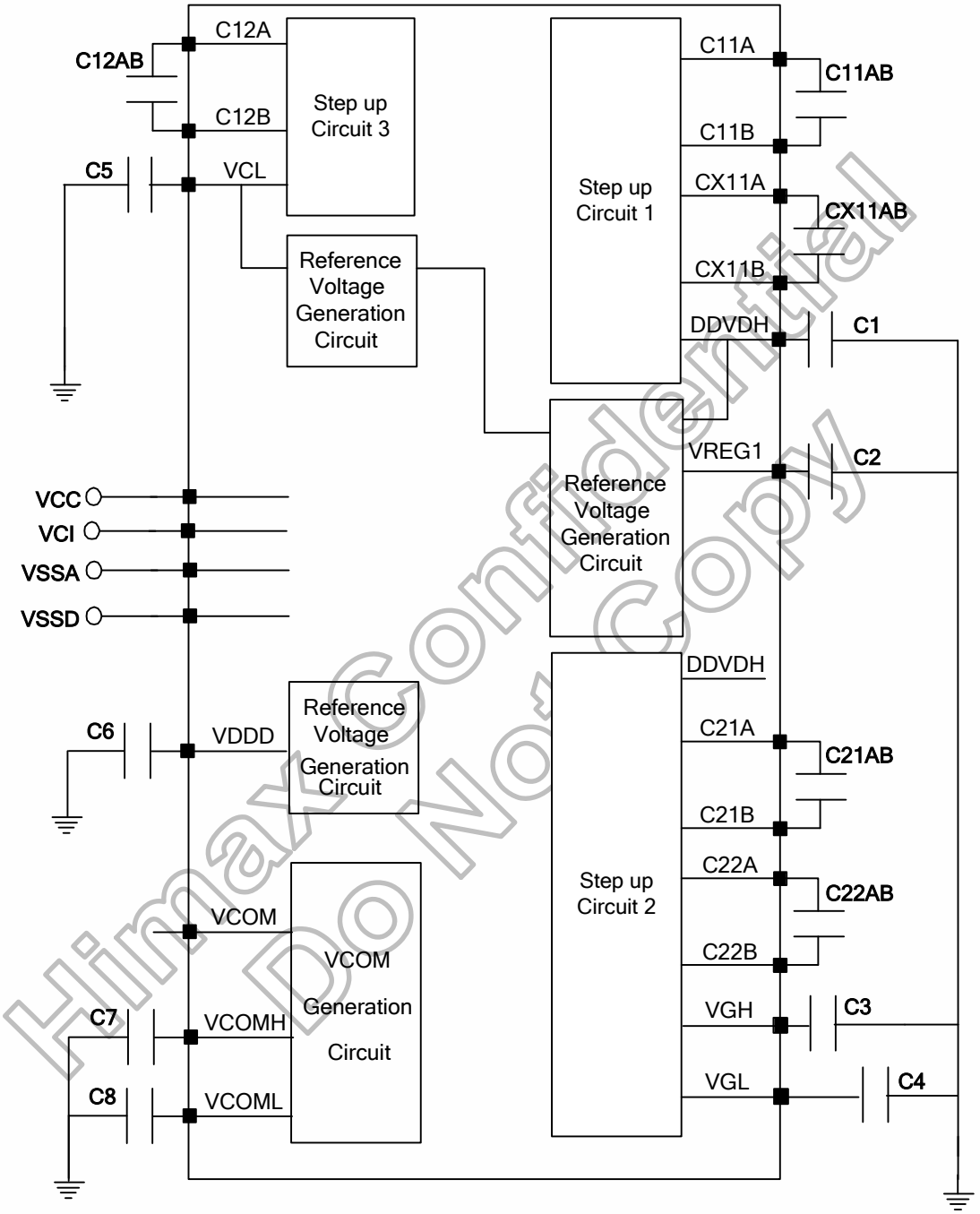


Figure 7. 27 The Block Diagram of HX8357-A Power Circuit

Specification of connected passive component

Capacitor	Recommended voltage	Capacity
C1 (DDVDH)	10V	1 µF (B characteristics)
C2 (VREG1)	10V	1 µF (B characteristics)
C3 (VGH)	25V	1 µF (B characteristics)
C4 (VGL)	16V	1 µF (B characteristics)
C5 (VCL)	6V	1 µF (B characteristics)
C6(VDDD)	6V	1 µF (B characteristics)
C7 (VCOMH)	10V	1 µF (B characteristics)
C8(VCOML)	6V	1 µF (B characteristics)
C11AB (C11A/B)	6V	1 µF (B characteristics)
CX11AB (CX11A/B)	6V	1 µF (B characteristics)
C12AB (C12A/B)	6V	1 µF (B characteristics)
C21AB (C21A/B)	10V	1 µF (B characteristics)
C22AB (C22A/B)	10V	1 µF (B characteristics)

Table 7. 27 The adoptability of Capacitor

7.7.2 LCD power generation scheme

The boost voltage generated is shown as below.

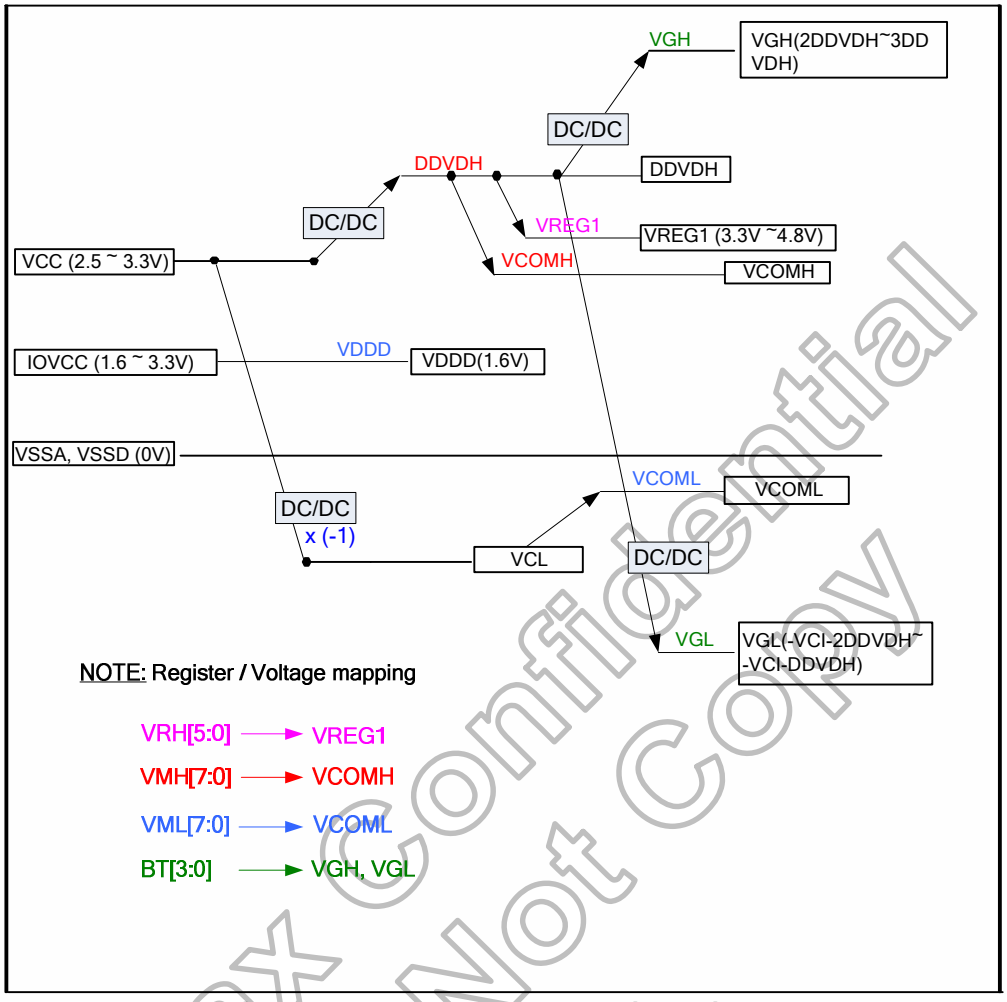


Figure 7. 28 LCD Power Generation Scheme

7.8 Internal Power on/off setting sequence

The following are the sequences of register setting flow that applied to this driver driving the TFT display, when operate in Register-Content interface mode.

Display on/off set flow

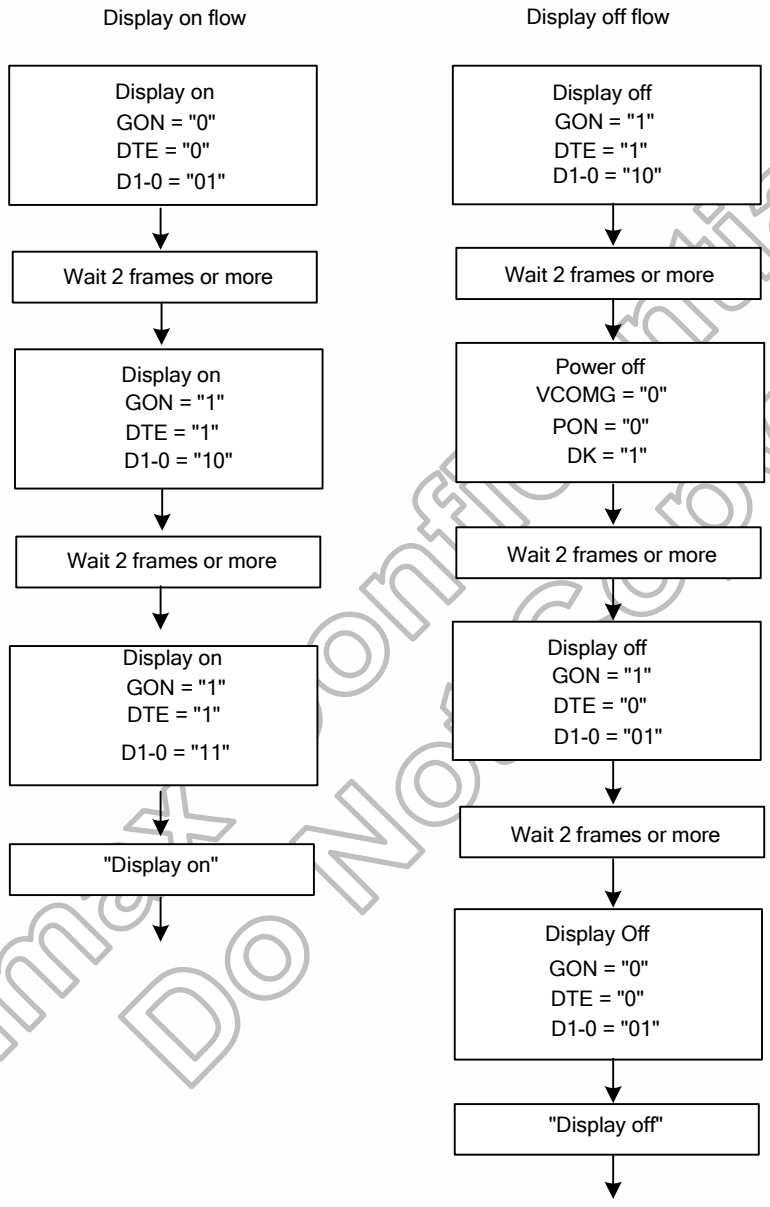


Figure 7. 29 Display On/Off Set flow

Sleep mode set up flow

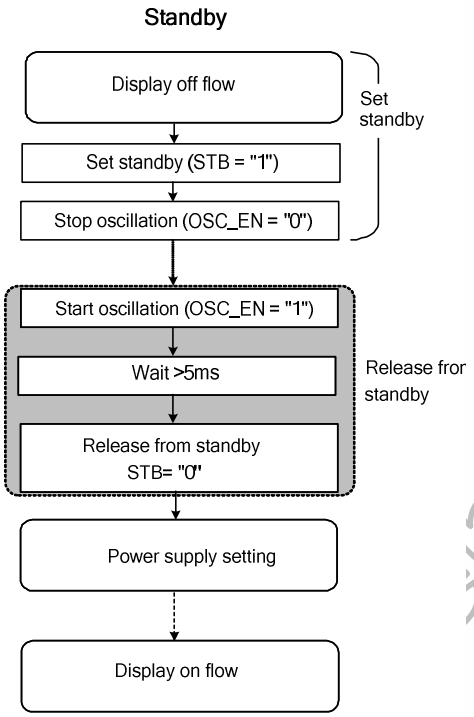


Figure 7. 30 Standby Mode Setting flow

Power on/off setting up flow

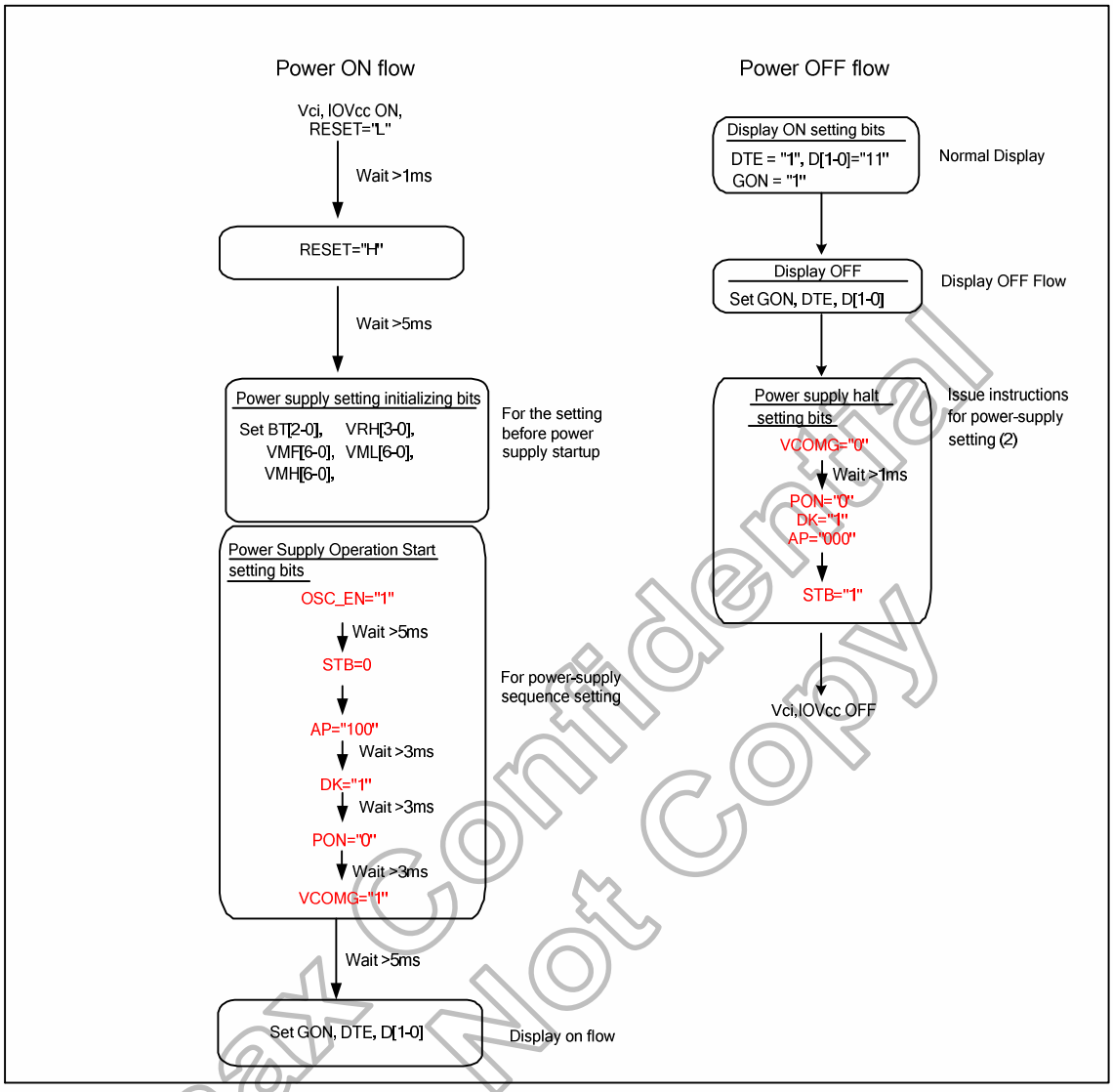


Figure 7. 31 Power Supply Setting Flow

7.9 Input / output pin state

7.9.1 Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDA	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
NISD	High	High
PWM_OUT	Low	Low

Table 7. 28 Characteristics of Output Pins

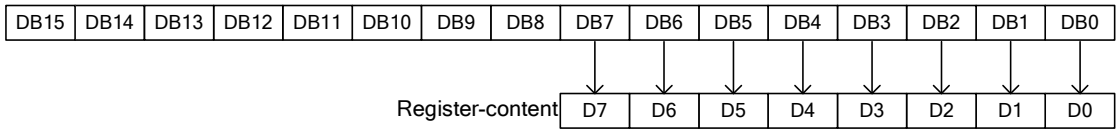
7.9.2 Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Section 11.4.4	Input valid	Input valid	Section 11.34.4
CSX	Input invalid	Input valid	Input valid	Input invalid
NWR_DCX	Input invalid	Input valid	Input valid	Input invalid
RDX_E	Input invalid	Input valid	Input valid	Input invalid
DCX_SCL	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
VS	Input invalid	Input valid	Input valid	Input invalid
HS	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
PCLK	Input invalid	Input valid	Input valid	Input invalid
DB[17:0]	Input invalid	Input valid	Input valid	Input invalid
MDDI_STBP/N	Input Invalid	Input valid	Input valid	Input Invalid
MDDI_DATAP/N	Input Invalid	Input valid	Input valid	Input Invalid
OSC, BS3,BS2, BS1,BS0, IFSEL, EXTC	Input invalid	Input valid	Input valid	Input invalid
TEST3-1	Input invalid	Input valid	Input valid	Input invalid

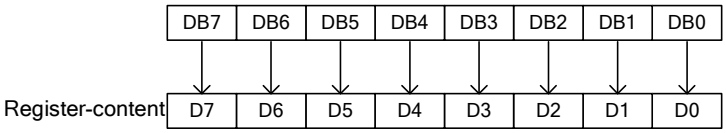
Table 7. 29 Characteristics of Input Pins

8. Command

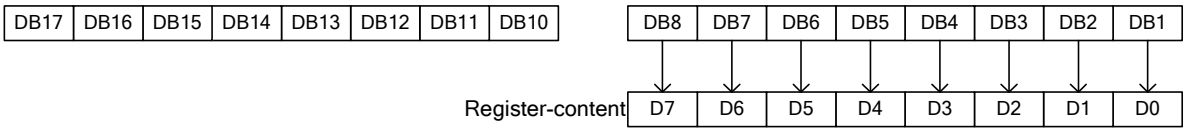
BS3~BS0 = “0000” 8080 MCU 16-bits Parallel type I



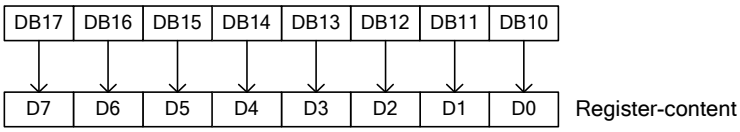
BS3~BS0 = “0001” 8080 MCU 8-bits Parallel type I



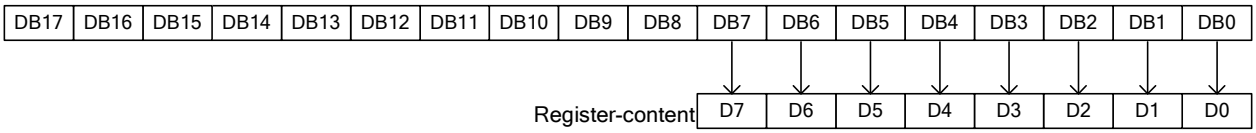
BS3~BS0 = “0010” 8080 MCU 16-bits Parallel type II



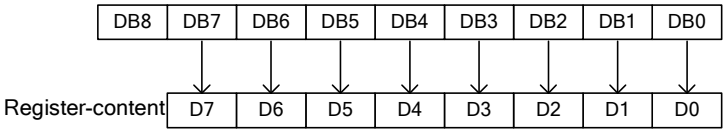
BS3~BS0 = “0011” 8080 MCU 8-bits Parallel type II



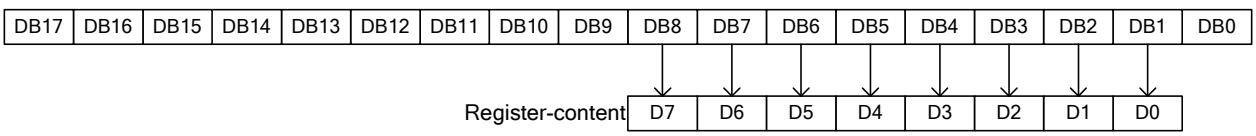
BS3~BS0 = “1000” 8080 MCU 18-bits Parallel type I



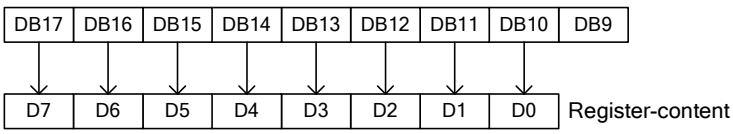
BS3~BS0 = “1001” 8080 MCU 9-bits Parallel type I



BS3~BS0 = “1010” 8080 MCU 18-bits Parallel type II



BS3~BS0 = “1011” 8080 MCU 9-bits Parallel type II



8.1 Command set

HX8357-A have two pages command set, can setting PAGE_SEL[1:0] to select command set page.

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R00h	Himax ID	R	-	0	1	0	1	0	1	1	1	
R01h	Display Mode control	W/R	-	DP_STB1 (0)	DP_STB0 (0)	-	-	SCROL (0)	IDMON (1)	INVON (0)	PTLON (0)	
R02h	Column address start 2	W/R	-	SC[15:8] (8'b0000_0000)								
R03h	Column address start 1	W/R	-	SC[7:0] (8'b0000_0000)								
R04h	Column address end 2	W/R	-	EC[15:8] (8'b0000_0001)								
R05h	Column address end 1	W/R	-	EC[7:0] (8'b0011_1111)								
R06h	Row address start 2	W/R	-	SP[15:8] (8'b0000_0000)								
R07h	Row address start 1	W/R	-	SP[7:0] (8'b0000_0000)								
R08h	Row address end 2	W/R	-	EP[15:8] (8'b0000_0001)								
R09h	Row address end 1	W/R	-	EP[7:0] (8'b0011_1111)								
R0Ah	Partial area start row 2	W/R	-	PSL[15:8] (8'b0000_0000)								
R0Bh	Partial area start row 1	W/R	-	PSL[7:0] (8'b0000_0000)								
R0Ch	Partial area end row 2	W/R	-	PEL[15:8] (8'b0000_0001)								
R0Dh	Partial area end row 1	W/R	-	PEL[7:0] (8'b0011_1111)								
R0Eh	Vertical Scroll Top fixed area 2	W/R	-	TFA[15:8] (8'b0000_0000)								
R0Fh	Vertical Scroll Top fixed area 1	W/R	-	TFA[7:0] (8'b0000_0000)								
R10h	Vertical Scroll height area 2	W/R	-	VSA[15:8] (8'b0000_0001)								
R11h	Vertical Scroll height area 1	W/R	-	VSA[7:0] (8'b0011_1111)								
R12h	Vertical Scroll Button area 2	W/R	-	BFA[15:8] (8'b0000_0000)								
R13h	Vertical Scroll Button area 1	W/R	-	BFA [7:0] (8'b0000_0000)								
R14h	Vertical Scroll Start address 2	W/R	-	VSP [15:8] (8'b0000_0000)								
R15h	Vertical Scroll Start address 1	W/R	-	VSP [7:0] (8'b0000_0000)								
R16h	Memory Access control	W/R	-	MY (0)	MX (0)	MV (0)	-	BGR (0)	-	SS (0)	GS (0)	
R17h	COLMOD	W/R	-	CSEL[3:0] (4b'0110)				-	IFPF[2:0] (3b'110)			
R18h	OSC Control 1	W/R	-	-	I/P_RADJ1[2:0] (3b'111)			-	N/P_RADJ0[2:0](3b'111)			*
R19h	OSC Control 2	W/R	-	-	-	-	-	-	-	-	OSC_EN(0)	
R1Ah	Power Control	W/R	-	-	-	-	-	BT[3:0] (0100)				
R1Bh	Power Control	W/R	-	-	-	VRH[5:0] (6'b01_0010)						
R1Ch	Power Control	W/R	-	-	-	-	-	-	AP[2:0] (011)			
R1Dh	Power Control	W/R	-	-	I/PI_FS0[2:0] (100)			-	N/P_FS0[2:0] (100)			
R1Eh	Power Control	W/R		-	I/PI_FS1[2:0] (100)			-	N/P_FS1[2:0] (100)			
R1Fh	Power Control 1	W/R	-	GASEN (1)	VCOMG (0)	-	PON(0)	DK(1)	XDK(0)	DDVDH_TRI(0)	STB(0)	
R22h	SRAM Control	W/R	SRAM Write/Read									
R23h	VCOM Control 1	W/R	-	VMF[7:0] (8'b1000_0000)								
R24h	VCOM Control 2	W/R	-	VMH[7:0] (8'b0011_1000)								
R25h	VCOM Control 3	W/R	-	VML[7:0] (8'b(0011_1000)								
R26h	Display Control 1	W/R	-	I/P_ISC[3:0] (0011)				N/P_ISC[3:0] (0011)				
R27h	Display Control 2	W/R	-	PT[1:0] (10)		PTV[1:0] (01)		-	-	PTG(1)	REF(1)	
R28h	Display Control 3	W/R	-	-	-	GON (1)	DTE (0)	D[1:0] (00)		-	-	
R29h	Frame Rate	W/R	-	I/P_RTN[3:0] (0000)				N/P_RTN[3:0] (0000)				

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
	control 1											
R2Ah	Frame Rate Control 2	W/R	-	-	-	I/P_DIV[1:0] (00)		-	-	N/P_DIV[1:0] (00)		
R2Bh	Frame Rate Control 3	W/R	-	N/P_DUM[7:0] (8,b0001_0010)								
R2Ch	Frame Rate Control 4	W/R	-	I/P_DUM[7:0] (8'b0001_0010)								
R2Dh	Cycle Control 2	W/R	-	GDON[7:0] (8'b0000_0011)								
R2Eh	Cycle Control 3	W/R	-	GDOF[7:0] (8'b1111_1000)								
R2Fh	Display inversion	W/R	-	-	I/P_NW[2:0](000)			-	N/P_NW[2:0] (001)			
R31h	RGB interface control 1	W/R	-	-	-	-	-	-	-	RCM[1:0] (00)		
R32h	RGB interface control 2	W/R	-	-	-	-	-	DPL (0)	HSPL (0)	VSPL (0)	EPL (0)	
R33h	RGB interface control 3	W/R	-	HBP[7:0] (8'b0000_1000)								
R34h	RGB interface control 4	W/R	-	HBP[9:8] (00)		VBP[5:0] (6'b00_0010)						
R36h	Panel Characteric	W/R	-	-	-	-	SM_Panel (0)	SS_Panel (0)	GS_Panel (0)	REV_Panel (0)	BGR_Panel (0)	
R38h	OTP Control 1	W/R	-	OTP_MASK[7:0]								
R39h	OTP Control 2	W/R	-	OTP_INDEX[7:0]								
R3Ah	OTP Control 3	W/R	-	OTP_LOAD_DISABLE (0)	OTP_TEST	OTP_POR(0)	OTP_PWE (0)	OTP_PTM[1:0]		VPP_SEL (0)	OTP_PROG (0)	
R3Bh	OTP Control 4	W/R	-	OTP_DATA[7:0]								
R3Ch	CABC Control 1	W/R	-	DBV[7:0](8'b0000_0000)								
R3Dh	CABC Control 2	W/R	-	-	-	BCTRL (0)	-	DD (0)	BL (0)	-	-	
R3Eh	CABC Control 3	W/R	-	-	-	-	-	-	-	CABC[1:0] (00)		
R3Fh	CABC Control 4	W/R	-	CMB[7:0](8'b0000_0000)								
R40h	r1 Control (1)	W/R	-	-	-	VRP0[5:0] (6'b00_0101)						
R41h	r1 Control (2)	W/R	-	-	-	VRP1[5:0] (6'b00_1101)						
R42h	r1 Control (3)	W/R	-	-	-	VRP2[5:0] (6'b01_0000)						
R43h	r1 Control (4)	W/R	-	-	-	VRP3[5:0] (6'b01_1011)						
R44h	r1 Control (5)	W/R	-	-	-	VRP4[5:0] (6'b01_1111)						
R45h	r1 Control (6)	W/R	-	-	-	VRP5[5:0] (6'b11_1010)						
R46h	r1 Control (7)	W/R	-	-	PRP0[6:0] (7'b010_1101)							
R47h	r1 Control (8)	W/R	-	-	PRP1[6:0] (7'b011_0111)							
R48h	r1 Control (9)	W/R	-	-	-	-	PKP0[4:0] (5'b0_1010)					
R49h	r1 Control (10)	W/R	-	-	-	-	PKP1[4:0] (5'b1_0001)					
R4Ah	r1 Control (11)	W/R	-	-	-	-	PKP2[4:0] (5'b1_0001)					
R4Bh	r1 Control (12)	W/R	-	-	-	-	PKP3[4:0] (5'b1_0101)					
R4Ch	r1 Control (13)	W/R	-	-	-	-	PKP4[4:0] (5'b1_0110)					
R50h	r1 Control (18)	W/R	-	-	-	VRN0[5:0] (6'b00_0101)						
R51h	r1 Control (19)	W/R	-	-	-	VRN1[5:0] (6'b10_0000)						
R52h	r1 Control (20)	W/R	-	-	-	VRN2[5:0] (6'b10_0100)						
R53h	r1 Control (21)	W/R	-	-	-	VRN3[5:0] (6'b10_1111)						
R54h	r1 Control (22)	W/R	-	-	-	VRN4[5:0] (6'b11_0010)						
R55h	r1 Control (23)	W/R	-	-	-	VRN5[5:0] (6'b11_1010)						
R56h	r1 Control (24)	W/R	-	-	PRN0[6:0] (7'b010_0000)							
R57h	r1 Control (25)	W/R	-	-	PRN1[6:0] (7'b010_1010)							
R58h	r1 Control (26)	W/R	-	-	-	PKN0[4:0] (5'b0_0111)						
R59h	r1 Control (27)	W/R	-	-	-	PKN1[4:0] (5'b0_1100)						
R5Ah	r1 Control (28)	W/R	-	-	-	PKN2[4:0] (5'b0_1010)						
R5Bh	r1 Control (29)	W/R	-	-	-	PKN3[4:0] (5'b0_1010)						
R5Ch	r1 Control (30)	W/R	-	-	-	PKN4[4:0] (5'b0_1001)						
R5Dh	r1 Control (35)	W/R	-	CGMN1[1:0]		CGMN0[1:0]		CGMN1[1:0]		CGMN0[1:0]		
R60h	TE Control	W/R	-	-	-	-	TE_mode (0)	TE (0)	-	-	-	
R61h	ID1	W/R	-	ID1[7:0](8'b0000_0000)								
R62h	ID2	W/R	-	ID2[7:0](8'b0000_0000)								
R63h	ID3	W/R	-	ID3[7:0](8'b0000_0000)								
R64h	ID4	W/R	-	ID4[7:0](8'b0000_0000)								
R68h	MDDI Control 4	W/R	-	VWAKE (0)	WKL[8] (0)	-	-	WKF[3:0] (0000)				
R69h	MDDI Control 5	W/R	-	WKL[7:0] (8'b0000_0000)								

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R6Bh	GPIO Control 1	W/R	-	GPIO[7:0] (8'b0000_0000)								
R6Ch	GPIO Control 2	W/R	-	GPIO_CON[7:0] (8'b0000_0000)								
R6Dh	GPIO Control 3	W/R	-	GPIO_EN[7:0] (8'b0000_0000)								
R6Eh	GPIO Control 4	W/R	-	GPIO_POL[7:0] (8'b0000_0000)								
R6Fh	GPIO Control 5	W/R	-	GPIO_CLR[7:0] (8'b0000_0000)								
R70h	SUB_PANEL Control 1	W/R	-	SUB_WR[15:8] (8'b0000_0000)								
R71h	SUB_PANEL Control 2	W/R	-	SUB_WR[7:0] (8'b0000_0000)								
R72h	SUB_PANEL Control 3	W/R	-	SUB_SEL[7:0] (8'b0000_0000)								
R73h	SUB_PANEL Control 4	W/R	-	SUB_EN (0)	SUB_RS [1:0]		MPU_ MODE (0)	STN_EN (0)	-	SUB_IM [1:0] (00)		
R80h	Column address counter 2	W/R	-	CAC[15:8] (8'b0000_0000)								
R81h	Column address counter 1	W/R	-	CAC[7:0] (8'b0000_0000)								
R82h	Row address counter 2	W/R	-	RAC[15:8] (8'b0000_0000)								
R83h	Row address counter 1	W/R	-	RAC[7:0] (8'b0000_0000)								
RE4h	Power saving counter 1	W/R	-	EQVCI_M1[7:0]								
RE5h	Power saving counter 2	W/R	-	EQGND_M1[7:0]								
RE6h	Power saving counter 3	W/R	-	EQVCI_M0[7:0]								
RE7h	Power saving counter 4	W/R	-	EQGND_M0[7:0]								
RFDh	Set SPI Rrad Index	W	-	INDEX[7:0]								
RFEh	Get SPI Index data	R	-	DATA[7:0]								
RFFh	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0] (00)		

Table 8. 1 List Table of Command Set page 0

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R00h	DGC control	W/R	-	-	-	-	-	-	-	-	DGC_EN (0)	
R01h	DGC LUT1	W/R	-	DGC_LUT_R00								
R02h	DGC LUT2	W/R	-	DGC_LUT_R01								
R03h	DGC LUT3	W/R	-	DGC_LUT_R02								
R04h	DGC LUT4	W/R	-	DGC_LUT_R03								
R05h	DGC LUT5	W/R	-	DGC_LUT_R04								
R06h	DGC LUT6	W/R	-	DGC_LUT_R05								
R07h	DGC LUT7	W/R	-	DGC_LUT_R06								
R08h	DGC LUT8	W/R	-	DGC_LUT_R07								
R09h	DGC LUT9	W/R	-	DGC_LUT_R08								
R0Ah	DGC LUT10	W/R	-	DGC_LUT_R09								
R0Bh	DGC LUT11	W/R	-	DGC_LUT_R10								
R0Ch	DGC LUT12	W/R	-	DGC_LUT_R11								
R0Dh	DGC LUT13	W/R	-	DGC_LUT_R12								
R0Eh	DGC LUT14	W/R	-	DGC_LUT_R13								
R0Fh	DGC LUT15	W/R	-	DGC_LUT_R14								
R10h	DGC LUT16	W/R	-	DGC_LUT_R15								
R11h	DGC LUT17	W/R	-	DGC_LUT_R16								
R12h	DGC LUT18	W/R	-	DGC_LUT_R17								
R13h	DGC LUT19	W/R	-	DGC_LUT_R18								
R14h	DGC LUT20	W/R	-	DGC_LUT_R19								
R15h	DGC LUT21	W/R	-	DGC_LUT_R20								
R16h	DGC LUT22	W/R	-	DGC_LUT_R21								
R17h	DGC LUT23	W/R	-	DGC_LUT_R22								
R18h	DGC LUT24	W/R	-	DGC_LUT_R23								*
R19h	DGC LUT25	W/R	-	DGC_LUT_R24								
R1Ah	DGC LUT26	W/R	-	DGC_LUT_R25								
R1Bh	DGC LUT27	W/R	-	DGC_LUT_R26								
R1Ch	DGC LUT28	W/R	-	DGC_LUT_R27								
R1Dh	DGC LUT29	W/R	-	DGC_LUT_R28								
R1Eh	DGC LUT30	W/R	-	DGC_LUT_R29								
R1Fh	DGC LUT31	W/R	-	DGC_LUT_R30								
R20h	DGC LUT32	W/R	-	DGC_LUT_R31								
R21h	DGC LUT33	W/R	-	DGC_LUT_R32								
R22h	DGC LUT34	W/R	-	DGC_LUT_R33								
R23h	DGC LUT35	W/R	-	DGC_LUT_R34								
R24h	DGC LUT36	W/R	-	DGC_LUT_R35								
R25h	DGC LUT37	W/R	-	DGC_LUT_R36								
R26h	DGC LUT38	W/R	-	DGC_LUT_R37								
R27h	DGC LUT39	W/R	-	DGC_LUT_R38								
R28h	DGC LUT40	W/R	-	DGC_LUT_R39								
R29h	DGC LUT41	W/R	-	DGC_LUT_R40								
R2Ah	DGC LUT42	W/R	-	DGC_LUT_R41								
R2Bh	DGC LUT43	W/R	-	DGC_LUT_R42								
R2Ch	DGC LUT44	W/R	-	DGC_LUT_R43								
R2Dh	DGC LUT45	W/R	-	DGC_LUT_R44								
R2Eh	DGC LUT46	W/R	-	DGC_LUT_R45								
R2Fh	DGC LUT47	W/R	-	DGC_LUT_R46								
R30h	DGC LUT48	W/R	-	DGC_LUT_R47								
R31h	DGC LUT49	W/R	-	DGC_LUT_R48								
R32h	DGC LUT50	W/R	-	DGC_LUT_R49								
R33h	DGC LUT51	W/R	-	DGC_LUT_R50								
R34h	DGC LUT52	W/R	-	DGC_LUT_R51								
R35h	DGC LUT53	W/R	-	DGC_LUT_R52								
R36h	DGC LUT54	W/R	-	DGC_LUT_R53								
R37h	DGC LUT55	W/R	-	DGC_LUT_R54								
R38h	DGC LUT56	W/R	-	DGC_LUT_R55								
R39h	DGC LUT57	W/R	-	DGC_LUT_R56								
R3Ah	DGC LUT58	W/R	-	DGC_LUT_R57								
R3Bh	DGC LUT59	W/R	-	DGC_LUT_R58								
R3Ch	DGC LUT60	W/R	-	DGC_LUT_R59								
R3Dh	DGC LUT61	W/R	-	DGC_LUT_R60								
R3Eh	DGC LUT62	W/R	-	DGC_LUT_R61								
R3Fh	DGC LUT63	W/R	-	DGC_LUT_R62								
R40h	DGC LUT64	W/R	-	DGC_LUT_R63								
R41h	DGC LUT65	W/R	-	DGC_LUT_G00								

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R42h	DGC LUT66	W/R	-	DGC_LUT_G01								
R43h	DGC LUT67	W/R	-	DGC_LUT_G02								
R44h	DGC LUT68	W/R	-	DGC_LUT_G03								
R45h	DGC LUT69	W/R	-	DGC_LUT_G04								
R46h	DGC LUT70	W/R	-	DGC_LUT_G05								
R47h	DGC LUT71	W/R	-	DGC_LUT_G06								
R48h	DGC LUT72	W/R	-	DGC_LUT_G07								
R49h	DGC LUT73	W/R	-	DGC_LUT_G08								
R4Ah	DGC LUT74	W/R	-	DGC_LUT_G09								
R4Bh	DGC LUT75	W/R	-	DGC_LUT_G10								
R4Ch	DGC LUT76	W/R	-	DGC_LUT_G11								
R4Dh	DGC LUT77	W/R	-	DGC_LUT_G12								
R4Eh	DGC LUT78	W/R	-	DGC_LUT_G13								
R4Fh	DGC LUT79	W/R	-	DGC_LUT_G14								
R50h	DGC LUT80	W/R	-	DGC_LUT_G15								
R51h	DGC LUT81	W/R	-	DGC_LUT_G16								
R52h	DGC LUT82	W/R	-	DGC_LUT_G17								
R53h	DGC LUT83	W/R	-	DGC_LUT_G18								
R54h	DGC LUT84	W/R	-	DGC_LUT_G19								
R55h	DGC LUT85	W/R	-	DGC_LUT_G20								
R56h	DGC LUT86	W/R	-	DGC_LUT_G21								
R57h	DGC LUT87	W/R	-	DGC_LUT_G22								
R58h	DGC LUT88	W/R	-	DGC_LUT_G23								
R59h	DGC LUT89	W/R	-	DGC_LUT_G24								
R5Ah	DGC LUT90	W/R	-	DGC_LUT_G25								
R5Bh	DGC LUT91	W/R	-	DGC_LUT_G26								
R5Ch	DGC LUT92	W/R	-	DGC_LUT_G27								
R5Dh	DGC LUT93	W/R	-	DGC_LUT_G28								
R5Eh	DGC LUT94	W/R	-	DGC_LUT_G29								
R5Fh	DGC LUT95	W/R	-	DGC_LUT_G30								
R60h	DGC LUT96	W/R	-	DGC_LUT_G31								
R61h	DGC LUT97	W/R	-	DGC_LUT_G32								
R62h	DGC LUT98	W/R	-	DGC_LUT_G33								
R63h	DGC LUT99	W/R	-	DGC_LUT_G34								
R64h	DGC LUT100	W/R	-	DGC_LUT_G35								
R65h	DGC LUT101	W/R	-	DGC_LUT_G36								
R66h	DGC LUT102	W/R	-	DGC_LUT_G37								
R67h	DGC LUT103	W/R	-	DGC_LUT_G38								
R68h	DGC LUT104	W/R	-	DGC_LUT_G39								
R69h	DGC LUT105	W/R	-	DGC_LUT_G40								
R6Ah	DGC LUT106	W/R	-	DGC_LUT_G41								
R6Bh	DGC LUT107	W/R	-	DGC_LUT_G42								
R6Ch	DGC LUT108	W/R	-	DGC_LUT_G43								
R6Dh	DGC LUT109	W/R	-	DGC_LUT_G44								
R6Eh	DGC LUT110	W/R	-	DGC_LUT_G45								
R6Fh	DGC LUT111	W/R	-	DGC_LUT_G46								
R70h	DGC LUT112	W/R	-	DGC_LUT_G47								
R71h	DGC LUT113	W/R	-	DGC_LUT_G48								
R72h	DGC LUT114	W/R	-	DGC_LUT_G49								
R73h	DGC LUT115	W/R	-	DGC_LUT_G50								
R74h	DGC LUT116	W/R	-	DGC_LUT_G51								
R75h	DGC LUT117	W/R	-	DGC_LUT_G52								
R76h	DGC LUT118	W/R	-	DGC_LUT_G53								
R77h	DGC LUT119	W/R	-	DGC_LUT_G54								
R78h	DGC LUT120	W/R	-	DGC_LUT_G55								
R79h	DGC LUT121	W/R	-	DGC_LUT_G56								
R7Ah	DGC LUT122	W/R	-	DGC_LUT_G57								
R7Bh	DGC LUT123	W/R	-	DGC_LUT_G58								
R7Ch	DGC LUT124	W/R	-	DGC_LUT_G59								
R7Dh	DGC LUT125	W/R	-	DGC_LUT_G60								
R7Eh	DGC LUT126	W/R	-	DGC_LUT_G61								
R7Fh	DGC LUT127	W/R	-	DGC_LUT_G62								
R80h	DGC LUT128	W/R	-	DGC_LUT_G63								
R81h	DGC LUT129	W/R	-	DGC_LUT_B00								
R82h	DGC LUT130	W/R	-	DGC_LUT_B01								
R83h	DGC LUT131	W/R	-	DGC_LUT_B02								
R84h	DGC LUT132	W/R	-	DGC_LUT_B03								
R85h	DGC LUT133	W/R	-	DGC_LUT_B04								

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R86h	DGC LUT134	W/R	-	DGC_LUT_B05								
R87h	DGC LUT135	W/R	-	DGC_LUT_B06								
R88h	DGC LUT136	W/R	-	DGC_LUT_B07								
R89h	DGC LUT137	W/R	-	DGC_LUT_B08								
R8Ah	DGC LUT138	W/R	-	DGC_LUT_B09								
R8Bh	DGC LUT139	W/R	-	DGC_LUT_B10								
R8Ch	DGC LUT140	W/R	-	DGC_LUT_B11								
R8Dh	DGC LUT141	W/R	-	DGC_LUT_B12								
R8Eh	DGC LUT142	W/R	-	DGC_LUT_B13								
R8Fh	DGC LUT143	W/R	-	DGC_LUT_B14								
R90h	DGC LUT144	W/R	-	DGC_LUT_B15								
R91h	DGC LUT145	W/R	-	DGC_LUT_B16								
R92h	DGC LUT146	W/R	-	DGC_LUT_B17								
R93h	DGC LUT147	W/R	-	DGC_LUT_B18								
R94h	DGC LUT148	W/R	-	DGC_LUT_B19								
R95h	DGC LUT149	W/R	-	DGC_LUT_B20								
R96h	DGC LUT150	W/R	-	DGC_LUT_B21								
R97h	DGC LUT151	W/R	-	DGC_LUT_B22								
R98h	DGC LUT152	W/R	-	DGC_LUT_B23								
R99h	DGC LUT153	W/R	-	DGC_LUT_B24								
R9Ah	DGC LUT154	W/R	-	DGC_LUT_B25								
R9Bh	DGC LUT155	W/R	-	DGC_LUT_B26								
R9Ch	DGC LUT156	W/R	-	DGC_LUT_B27								
R9Dh	DGC LUT157	W/R	-	DGC_LUT_B28								
R9Eh	DGC LUT158	W/R	-	DGC_LUT_B29								
R9Fh	DGC LUT159	W/R	-	DGC_LUT_B30								
RA0h	DGC LUT160	W/R	-	DGC_LUT_B31								
RA1h	DGC LUT161	W/R	-	DGC_LUT_B32								
RA2h	DGC LUT162	W/R	-	DGC_LUT_B33								
RA3h	DGC LUT163	W/R	-	DGC_LUT_B34								
RA4h	DGC LUT164	W/R	-	DGC_LUT_B35								
RA5h	DGC LUT165	W/R	-	DGC_LUT_B36								
RA6h	DGC LUT166	W/R	-	DGC_LUT_B37								
RA7h	DGC LUT167	W/R	-	DGC_LUT_B38								
RA8h	DGC LUT168	W/R	-	DGC_LUT_B39								
RA9h	DGC LUT169	W/R	-	DGC_LUT_B40								
RAAh	DGC LUT170	W/R	-	DGC_LUT_B41								
RABh	DGC LUT171	W/R	-	DGC_LUT_B42								
RACh	DGC LUT172	W/R	-	DGC_LUT_B43								
RADh	DGC LUT173	W/R	-	DGC_LUT_B44								
RAEh	DGC LUT174	W/R	-	DGC_LUT_B45								
RAFh	DGC LUT175	W/R	-	DGC_LUT_B46								
RB0h	DGC LUT176	W/R	-	DGC_LUT_B47								
RB1h	DGC LUT177	W/R	-	DGC_LUT_B48								
RB2h	DGC LUT178	W/R	-	DGC_LUT_B49								
RB3h	DGC LUT179	W/R	-	DGC_LUT_B50								
RB4h	DGC LUT180	W/R	-	DGC_LUT_B51								
RB5h	DGC LUT181	W/R	-	DGC_LUT_B52								
RB6h	DGC LUT182	W/R	-	DGC_LUT_B53								
RB7h	DGC LUT183	W/R	-	DGC_LUT_B54								
RB8h	DGC LUT184	W/R	-	DGC_LUT_B55								
RB9h	DGC LUT185	W/R	-	DGC_LUT_B56								
RBAh	DGC LUT186	W/R	-	DGC_LUT_B57								
RBBh	DGC LUT187	W/R	-	DGC_LUT_B58								
RBCh	DGC LUT188	W/R	-	DGC_LUT_B59								
RBDh	DGC LUT189	W/R	-	DGC_LUT_B60								
RBEh	DGC LUT190	W/R	-	DGC_LUT_B61								
RBFh	DGC LUT191	W/R	-	DGC_LUT_B62								
RC0h	DGC LUT192	W/R	-	DGC_LUT_B63								
RC3h	CABC Control 5	W/R	-	0	PWMDIV[2:0](000)			1	1	INPLUS (1)	1	
RC5h	CABC Control 6	W/R	-	PWM_PERIOD[7:0] (43d)								
RC7h	CABC Control 7	W/R	-	-	DIM_FRAME[6:0] (20)							
RCBh	Gain select register 0	W/R	-	-	DBG0[6:0](40)							
RCCh	Gain select register 1	W/R	-	-	DBG1[6:0](3C)							
RCDh	Gain select register 2	W/R	-	-	DBG2[6:0](38)							

Register No.	Register	W/R	Upper Code	Lower Code								Comment
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
RCEh	Gain select register 3	W/R	-	-	DBG3[6:0](34)							
RCFh	Gain select register 4	W/R	-	-	DBG4[6:0](33)							
RD0h	Gain select register 5	W/R	-	-	DBG5[6:0](32)							
RD1h	Gain select register 6	W/R	-	-	DBG6[6:0](2B)							
RD2h	Gain select register 7	W/R	-	-	DBG7[6:0](24)							
RD3h	Gain select register 8	W/R	-	-	DBG8[6:0](22)							
RFDh	Set SPI Rrad Index	W	-	INDEX[7:0]								
RFEh	Get SPI Index data	R	-	DATA[7:0]								
RFFh	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0] (00)		

Table 8. 2 List Table of Command Set page 1

8.2 Index register

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 8. 1 Index Register

Index register (IR) specifies the Index of register from R00h to RFFh. It sets the register number (ID7-0) in the range from 00000000b to 11111111b in binary form.

8.3 Display mode control register (PAGE0 - R00h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	1	0	0	0	1	1	1

Figure 8. 2 Himax ID Register (PAGE0 - R00h)

This command is used to read this IC's ID code. The ID code of this IC is 57h.

8.4 Display mode control register (PAGE0 - R01h)

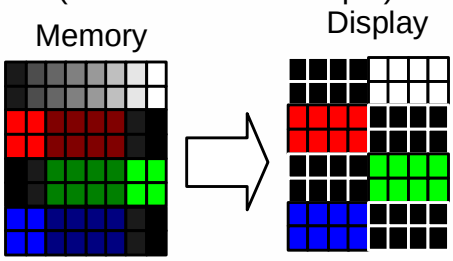
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	DP_STB1	DP_STB0	*	*	SCROL	IDMON	INVON	PLTON
R	1	DP_STB1	DP_STB0	0	0	SCROL	IDMON	INVON	PLTON

Figure 8. 3 Display Mode Control Register (PAGE0 - R01h)

DP_STB[1:0] : When DP_STB[1:0] = '11', the driver into the deep stand_by mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the deep stand_by mode, only the following process can be executed.
a. Exit the Deep Standby mode (DP_STB[1:0] = "00")
b. Start the oscillation
In the Sleep mode, the GRAM data and register content are not retained.

IDMON: This bit is Idle mode (8-color display mode) enable bit. **IDMON** = '1', chip will be into idle mode, and color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

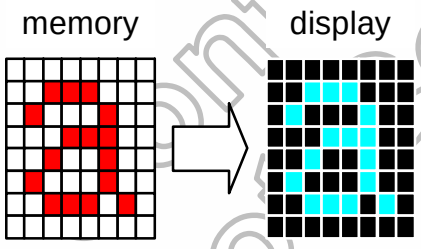
(Idel Mode On Example)



SCROL : This bit turns on scroll mode by setting SCROLL = '1'. The scroll mode window is described by the Vertical Srocll Area command **TFA[15:0], VSA[15:0], BFA[15:0]** and **the Vertical start address VSP[15:0]** (PAGE0 - R0Eh~R15h). To leave scrollmode to normal mode, the **SCROL** bit should be set to '0'.

INVON: This bit is display inversion mode enable bit. **INVON** = '1', chip will be into display inversion mode, and makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.

(Example)



PTLON: This command is used for turning on/off Partial mode by setting PTLON=1/0. The Partial mode window is described by the Partial Area command **PSL[15:0], PEL[15:0]** bits(PAGE0 - R0Ah~R0Dh). To leave Partial mode to normal mode, the **PLTON** bit should be set to '0'.

8.5 Column address start register (PAGE0 - R02~03h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8
R	1	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8

Figure 8. 4 Column Address Start Register Upper Byte (PAGE0 - R02h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
R	1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Figure 8. 5 Column Address Start Register Low Byte (PAGE0 - R03h)

8.6 Column address end register (PAGE0 - R04~05h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8
R	1	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8

Figure 8. 6 Column Address End Register Upper Byte (PAGE0 - R04h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Figure 8. 7 Column Address End Register Low Byte (PAGE0 - R05h)

8.7 Row address start register (PAGE0 - R06~07h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8
R	1	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8

Figure 8. 8 Row Address Start Register Upper Byte (PAGE0 - R06h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
R	1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Figure 8. 9 Row Address Start Register Low Byte (PAGE0 - R07h)

8.8 Row address end register (PAGE0 - R08~09h)

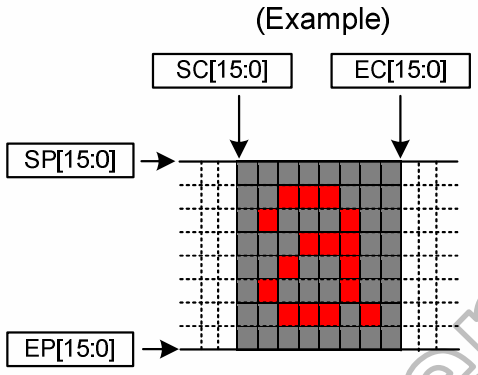
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8
R	1	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8

Figure 8. 10 Row Address End Register Upper Byte (PAGE0 - R08h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
R	1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

Figure 8. 11 Row Address End Register Low Byte (PAGE0 - R09h)

These commands (PAGE0 - R02h~R09h) are used to define area of frame memory where MCU can access. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value of SC[15:0], EC[15:0] represents one column line in the Frame Memory. Each value of SP[15:0], EP[15:0] represents one page line in the Frame Memory.



Note: (1) SC[15:0] must always be equal to or less than EC[15:0]
(2) If SC[15:0] or EC[15:0] is greater then the available frame memory then the GRAM write/read will wrong.
(3) SP[15:0] must always be equal to or less than EP[15:0]
(4) If SP[15:0] or EP[15:0] is greater then the available frame memory then the GRAM write/read will worng.

8.9 Partial area start row register (PAGE0 - R0A~0Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8
R	1	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8

Figure 8. 12 Partial Area Start Row Register Upper Byte (PAGE0 - R0Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0
R	1	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0

Figure 8. 13 Partial Area Start Row Register Low Byte (PAGE0 - R0Bh)

8.10 Partial area end row register (PAGE0 - R0C~0Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8
R	1	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8

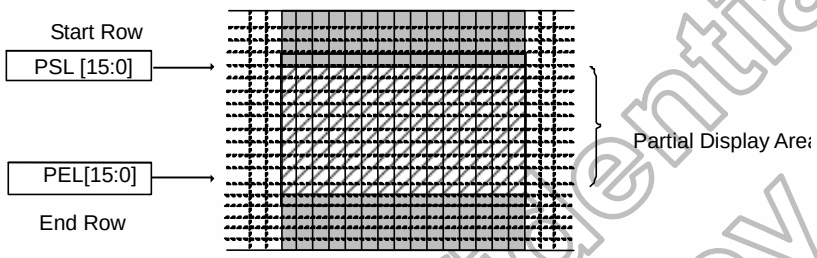
Figure 8. 14 Partial Area End Row Register Upper Byte (PAGE0 - R0Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0
R	1	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0

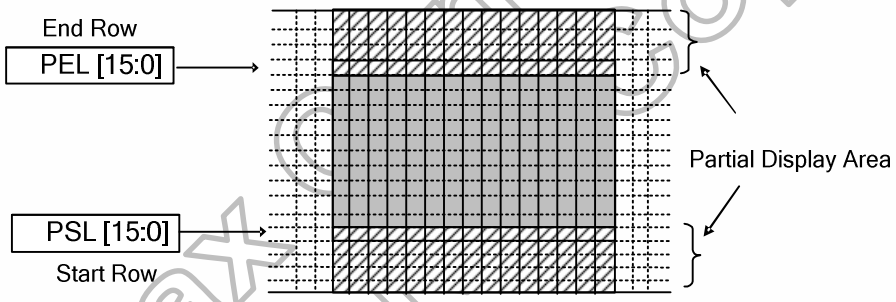
Figure 8. 15 Partial Area End Row Register Low Byte (PAGE0 - R0Dh)

These commands (PAGE0 - R0Ah~~0Dh) define the partial mode's display area. The Start Row (PSL) and the second the End Row (PEL) are illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

If End Row > Start Row



If End Row < Start Row



If End Row = Start Row then the Partial Area will be one row deep.

8.11 Vertical scroll top fixed area register (PAGE0 - R0E~0Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8
R	1	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8

Figure 8. 16 Vertical Scroll Top Fixed Area Register Upper Byte (PAGE0 - R0Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0
R	1	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0

Figure 8. 17 Vertical Scroll Top Fixed Area Register Low Byte (PAGE0 - R0Fh)

8.12 Vertical scroll height area register (PAGE0 - R10~11h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8
R	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8

Figure 8. 18 Vertical Scroll Height Area Register Upper Byte (PAGE0 - R10h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
R	1	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 8. 19 Vertical Scroll Height Area Register Low Byte (PAGE0 - R11h)

8.13 Vertical scroll button fixed area register (PAGE0 - R12~13h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8
R	1	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8

Figure 8. 20 Vertical Scroll Button Fixed Area Register Upper Byte (PAGE0 - R12h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0
R	1	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0

Figure 8. 21 Vertical Scroll Button Fixed Area Register Low Byte (PAGE0 - R13h)

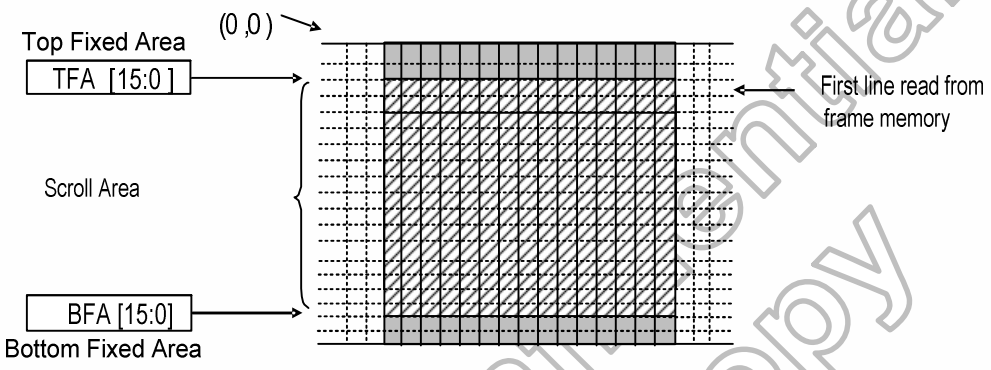
These commands (PAGE0 - R0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display.

TFA[15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Please note that (TFA+VSA+BFA) must be set to '320d'(320RGBx320 dot display mode), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, **MV** bit should be set to '0' – this only affects the Frame Memory Write.

8.14 Vertical scroll start address register (PAGE0 - R14~15h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8
R	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8

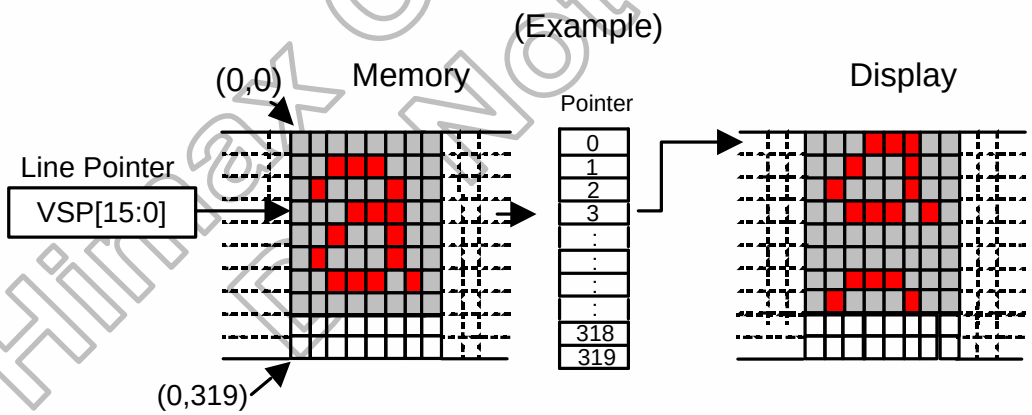
Figure 8. 22 Vertical Scroll Start Address Register Upper Byte (PAGE0 - R14h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0
R	1	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0

Figure 8. 23 Vertical Scroll Start Address Register Low Byte (PAGE0 - R15h)

VSP[15:0] is used together with Vertical Scrolling Definition register (PAGE0 - R0Eh~R13h), which describe the scrolling area and the scrolling mode.
VSP[15:0] refers to the Frame Memory line Pointer, and describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

Example:
When Top Fixed Area TFA = '00d', Bottom Fixed Area BFA = '02'd, Vertical Scrolling Area VSA = '318'd' and VSP = '3d' (**SS** = '0', **GS** = '0')



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

.

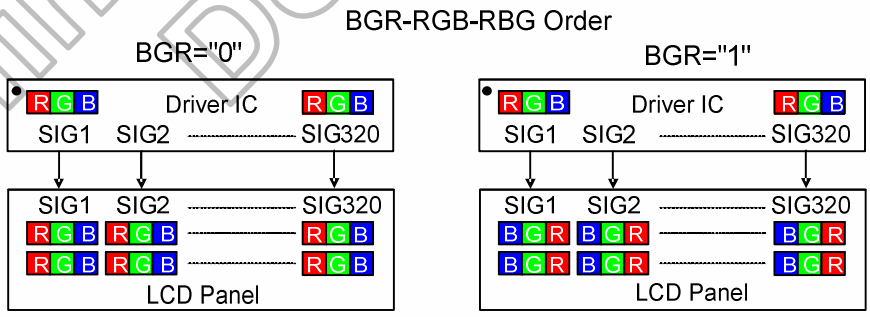
8.15 Memory access control register (PAGE0 - R16h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	MY	MX	MV	*	BGR	*	SS	GS
R	1	MY	MX	MV	0	BGR	0	SS	GS

Figure 8. 24 Memory Access Control Register (PAGE0 - R16h)

This command defines read/write scanning direction of frame memory. **MX, MY** bits also define the display direction in the RGB interface. This command makes no change on the other driver status. For details, please refer to “6.2.1 System interface to GRAM Write Direction” section.

Bit	Name	Description
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write/read direction. “MCU to memory write/read direction”
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel) Note : HW pin SRGB=0, BGR color filter SRGB=1, RGB color filter
SS	SOURCE OUTPUT ORDER	The source driver output shift direction selected. When SS = 0, the shift direction don’t reverse(S1 -> S960). When SS = 1, the shift direction will be reversed(S960 -> S1).
GS	GATE OUTPUT ORDER	The gate driver output shift direction selected. When GS = 0, the shift direction don’t reverse(G1 -> G480). When GS = 1, the shift direction will be reversed(G480 -> G1).



8.16 COLMOD control register (PAGE0 - R17h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CSEL3 (0)	CSEL2 (1)	CSEL1 (1)	CSEL0 (0)	*	IFPF2 (1)	IFPF1 (1)	IFPF0 (0)
R	1	CSEL3 (0)	CSEL2 (1)	CSEL1 (1)	CSEL0 (0)	*	IFPF2 (1)	IFPF1 (1)	IFPF0 (0)

Figure 8. 25 COLMOD Control Register (PAGE0 - R17h)

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

System interface

Interface Format	IFPF2	IFPF1	IFPF0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
18 Bit/Pixel at 16-bits data bus interface (16+2)	1	1	1

RGB interface

Interface Format	CSEL3	CSEL2	CSEL1	CSEL0
16 Bit/Pixel	0	1	0	1
18 Bit/Pixel	0	1	1	0
6 Bit/Pixel	1	1	1	0
Not Defined	The Other Setting			

8.17 OSC control register (PAGE0 - R18h & R19h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I/P_RADJ2	IP_RADJ1	I/P_RADJ0	*	N/P_RADJ2	N/P_RADJ1	N/P_RADJ0
R	1	0	I/P_RADJ2	IP_RADJ1	I/P_RADJ0	0	N/P_RADJ2	N/P_RADJ1	N/P_RADJ0

Figure 8. 26 OSC Control 1 Register (PAGE0 - R18h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	OSC_EN
R	1	0	0	0	0	0	0	0	OSC_EN

Figure 8. 27 OSC Control 2 Register (PAGE0 - R19h)

These commands are used to set internal oscillator related setting

OSC_EN: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop. In RGB interface mode (RCM[1:0] = '10' or '11'), internal oscillator will be stop to oscillate and OSC_EN bit control is invalid.

N/P_RADJ[2:0]: Internal oscillator frequency adjusts in Normal / Partial mode.
I/PI_RADJ[2:0]: Internal oscillator frequency adjusts in Idle(8-color) / Partial Idle mode.
For details, please refer to "7.1 Internal Oscillator" section.

RADJ2	RADJ1	RADJ0	Internal Oscillator Frequency
0	0	0	182%
0	0	1	163%
0	1	0	147%
0	1	1	135%
1	0	0	124%
1	0	1	115%
1	1	0	107%
1	1	1	100%

Figure 8. 28 Power Control 8 Register

8.18 Power control 1 register (PAGE0 - R1Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	BT3	BT2	BT1	BT0
R	1	*	*	*	*	BT3	BT2	BT0	BT0

Figure 8. 29 Power Control 1 Register (PAGE0 - R1Ah)

BT[3:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT3	BT2	BT1	BT0	DDVDH	VCL	VGH	VGL
0	0	0	0	5V	-VCI	3DDVDH	-VCI-2DDVDH
0	0	0	1	5V	-VCI	3DDVDH	-2DDVDH
0	0	1	0	5V	-VCI	3DDVDH	VCI-2DDVDH
0	0	1	1	5V	-VCI	VCI+2DDVDH	-VCI-2DDVDH
0	1	0	0	5V	-VCI	VCI+2DDVDH	-2DDVDH
0	1	0	1	5V	-VCI	VCI+2DDVDH	VCI-2DDVDH
0	1	1	0	5V	-VCI	2DDVDH	-2DDVDH
0	1	1	1	5V	-VCI	2DDVDH	-VCI-DDVDH

Note: When VCI = 2.8V

8.19 Power control 2 register (PAGE0 - R1Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
R	1	*	*	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 8. 30 Power Control 2 Register (PAGE0 - R1Bh)

VRH[5:0]: Specify the VREG1 voltage adjusting. VREG1 voltage is for gamma voltage setting.VREG1=Decimal(VRH[5:0])x0.05+3.3.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VREG1 (TRI_VDH=0)	VREG1 (TRI_VDH=1)
0	0	0	0	0	0	3.30	3.30
0	0	0	0	0	1	3.35	3.35
0	0	0	0	1	0	3.40	3.40
0	0	0	0	1	1	3.45	3.45
0	0	0	1	0	0	3.50	3.50
0	0	0	1	0	1	3.55	3.55
0	0	0	1	1	0	3.60	3.60
0	0	0	1	1	1	3.65	3.65
0	0	1	0	0	0	3.70	3.70
:	:	:	:	:	:	:	:
0	1	1	1	1	0	4.80	4.80
0	1	1	1	1	1	4.80	4.85
1	0	0	0	0	0	4.80	4.90
1	0	0	0	0	1	4.80	4.95
1	0	0	0	1	0	:	:
:	:	:	:	:	:	:	:
1	0	1	0	1	0	4.80	5.40
1	0	1	0	1	1	4.80	5.45
1	0	1	1	0	0	Inhibited	Inhibited
:	:	:	:	:	:	:	:
1	1	1	0	1	1	Inhibited	Inhibited
1	1	1	1	0	1	Inhibited	Inhibited
1	1	1	1	1	0	Inhibited	Inhibited
1	1	1	1	1	1	Internal circuit operations stop. The gamma voltage can be adjusted from external VREG1 input.	

8.20 Power control 3 register (PAGE0 - R1Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	AP2	AP1	AP0
R	1	*	*	*	*	*	AP2	AP1	AP0

Figure 8. 31 Power Control 3 Register (PAGE0 - R1Ch)

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Small
0	1	0	Medium Low
0	1	1	Medium
1	0	0	Medium High
1	0	1	Large
1	1	0	Setting Inhibited
1	1	1	Setting Inhibited

8.21 Power control 4 register (PAGE0 - R1Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I/P_FS02	I/P_FS01	I/P_FS00	*	N/P_FS02	N/P_FS01	N/P_FS00
R	1	*	I/P_FS02	I/P_FS01	I/P_FS00	*	N/P_FS02	N/P_FS01	N/P_FS00

Figure 8. 32 Power Control 4 Register (PAGE0 - R1Dh)

N/P_FS0[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Normal / Partial mode.

I/P_FS0[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Idle(8-color) / Partial Idle mode.
For details, please refer to “7.1 Internal Oscillator” section.

FS02	FS01	FS00	Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

8.22 Power control 5 register (PAGE0 - R1Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I/P_FS12	I/P_FS11	I/P_FS10	*	N/P_FS12	N/P_FS11	N/P_FS10
R	1	*	I/P_FS12	I/P_FS11	I/P_FS10	*	N/P_FS12	N/P_FS11	N/P_FS10

Figure 8. 33 Power Control 5 Register (PAGE0 - R1Eh)

N/P_FS1[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Normal / Partial mode.

I/P_FS1[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Idle(8-color) / Partial Idle mode.
For details, please refer to “7.1 Internal Oscillator” section.

FS12	FS11	FS10	Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3
0	0	0	¼ x H Line Frequency
0	0	1	½ x H Line Frequency
0	1	0	1 x H Line Frequency
0	1	1	1.5 x H Line Frequency
1	0	0	2 x H Line Frequency
1	0	1	3 x H Line Frequency
1	1	0	4 x H Line Frequency
1	1	1	8 x H Line Frequency

Note: Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2

8.23 Power control 6 register (PAGE0 - R1Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GASEN	VCOMG	*	PON	DK	XDK	DDVDH_TRI	STB
R	1	GASEN	VCOMG	*	PON	DK	XDK	DDVDH_TRI	STB

Figure 8. 34 Power Control 6 Register (PAGE0 - R1Fh)

GASEN: This stands for abnormal power-off supervisal function when the power is off. It’s for monitoring power status by NISD pad when GASEN is set to 1.

VCOMG: When **VCOMG** = ‘1’, VCOML voltage can output to negative voltage (1.0V ~ VCL+0.5V). When VCOMG = ‘0’, VCOML outputs GND and **VML[7:0]** setting are invalid. Then, low power consumption is accomplished.

PON: Specify on/off control of step-up circuit 2 for VCL, VGL voltage generation.
For detail, see the Power On/Off Setting Flow.

PON	Operation of step-up circuit 2
0	OFF
1	ON

DK: Specify on/off control of step-up circuit 1 for DDVDH voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

STB: When **STB** = '1', the HX8357-A into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed. For details, please refer to STB mode flow.

a. Start the oscillation
b. Exit the Standby mode (STB = "0") ,

In the standby mode, the GRAM data and register content are retained.

XDK, DDVDH_TRI: Specify the ratio of step-up circuit for DDVDH voltage generation.

DDVDH_TRI	XDK	Step up circuit 1	Capacitor connection pins used
0	0	2 x VCI	C11A, C11B
0	1	2 x VCI	C11A, C11B, CX11A, CX11B
1	0	3 x VCI	C11A, C11B, CX11A, CX11B
1	1	Setting inhabited	Setting inhabited

8.24 Read data register (PAGE0 - R22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
R	1	RD 17	RD 16	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 8. 35 Read Data Register (PAGE0 - R22h)

WD[17:0] : Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

RD[17:0]: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal.

8.25 VCOM control 1~3 register (PAGE0 - R23~25h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VMF 7	VMF 6	VMF 5	VMF 4	VMF 3	VMF 2	VMF 1	VMF 0
R	1	VMF 7	VMF 6	VMF 5	VMF 4	VMF 3	VMF 2	VMF 1	VMF 0

Figure 8. 36 Vcom Control 1 Register (PAGE0 - R23h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VMH 7	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0
R	1	VMH 7	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0

Figure 8. 37 Vcom Control 2 Register (PAGE0 - R24h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VML 7	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0
R	1	VML 7	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0

Figure 8. 38 Vcom Control 3 Register (PAGE0 - R25h)

This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage

VMH[7:0]: Set the VCOMH voltage (High level voltage of VCOM). VCOM High voltage = Decimal(VMH[7:0])x0.015+2.5. The default value is 1Ch(28x0.025+2.5=3.2V)

VMH 7	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	VCOMH (DDVD_TRI_=0)	VCOMH (DDVDH_TRI=1)
0	0	0	0	0	0	0	0	2.500	2.500
0	0	0	0	0	0	0	1	2.515	2.515
0	0	0	0	0	0	1	0	2.530	2.530
0	0	0	0	0	0	1	1	2.545	2.545
0	0	0	0	0	1	0	0	2.560	2.560
0	0	0	0	0	1	0	1	2.575	2.575
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
1	0	0	1	0	0	1	1	4.705	4.705
1	0	0	1	0	1	0	0	4.720	4.720
1	0	0	1	0	1	0	1	4.735	4.735
1	0	0	1	0	1	1	0	4.750	4.750
1	0	0	1	0	1	1	1	4.765	4.765
1	0	0	1	1	0	0	0	4.780	4.780
1	0	0	1	1	0	0	1	4.795	4.795
1	0	0	1	1	0	1	0	4.810	4.810
1	0	0	1	1	0	1	1	4.825	4.825
1	0	0	1	1	1	0	0	4.825	4.840
1	0	0	1	1	1	0	1	4.825	4.855
:	:	:	:	:	:	:	:	4.825	:
1	1	0	0	1	0	0	0	4.825	5.500
:	:	:	:	:	:	:	:	4.825	:

VMH 7	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	VCOMH (DDVD_TRI_=0)	VCOMH (DDVDH_TRI=1)
1	1	1	1	1	1	1	0	4.825	5.500
1	1	1	1	1	1	1	1	Setting inhibited	

VML[7:0]: Set the VCOML voltage (Low level voltage of VCOM). VCOM Low voltage = Decimal(VML[7:0])x0.015-2.5. The default value is 34h(52x0.025-2.5=-1.2V)

VML7	VML6	VML5	VML4	VML3	VML2	VML1	VML0	VCOML
0	0	0	0	0	0	0	0	-2.500
0	0	0	0	0	0	0	1	-2.485
0	0	0	0	0	0	1	0	-2.470
0	0	0	0	0	1	0	1	-2.455
:	:	:	:	:	:	:	:	:
1	0	1	0	0	0	1	1	-0.055
1	0	1	0	0	1	0	0	-0.040
1	0	1	0	0	1	0	1	-0.025
1	0	1	0	0	1	1	0	-0.010
1	0	1	0	0	1	1	1	Setting inhibit
	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	Setting inhibit

VMF[7:0]: Set the VCOM offset voltage. VMH+1d/VML+1d means VMH/VML from original setting move up one step (15mV). VMH-1d/VML-1d means VMH/VML from original setting move down one step (15mV)

VMF[7:0]	VCOMH	VCOML
0	"VMH" – 128d	"VML" – 128d
1	"VMH" – 127d	"VML" – 127d
2	"VMH" – 126d	"VML" – 126d
3	"VMH" – 125d	"VML" – 125d
:	:	:
126	"VMH" – 2d	"VML" – 2d
127	"VMH" – 1d	"VML" – 1d
128	"VMH"	"VML"
129	"VMH" + 1d	"VML" + 1d
130	"VMH" + 2d	"VML" + 2d
:	:	:
254	"VMH" + 126d	"VML" + 126d
255	"VMH" + 127d	"VML" + 127d

Note: 1. 0d < (VMF+VMH) < 255d.
2. 0d< (VMF+VML) < 255d.

8.26 Display control 1~3 register (PAGE0 - R26h~R28h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	I/P_ISC3	I/P_ISC2	I/P_ISC1	I/P_ISC0	N/P_ISC3	N/P_ISC2	N/P_ISC1	N/P_ISC0
R	1	I/P_ISC3	I/P_ISC2	I/P_ISC1	I/P_ISC0	N/P_ISC3	N/P_ISC2	N/P_ISC1	N/P_ISC0

Figure 8. 39 Display Control 1 Register (PAGE0 - R26h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PT1	PT0	PTV1	PTV0	*	*	PTG	REF
R	1	PT1	PT0	PTV1	PTV0	*	*	PTG	REF

Figure 8. 40 Display Control 2 Register (PAGE0 - R27h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	GON	DTE	D1	D0	*	*
R	1	*	*	GON	DTE	D1	D0	0	0

Figure 8. 41 Display Control 3 Register (PAGE0 - R28h)

N/P_ISC[3:0]: Specify the scan cycle of gate driver when **REF** = '1' in non-display area for Nornal/ Partial mode. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

I/P_ISC[3:0]: Specify the scan cycle of gate driver when **REF** = '1' in non-display area for Idle (8-color) / Partial Idle mode. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	3 frames	50ms
0	0	1	0	5 frames	83ms
0	0	1	1	7 frames	117ms
0	1	0	0	9 frames	150ms
0	1	0	1	11 frames	183ms
0	1	1	0	13 frames	217ms
0	1	1	1	15 frames	250ms
1	0	0	0	17 frames	283ms
1	0	0	1	19 frames	317ms
1	0	1	0	21 frames	350ms
1	0	1	1	23 frames	383ms
1	1	0	0	25 frames	417ms
1	1	0	1	27 frames	450ms
1	1	1	0	29 frames	483ms
1	1	1	1	31 frames	517ms

REF: Refresh display in non-display area in Partial mode enable bit.
REF = '0': Refresh display operation is disabling.
REF = '1': Refresh display operation is enable.

PTG: Specify the scan mode of gate driver in non-display area.

PTG	Gate Outputs in Non-display Area
0	Normal Drive
1	Fixed VGL

PTV[1:0]: Specify the scan mode of VCOM in non-display area.

PTV1	PTV0	VCOM Outputs in Non-display Area
0	0	Normal Drive
0	1	Fixed to VCOML
1	0	Fixed to GND
1	1	Setting Inhibited

PT[1:0] : Specify the Non-display area source output in partial display mode.

INVON	GRAM Data	Source Output Level							
		Display area		Non-display Area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
1	18'h00000 . . 18'h3FFFF	V63P . . V0P	V0N . . V63N	V63P	V0N	VSSD	VSSD	Hi-z	Hi-z
0	18'h00000 . . 18'h3FFFF	V0P . . V63P	V63N . . V0N	V63P	V0N	VSSD	VSSD	Hi-z	Hi-z

D[1:0]: When D1='1', display is on; when D1='0', display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = '1'. When D1='0', the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8357-A can control the charging current for the LCD with AC driving. Control the display on/off while control GON and DTE.
When D[1:0]= '01', the internal display of the HX8357-A is performed although the actual display is off. When D[1:0]= '00', the internal display operation halts and the display is off.

D1	D0	Source Output	HX8357-A Internal Display Operations	Gate-Driver Control Signals
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	=PT(0,0)	Operate	Operate
1	1	Display	Operate	Operate

GON, DTE:

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

PT1	PT0	REF	ISC[3:0]	Source Output	VCOM Output	Gate Output
0	x	x	--	Black Display (INVON = '1') White Display (INVON = '0')	Normal Driving	Normal Driving
1	0	0	--	GND	PTV[1:0]	PTG
		1	Non-refresh cycle	GND	PTV[1:0]	PTG
			Refresh cycle	Black Display (INVON = '1') White Display (INVON = '0')	Normal Driving	Normal Driving
1	1	0	--	Hi-z	PTV[1:0]	PTG
		1	Non-refresh cycle	Hi-z	PTV[1:0]	PTG
			Refresh cycle	Black Display (INVON = '1') White Display (INVON = '0')	Normal Driving	Normal Driving

8.27 Frame control 1~4 register (PAGE0 - R29h~R2Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	I/P_RTN3	I/P_RTN2	I/P_RTN1	I/P_RTN0	N/P_RTN3	N/P_RTN2	N/P_RTN1	N/P_RTN0
R	1	I/P_RTN3	I/P_RTN2	I/P_RTN1	I/P_RTN0	N/P_RTN3	N/P_RTN_2	N/P_RTN1	N/P_RTN0

Figure 8. 42 Frame Control 1 Register (PAGE0 - R29h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	I/P_DIV1	I/P_DIV0	*	*	N/P_DIV1	N/P_DIV0
R	1	*	*	I/P_DIV1	I/P_DIV0	*	*	N/P_DIV1	N/P_DIV0

Figure 8. 43 Frame Control 2 Register (PAGE0 - R2Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	N/P_DUM7	N/P_DUM6	N/P_DUM5	N/P_DUM4	N/P_DUM3	N/P_DUM2	N/P_DUM1	N/P_DUM0
R	1	N/P_DUM7	N/P_DUM6	N/P_DUM5	N/P_DUM4	N/P_DUM3	N/P_DUM2	N/P_DUM1	N/P_DUM0

Figure 8. 44 Frame Control 3 Register (PAGE0 - R2Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	I/P_DUM7	I/P_DUM6	I/P_DUM5	I/P_DUM4	I/P_DUM3	I/P_DUM2	I/P_DUM1	I/P_DUM0
R	1	I/P_DUM7	I/P_DUM6	I/P_DUM5	I/P_DUM4	I/P_DUM3	I/P_DUM2	I/P_DUM1	I/P_DUM0

Figure 8. 45 Frame Control 4 Register (PAGE0 - R2Ch)

N/P_DIV[1:0]: Specify the division ratio of internal clocks in Normal / Partial mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **N/P_RTN[3:0]** bits (1H period clock cycle), **N/P_DIV[1:0**], and **N/P_DUM[7:0]** bits.

I/P_DIV[1:0]: Specify the division ratio of internal clocks in Idle (8-color) / Partial Idle mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the **I/P_RTN[3:0]** bits(1H period clock cycle), **I/P_DIV[1:0**], and **I/P_DUM[7:0]** bits.

fosc = R-C oscillation frequency

DIV1	DIV0	Division Ratio	Internal Display Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

N/P_RTN[3:0]: Specify clock number of one line period in Normal / Partial mode for internal operation.

I/P_ RTN[3:0]: Specify clock number of one line period in Idle (8-color) / Partial Idle mode for internal operation.

Clock cycles=1/internal operation clock frequency(fosc)

RTN[3:0]	Clock number per Line
4'b0000	168
4'b0001	169
4'b0010	170
4'b0011	171
4'b0100	172
:	:
4'b1110	182
4'b1111	182

N/P_DUM[7:0]: Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.

I/P_DUM[7:0]: Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

DUM[7:0]	Line number in blanking period
000d	Setting Inhibited
001d	2
002d	4
003d	6
004d	8
:	:
190d	380
others	Setting Inhibited

Formula for the Frame Frequency during internal display mode:
Frame frequency = fosc/(RTN × DIV × (480+DUM)) [Hz]
fosc: RC oscillation frequency

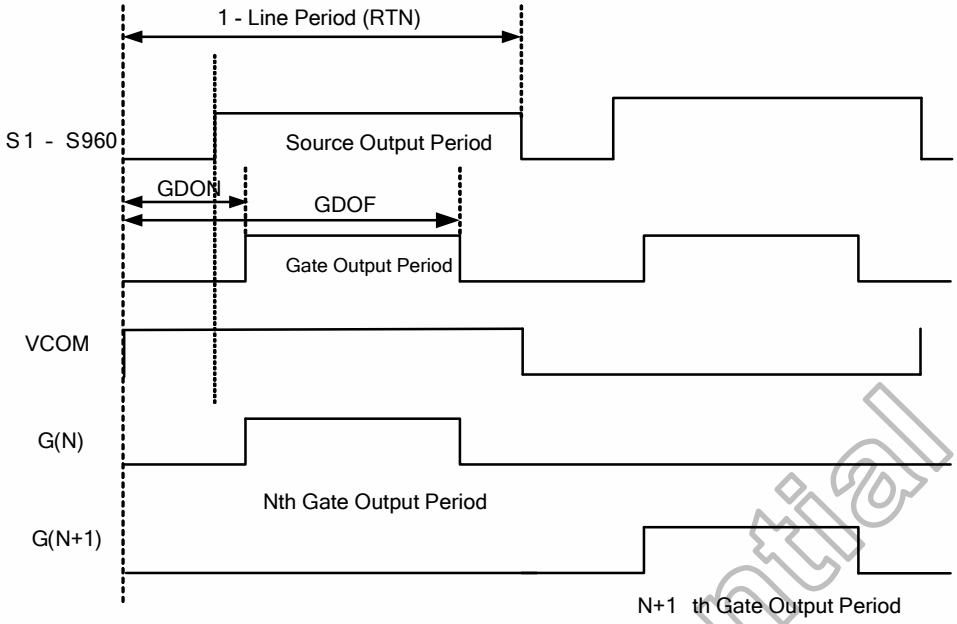
8.28 Cycle control 1~2 Register (PAGE0 - R2Dh~R2Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GDON7	GDON6	GDON5	GDON4	GDON3	GDON2	GDON1	GDON0
R	1	GDON7	GDON6	GDON5	GDON4	GDON3	GDON2	GDON1	GDON0

Figure 8. 46 Cycle Control 1 Register (PAGE0 - R2Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GDOF7	GDOF6	GDOF5	GDOF4	GDOF3	GDOF2	GDOF1	GDOF0
R	1	GDOF7	GDOF6	GDOF5	GDOF4	GDOF3	GDOF2	GDOF1	GDOF0

Figure 8. 47 Cycle Control 2 Register (PAGE0 - R2Eh)



GDON[7:0]: Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting "00h", "01h", "02h" is inhibited)**.**

GDOF[7:0]: Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the GDON[7:0] + 1≤ GDOF[7:0] ≤ RTN-1).

8.29 Display Inversion Register (PAGE0 - R2Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	I/P_ NW2	I/P_ NW1	I/P_ NW0	*	N/P_ NW2	N/P_ NW1	N/P_ NW0
R	1	*	I/P_ NW2	I/P_ NW1	I/P_ NW0	*	N/P_ NW2	N/P_ NW1	N/P_ NW0

Figure 8. 48 Display Inversion Control Register (PAGE0 - R2Fh)

N/P_ NW[2:0]: Specify LCD driving inversion type in Normal/ Partial mode.
I/P_ NW[2:0]: Specify LCD driving inversion type in Idle / Partial Idle mode.

NW[2:0]	LCD driving Inversion Type
0d	Frame inversion
1d	1-line inversion
2d	2-line inversion
3d	3-line inversion
:	:
6d	6-line inversion
7d	7-line inversion

8.30 RGB interface control 1~4 register (PAGE0 - R31h~R34h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	RCM 1	RCM 0
R	1	0	0	0	0	0	0	RCM 1	RCM 0

Figure 8. 49 RGB Interface Control 1 Register (PAGE0 - R31h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	DPL	HSPL	VSPL	EPL
R	1	0	0	0	*	DPL	HSPL	VSPL	EPL

Figure 8. 50 RGB Interface Control 2 Register (PAGE0 - R32h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
R	1	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

Figure 8. 51 RGB Interface Control 3 Register (PAGE0 - R33h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HBP9	HBP8	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R	1	HBP9	HBP8	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 8. 52 RGB Interface Control 4 Register (PAGE0 - R34h)

This command is used to set RGB interface related register

RCM[1:0]: RGB and MCU interface select.

RCM1	RCM0	Interface Select
0	x	System Interface(1)
1	0	RGB Interface(1) (VS+HS+DE)
1	1	RGB Interface(2) (VS+HS)

Note: (1) As RCM[1:0] bit be written, the external pin RCM[1:0] control is invalid.

EPL: Specify the polarity of DE signal in RGB interface mode. EPL='1', the DE signal is Low active; EPL=0, the DE signal is High active.

VSPL: The polarity of VSYNC pin. When VSPL='0', the VSYNC signal is Low active. When VSPL=1, the VSYNC signal is High active.

HSPL: The polarity of HSYNC pin. When HSPL='0', the HSYNC signal is Low active. When HSPL=1, the HSYNC signal is High active.

DPL: The polarity of PCLK pin. When DPL='0', the data is latched by the chip on the rising edge of PCLK signal. When DPL='1', the data is latched by the chip on the falling edge of PCLK signal.

HBP and **VBP** are used to set vertical and horizontal back porch control in RGB I/F mode 2 (RCM[1:0]= '11') (RGB I/F mode 1 is using DE signal as data enable signal)

HBP[9:0]: Set the delay period from falling edge of HSYNC signal to first valid data in RGB I/F mode 2

HBP[9:0]	No. of clock cycle of DOTCLK	
	CSEL="0101" or "0110"	CSEL="1110"
00d	Setting Inhibited	Setting Inhibited
01d	Setting Inhibited	Setting Inhibited
02d	2	6
03d	3	9
04d	4	12
:	:	:
1021d	1021	3063
1022d	1022	3066
1023d	Setting Inhibited	Setting Inhibited

VBP[5:0]: Set the delay period from falling edge of VSYNC signal to first valid line in RGB I/F mode 2

VBP[5:0]	No. of clock cycle of HSYNC
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
61d	61
62d	62
63d	63

8.31 Panel characteric control register (PAGE0 - R36h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL
R	1	*	*	*	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL

Figure 8. 53 RGB Interface Control Register (PAGE0 - R36h)

This command is internal use for display panel setting. As this command be written, the external pin SRGB, SMX and SMY hardware control pins are invalid.

SM_PANEL: Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin.

SS_PANEL: The source driver output shift direction selected. When SS_PANEL = 0, the shift direction don't reverse. When SS_PANEL = 1, the shift direction will be reversed.

GS_PANEL: The gate driver output shift direction selected. When GS_PANEL = 0, the shift direction don't reverse. When GS_PANEL = 1, the shift direction will be reversed.

REV_PANEL: The source output data ploarity selected. When REV_PANEL = 0, normally white panel is selected. When REV_PANEL = 1, normally black panel is selected.

BGR_PANEL: The color filter order direction selected. When BGR_PANEL = 0, don't reverse the SRGB setting. When BGR_PANEL = 1, the color filter order will be reversed.

8.32 OTP contril 1~4 register (PAGE0 - R38h ~ R3Bh)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_MASK7	OTP_MASK6	OTP_MASK5	OTP_MASK4	OTP_MASK3	OTP_MASK2	OTP_MASK1	OTP_MASK0
R	1	OTP_MASK7	OTP_MASK6	OTP_MASK5	OTP_MASK4	OTP_MASK3	OTP_MASK2	OTP_MASK1	OTP_MASK0

Figure 8. 54 OTP Control 1 Register (PAGE0 - R38h)

R/W	RS	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_IND EX7	OTP_IND EX6	OTP_IND EX5	OTP_IND EX4	OTP_IND EX3	OTP_IND EX2	OTP_IND EX1	OTP_IND EX0
R	1	OTP_IND EX7	OTP_IND EX6	OTP_IND EX5	OTP_IND EX4	OTP_IND EX3	OTP_IND EX2	OTP_IND EX1	OTP_IND EX0

Figure 8. 55 OTP Control 2 Register (PAGE0 - R39h)

R/W	RS	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM1	OTP_PTM0	VPP_SEL	OTP_PROG
R	1	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM1	OTP_PTM0	VPP_SEL	OTP_PROG

Figure 8. 56 OTP Control 3 Register (PAGE0 - R3Ah)

R/W	RS	D7	D6	D5	D4	D3	D2	D1	D0
R	1	OTP_DATA 7	OTP_DATA 6	OTP_DATA 5	OTP_DATA 4	OTP_DATA 3	OTP_DAT A2	OTP_DATA 1	OTP_DATA 0

Figure 8. 57 OTP Control 4 Register (PAGE0 - R3Bh)

This command is used to set the OTP related setting. Please see OTP flow for detail use.

OTP_MASK[7:0]: Bit programming mask, if 1, means don't programming this bit

OTP_INDEX[7:0]: Set location of OTP to be programmed

OTP_LOAD_DISABLE: When written to 1, auto load from OTP to internal register is disabled, this is used when OTP is not yet programmed

OTP_TEST: Internal use, not open. Please set "0".

OTP_POR: OTP read control bit.

OTP_PWE: Internal use, not open. Please set "0".

OTP_PTM[1:0]: Internal use, not open. Please set "00".

VPP_SEL: When written to 1, VPP voltage is fed to OTP

OTP_PROG: When written to 1, internal register begin written to OTP

OTP_DATA[7:0]: OTP data of read OTP index.

For details, please refer to 10. OTP Programming.

8.33 CABC control 1~4 register (PAGE0 - R3Ch~3Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	DBV 7	DBV 6	DBV 5	DBV 4	DBV 3	DBV 2	DBV 1	DBV 0
R	1	DBV 7	DBV 6	DBV 5	DBV 4	DBV 3	DBV 2	DBV 1	DBV 0

Figure 8. 58 CABC Control 1 Register (PAGE0 - R3Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	BCTRL	*	DD	BL	*	*
R	1	0	0	BCTRL	0	DD	BL	0	0

Figure 8. 59 CABC Control 2 Register (PAGE0 - R3Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	CABC 1	CABC 0
R	1	0	0	0	0	0	0	CABC 1	CABC 0

Figure 8. 60 CABC Control 3 Register (PAGE0 - R3Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CMB 7	CMB 6	CMB 5	CMB 4	CMB 3	CMB 2	CMB 1	CMB 0
R	1	CMB 7	CMB 6	CMB 5	CMB 4	CMB 3	CMB 2	CMB 1	CMB 0

Figure 8. 61 CABC Control 4 Register (PAGE0 - R3Fh)

These commands are used to set CABC parameter

DBV[7:0]: The backlight PWM pulse output duty is equal to (DBV[7:0]+1)/256 x CABC_duty.

BCTRL: Backlight Control Block On/Off, This bit is always used to switch brightness for display.

'0' = Off (Equal to DBV[7:0] = '00h')

'1' = On (Brightness registers are active.)

DD: Display Dimming (Only for manual brightness setting)

'0': Display Dimming is off.

'1': Display Dimming is on.

BL: Backlight Control On/Off
'0' = Off (Completely turn off backlight circuit. Control lines must be low.)
'1' = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (**DD=1**) are selected.

CABC[1:0]: This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC1	CABC0	Function	Note
0	0	Off	-
0	1	User Interface Image	-
1	0	Still Picture	-
1	1	Moving Image	-

CMB[7:0]: This command is used to set the minimum brightness value of the display for CABC function.
In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

8.34 Gamma control 1~35 register (PAGE0 - R40h~5Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 05	VRP 04	VRP 03	VRP 02	VRP 01	VRP 00
R	1	0	0	VRP 05	VRP 04	VRP 03	VRP 02	VRP 01	VRP 00

Figure 8. 62 Gamma Control 1 Register (PAGE0 - R40h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 15	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10
R	1	0	0	VRP 15	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10

Figure 8. 63 Gamma Control 2 Register (PAGE0 - R41h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 25	VRP 24	VRP 23	VRP 22	VRP 21	VRP 20
R	1	0	0	VRP 25	VRP 24	VRP 23	VRP 22	VRP 21	VRP 20

Figure 8. 64 Gamma Control 3 Register (PAGE0 - R42h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 35	VRP 34	VRP 33	VRP 32	VRP 31	VRP 30
R	1	0	0	VRP 35	VRP 34	VRP 33	VRP 32	VRP 31	VRP 30

Figure 8. 65 Gamma Control 4 Register (PAGE0 - R43h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 45	VRP 44	VRP 43	VRP 42	VRP 41	VRP 40
R	1	0	0	VRP 45	VRP 44	VRP 43	VRP 42	VRP 41	VRP 40

Figure 8. 66 Gamma Control 5 Register (PAGE0 - R44h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRP 55	VRP 54	VRP 53	VRP 52	VRP 51	VRP 50
R	1	0	0	VRP 55	VRP 54	VRP 53	VRP 52	VRP 51	VRP 50

Figure 8. 67 Gamma Control 6 Register (PAGE0 - R45h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRP 06	PRP 05	PRP 04	PRP 03	PRP 02	PRP 01	PRP 00
R	1	0	PRP 06	PRP 05	PRP 04	PRP 03	PRP 02	PRP 01	PRP 00

Figure 8. 68 Gamma Control 7 Register (PAGE0 - R46h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRP 16	PRP 15	PRP 14	PRP 13	PRP 12	PRP 11	PRP 10
R	1	0	PRP 16	PRP 15	PRP 14	PRP 13	PRP 12	PRP 11	PRP 10

Figure 8. 69 Gamma Control 8 Register (PAGE0 - R47h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 04	PKP 03	PKP 02	PKP 01	PKP 00
R	1	0	0	0	PKP 04	PKP 03	PKP 02	PKP 01	PKP 00

Figure 8. 70 Gamma Control 9 Register (PAGE0 - R48h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 14	PKP 13	PKP 12	PKP 11	PKP 10
R	1	0	0	0	PKP 14	PKP 13	PKP 12	PKP 11	PKP 10

Figure 8. 71 Gamma Control 10 Register (PAGE0 - R49h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 24	PKP 23	PKP 22	PKP 21	PKP 20
R	1	0	0	0	PKP 24	PKP 23	PKP 22	PKP 21	PKP 20

Figure 8. 72 Gamma Control 11 Register (PAGE0 - R4Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 34	PKP 33	PKP 32	PKP 31	PKP 30
R	1	0	0	0	PKP 34	PKP 33	PKP 32	PKP 31	PKP 30

Figure 8. 73 Gamma Control 12 Register (PAGE0 - R4Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKP 44	PKP 43	PKP 42	PKP 41	PKP 40
R	1	0	0	0	PKP 44	PKP 43	PKP 42	PKP 41	PKP 40

Figure 8. 74 Gamma Control 13 Register (PAGE0 - R4Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 05	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00
R	1	0	0	VRN 05	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00

Figure 8. 75Gamma Control 17 Register (PAGE0 - R50h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 15	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10
R	1	0	0	VRN 15	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10

Figure 8. 76 Gamma Control 18 Register (PAGE0 - R51h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 25	VRN 24	VRN 23	VRN 22	VRN 21	VRN 20
R	1	0	0	VRN 25	VRN 24	VRN 23	VRN 22	VRN 21	VRN 20

Figure 8. 77 Gamma Control 19 Register (PAGE0 - R52h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 35	VRN 34	VRN 33	VRN 32	VRN 31	VRN 30
R	1	0	0	VRN 35	VRN 34	VRN 33	VRN 32	VRN 31	VRN 30

Figure 8. 78 Gamma Control 20 Register (PAGE0 - R53h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 45	VRN 44	VRN 43	VRN 42	VRN 41	VRN 40
R	1	0	0	VRN 45	VRN 44	VRN 43	VRN 42	VRN 41	VRN 40

Figure 8. 79 Gamma Control 21 Register (PAGE0 - R54h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	VRN 55	VRN 54	VRN 53	VRN 52	VRN 51	VRN 50
R	1	0	0	VRN 55	VRN 54	VRN 53	VRN 52	VRN 51	VRN 50

Figure 8. 80 Gamma Control 22 Register (PAGE0 - R55h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRN 06	PRN 05	PRN 04	PRN 03	PRN 02	PRN 01	PRN 00
R	1	0	PRN 06	PRN 05	PRN 04	PRN 03	PRN 02	PRN 01	PRN 00

Figure 8. 81 Gamma Control 23 Register (PAGE0 - R56h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	PRN 16	PRN 15	PRN 14	PRN 13	PRN 12	PRN 11	PRN 10
R	1	0	PRN 16	PRN 15	PRN 14	PRN 13	PRN 12	PRN 11	PRN 10

Figure 8. 82 Gamma Control 24 Register (PAGE0 - R57h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 04	PKN 03	PKN 02	PKN 01	PKN 00
R	1	0	0	0	PKN 04	PKN 03	PKN 02	PKN 01	PKN 00

Figure 8. 83 amma Control 25 Register (PAGE0 - R58h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 14	PKN 13	PKN 12	PKN 11	PKN 10
R	1	0	0	0	PKN 14	PKN 13	PKN 12	PKN 11	PKN 10

Figure 8. 84 Gamma Control 26 Register (PAGE0 - R59h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 24	PKN 23	PKN 22	PKN 21	PKN 20
R	1	0	0	0	PKN 24	PKN 23	PKN 22	PKN 21	PKN 20

Figure 8. 85 Gamma Control 27 Register (PAGE0 - R5Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 34	PKN 33	PKN 32	PKN 31	PKN 30
R	1	0	0	0	PKN 34	PKN 33	PKN 32	PKN 31	PKN 30

Figure 8. 86 Gamma Control 28 Register (PAGE0 - R5Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PKN 44	PKN 43	PKN 42	PKN 41	PKN 40
R	1	0	0	0	PKN 44	PKN 43	PKN 42	PKN 41	PKN 40

Figure 8. 87 Gamma Control 29 Register (PAGE0 - R5Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CGM N11	CGM N10	CGM N01	CGM N00	CGM P11	CGM P10	CGM P01	CGM P00
R	1	CGM N11	CGM N10	CGM N01	CGM N00	CGM P11	CGM P10	CGM P01	CGM P00

Figure 8. 88 Gamma Control 30 Register (PAGE0 - R5Dh)

VRP5-0[5:0]: Gamma Offset adjustment registers for positive polarity output
VRN5-0[5:0]: Gamma Offset adjustment registers for negative polarity output
PRP1-0[6:0]: Gamma Center adjustment registers for positive polarity output
PRN1-0[6:0]: Gamma Center adjustment registers for negative polarity output
PKP8-0[4:0]: Gamma Macro adjustment registers for positive polarity output
PKN8-0[4:0]: Gamma Macro adjustment registers for negative polarity output
For details, please refer to 7.2 Gamma resister stream and 8 to 1 Selector.

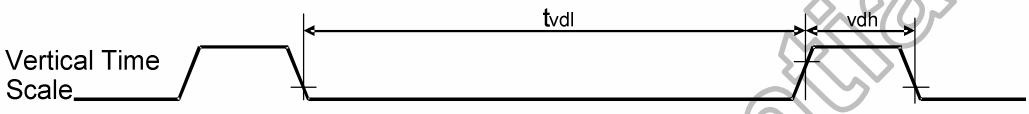
8.35 TE mode control (PAGE0 - R60h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	TEMODE	TEON	*	*	*
R	1	0	0	0	TEMODE	TEON	0	0	0

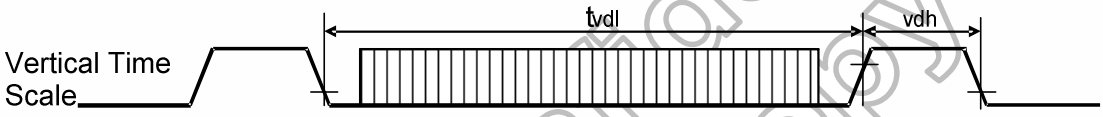
Figure 8. 89 Mode Control Register (PAGE0 - R60h)

TEMODE: Specify the Tearing-Effect mode.

When **TEMODE** = '0': The Tearing Effect Output line (TE) consists of V-Blanking information only.



When **TEMODE** ='1': The Tearing Effect Output Line (TE) consists of both V-Blanking and H-Blanking information



Note: During Stand by Mode with Tearing Effect Line On, Tearing Effect Output pin active low

TEON: This command is used to turn ON the Tearing Effect output signal from the TE signal line.

8.36 ID1~4 registe (PAGE0 - R61h~64h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
R	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

Figure 8. 90 ID1 Register (PAGE0 - R61h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
R	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20

Figure 8. 91 ID3 Register (PAGE0 - R62h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
R	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

Figure 8. 92 ID3 Register (PAGE0 - R63h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
R	1	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40

Figure 8. 93 ID4 Register (PAGE0 - R64h)

ID1~4: User can program any value to OTP for module number.

8.37 MDDI control 4~5 register (PAGE0 - R68h~R69h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VWAKW	WKL8	*	*	WKF3	WKF2	WKF1	WKF0
R	1	VWAKE	WKL8	0	0	WKF3	WKF2	WKF1	WKF0

Figure 8. 94 MDDI Control 4 Register (PAGE0 - R68h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0
R	1	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0

Figure 8. 95 MDDI Control 5 Register (PAGE0 - R69h)

Set a display position at which to start a wakeup request from the client to the host.

WKF[3:0]: When MDDI applies a client start wakeup, frame WKF[3:0] + 1 is used to release a wakeup request. The range you can set is from the first frame to the 16th frame. (Initial value: "0000")

VWAKE: Setting this bit to “1” will enable a client start wakeup. When the host accepts a wakeup request to clear hibernation, this bit is set automatically to “0.” (Initial value: 0)

WKL[8:0]: When MDDI applies a client start wakeup, a wakeup request is released from line WKL[8:0] + 1 of a frame set by WKF[3:0]. The range you can set is from the first line to the 512th line. (Initial value: "0 0000 0000")

When you set WKL to “0 0000 0001” with WKF set to “0010,” a wakeup request will be started at the second line of the third frame

8.38 GPIO control 1~5 register (PAGE0 - R6Bh~R6Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R	1	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

Figure 8. 96 GPIO Control 1 Register (PAGE0 - R6Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO_CON7	GPIO_CON6	GPIO_CON5	GPIO_CON4	GPIO_CON3	GPIO_CON2	GPIO_CON1	GPIO_CON0
R	1	GPIO_CON7	GPIO_CON6	GPIO_CON5	GPIO_CON4	GPIO_CON3	GPIO_CON2	GPIO_CON1	GPIO_CON0

Figure 8. 97 GPIO Control 2 Register (PAGE0 - R6Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO_EN7	GPIO_EN6	GPIO_EN5	GPIO_EN4	GPIO_EN3	GPIO_EN2	GPIO_EN1	GPIO_EN0
R	1	GPIO_EN7	GPIO_EN6	GPIO_EN5	GPIO_EN4	GPIO_EN3	GPIO_EN2	GPIO_EN1	GPIO_EN0

Figure 8. 98 GPIO Control 3 Register (PAGE0 - R6Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO_POL7	GPIO_POL6	GPIO_POL5	GPIO_POL4	GPIO_POL3	GPIO_POL2	GPIO_POL1	GPIO_POL0
R	1	GPIO_POL7	GPIO_POL6	GPIO_POL5	GPIO_POL4	GPIO_POL3	GPIO_POL2	GPIO_POL1	GPIO_POL0

Figure 8. 99 GPIO Control 4 Register (PAGE0 - R6Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GPIO_CLR7	GPIO_CLR6	GPIO_CLR5	GPIO_CLR4	GPIO_CLR3	GPIO_CLR2	GPIO_CLR1	GPIO_CLR0
R	1	GPIO_CLR7	GPIO_CLR6	GPIO_CLR5	GPIO_CLR4	GPIO_CLR3	GPIO_CLR2	GPIO_CLR1	GPIO_CLR0

Figure 8. 100 GPIO Control 5 Register (PAGE0 - R6Fh)

GPIO[7:0]: GPIO value. When GPIO is input mode, GPIO value is set to the register.

GPIO_CON[7:0]: Select GPIO I/O mode.

GPIO_CONx	GPIOx pin
0	INPUT
1	OUTPUT

x:7~0

GPIO_EN[7:0]: When GPIO is set input, if GPIO_EN is “1”, it acts as enable internal interrupt.

GPPOL[7:0]: Interrupt polarity select bit
1: rising edge
0: falling edge

GPIO_CLR[7:0]: Write ’0’, clear interrupt. After Wakeup, this bit is cleared.

For more information about these registers, refer to GPIO CONTROL section

8.39 SUB_PANEL control 1~4 register (PAGE0 - R70h~R73h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SUB_WR15	SUB_WR14	SUB_WR13	SUB_WR12	SUB_WR11	SUB_WR10	SUB_WR9	SUB_WR8
R	1	SUB_WR15	SUB_WR14	SUB_WR13	SUB_WR12	SUB_WR11	SUB_WR10	SUB_WR9	SUB_WR8

Figure 8. 101 SUB_PANEL Control 1 Register (PAGE0 - R70h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SUB_WR7	SUB_WR6	SUB_WR5	SUB_WR4	SUB_WR3	SUB_WR2	SUB_WR1	SUB_WR0
R	1	SUB_WR7	SUB_WR6	SUB_WR5	SUB_WR4	SUB_WR3	SUB_WR2	SUB_WR1	SUB_WR0

Figure 8. 102 SUB_PANEL Control 2 Register (PAGE0 - R71h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SUB_SEL7	SUB_SEL6	SUB_SEL5	SUB_SEL4	SUB_SEL3	SUB_SEL2	SUB_SEL1	SUB_SEL0
R	1	SUB_SEL7	SUB_SEL6	SUB_SEL5	SUB_SEL4	SUB_SEL3	SUB_SEL2	SUB_SEL1	SUB_SEL0

Figure 8. 103 SUB_PANEL Control 3 Register (PAGE0 - R72h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SUB_EN	SUB_RS1	SUB_RS0	MPU_MODE	STN_EN	*	SUB_IM1	SUB_IM0
R	1	SUB_EN	SUB_RS1	SUB_RS0	MPU_MODE	STN_EN	0	SUB_IM1	SUB_IM0

Figure 8. 104 SUB_PANEL Control 4 Register (PAGE0 - R73h)

SUB_WR[15:0]: SUB_WR is the index of sub panel data write. Initial value of SUB_WR is ‘202h’. When MDDI host transfer GRAM data to sub panel driver IC via video stream packet, SUB_WR (initially 202h), index for GRAM access is automatically transferred before GRAM data transfer. When sub panel driver IC uses other address, 202h address have to be changed. Then user can change SUB_WR value from 202h to other value.

SUB_SEL: SUB_SEL is the index of main/sub panel selection. If SUB_SEL is ‘01h’, then main panel is selected, and if that is “00h”, then sub panel is selected. Using SUB_SEL register, Main / Sub panel selection index change is possible.

SUB_EN: Enables the sub panel interface.

SUBRS [1:0]: Specifies operation of RS2 terminal when receiving the video stream packet for STN type sub panel control. These register bits are enabled when STN = 1.

SUB_RS1	SUB_RS0	Operation
0	0	Hold (no change)
0	1	High level output
1	0	Low level output
1	1	reserved

MPU_MODE: Selects MPU type for sub panel
If MPU_MODE = 0, then i80-type parallel interface mode is selected.
If MPU_MODE = 1, then M68-type parallel interface mode is selected.

STN_EN: Selects panel type for sub panel.
If STN = 0, then TFT-type sub panel interface is selected.
If STN = 1, then STN-type sub panel interface is selected.

SIM [1:0] : Selects interface mode for sub panel.

SIM1	SIM0	Interface Mode
0	0	18-bit Parallel (1-time transfer)
0	1	9-bit Parallel (2-time transfer)
1	0	16-bit Parallel (1-time transfer)
1	1	8-bit Parallel (2-time transfer)

Note : The HX8357-A does not support read operation from sub panel Interface.

8.40 Column address counter 2~1 register (PAGE0 - R80h~R81h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CAC15	CAC14	CAC13	CAC12	CAC11	CAC10	CAC9	CAC8
R	1	CAC15	CAC14	CAC13	CAC12	CAC11	CAC10	CAC9	CAC8

Figure 8. 105 Column address counter 2 Register (PAGE0 - R80h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CAC7	CAC6	CAC5	CAC4	CAC3	CAC2	CAC1	CAC0
R	1	CAC7	CAC6	CAC5	CAC4	CAC3	CAC2	CAC1	CAC0

Figure 8. 106 Column address counter 1 Register (PAGE0 - R81h)

CAC[15:0]: Set GRAM Column addresses to the address counter (AC) before access to the GRAM. Once the GRAM data is written, the AC is automatically updated according to the MX, MY and MV bits. CAC[15:0] must always be equal to or less than EC[15:0].

8.41 Row address counter 2~1 register (PAGE0 - R82h~R83h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	RAC15	RAC14	RAC13	RAC12	RAC11	RAC10	RAC9	RAC8
R	1	RAC15	RAC14	RAC13	RAC12	RAC11	RAC10	RAC9	RAC8

Figure 8. 107 Row address counter 2 Register (PAGE0 - R82h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	RAC7	RAC6	RAC5	RAC4	RAC3	RAC2	RAC1	RAC0
R	1	RAC7	RAC6	RAC5	RAC4	RAC3	RAC2	RAC1	RAC0

Figure 8. 108 Row address counter 1 Register (PAGE0 - R83h)

RAC[15:0]: Set GRAM Row addresses to the address counter (AC) before access to the GRAM. Once the GRAM data is written, the AC is automatically updated according to the MX, MY and MV bits. RAC[15:0] must always be equal to or less than EP[15:0].

8.42 Set SPI read index register (RFDh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	INDEX 7	INDEX 6	INDEX 5	INDEX 4	INDEX 3	INDEX 2	INDEX 1	INDEX 0

Figure 8. 109 Set SPI Resd Index Register (RFDh)

8.43 Get SPI index data register (RFEh)

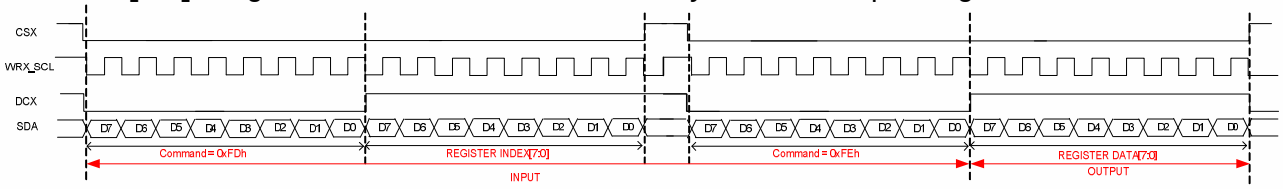
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0

Figure 8. 110 Get SPI Index Data Register (RFEh)

The registers only for 4-wire SPI I/F read.

INDEX[7:0]: Register address for SPI read. If will read register value in 4-wire SPI I/F, the system must input Register address.

DATA[7:0]: Register valuu in 4-wire SPI I/F, the system must input Register address.



8.44 Command page select register (RFFh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	PAGE_SEL 1	PAGE_SEL 0
R	1	0	0	0	0	0	0	PAGE_SEL 1	PAGE_SEL 0

Figure 8. 111 Command Page select 2 Register (RFFh)

PAGE_SEL[1:0]: Command set page select.

PAGE_SEL1	PAGE_SEL0	Command Page
0	0	Page 0
0	1	Page 1

8.45 DGC Control register (PAGE1 – R00h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	DGC_EN
R	1	0	0	0	0	0	0	0	DGC_EN

Figure 8. 112 DGC Control Register (PAGE1 – R00h)

DGC_EN: Digital gamma correction enable.
0 : Disable
1 : Enable

8.46 DGC LUT1~192 register (PAGE1 – R01h~C0h)

For more information about these registers, Please refer to "7.2.2 Gray Voltage Generator for Digital Gamma Correction" section

8.47 CABC control 5~7 register (PAGE1 – RC3h, RC5h, RC7h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	PWM DIV2	PWM DIV1	PWM DIV0	1	1	INPL US	1
R	1	0	PWM DIV2	PWM DIV1	PWM DIV0	1	1	INPL US	1

Figure 8. 113 CABC control 5 (PAGE1 – RC3h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PWM_ PERIOD7	PWM_ PERIOD6	PWM_ PERIOD5	PWM_ PERIOD4	PWM_ PERIOD3	PWM_ PERIOD2	PWM_ PERIOD1	PWM_ PERIOD0
R	1	PWM_ PERIOD7	PWM_ PERIOD6	PWM_ PERIOD5	PWM_ PERIOD4	PWM_ PERIOD3	PWM_ PERIOD2	PWM_ PERIOD1	PWM_ PERIOD0

Figure 8. 114 CABC control 6 (PAGE1 – RC5h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	0	DIM_FRAME6	DIM_FRAME5	DIM_FRAME4	DIM_FRAME3	DIM_FRAME2	DIM_FRAME1	DIM_FRAME0
R	1	0	DIM_FRAME6	DIM_FRAME5	DIM_FRAME4	DIM_FRAME3	DIM_FRAME2	DIM_FRAME1	DIM_FRAME0

Figure 8. 115 CABC control 7 (PAGE1 – RC7h)

PWM_DIV[2:0]: Internal PWM_CLK divider for CABC clock.

PWM_DIV[2:0]	Divider
0	PWM_CLK/1
1	PWM_CLK/2
2	PWM_CLK/4
3	PWM_CLK/8
4	PWM_CLK/16
5	PWM_CLK/32
6	PWM_CLK/64
7	PWM_CLK/128

Note:1. PWM_CLK is OSC frequency in any interface

INVPULS: The backlight PWM output polarity select.
'0', The backlight PWM output is low level active.
'1', The backlight PWM output is high level active.

PWM_PERIOD[7:0] : The backlight PWM output period setting.
Backlight PWM output period = 1 / (PWM_CLK / clock divider (PWMDIV)) x (255x(PWM_PERIOD[7:0]+1))

DIM_FRAME[6:0] : Manual brightness setting dimming period.

8.48 Gain select register 0~8 (PAGE1 – RCBh~D3h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 06	DBG 05	DBG 04	DBG 03	DBG 02	DBG 01	DBG 00
R	1	0	DBG 06	DBG 05	DBG 04	DBG 03	DBG 02	DBG 01	DBG 00

Figure 8. 116 Gain select register 0 (PAGE1 – RCBh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 16	DBG 15	DBG 14	DBG 13	DBG 12	DBG 11	DBG 10
R	1	0	DBG 16	DBG 15	DBG 14	DBG 13	DBG 12	DBG 11	DBG 10

Figure 8. 117 Gain select register 1 (PAGE1 – RCCh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 26	DBG 25	DBG 24	DBG 23	DBG 22	DBG 21	DBG 20
R	1	0	DBG 26	DBG 25	DBG 24	DBG 23	DBG 22	DBG 21	DBG 20

Figure 8. 118 Gain select register 2 (PAGE1 – RCDh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 36	DBG 35	DBG 34	DBG 33	DBG 32	DBG 31	DBG 30
R	1	0	DBG 36	DBG 35	DBG 34	DBG 33	DBG 32	DBG 31	DBG 30

Figure 8. 119 Gain select register 3 (PAGE1 – RCEh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 46	DBG 45	DBG 44	DBG 43	DBG 42	DBG 41	DBG 40
R	1	0	DBG 46	DBG 45	DBG 44	DBG 43	DBG 42	DBG 41	DBG 40

Figure 8. 120 Gain select register 4 (PAGE1 – RCFh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 56	DBG 55	DBG 54	DBG 53	DBG 52	DBG 51	DBG 50
R	1	0	DBG 56	DBG 55	DBG 54	DBG 53	DBG 52	DBG 51	DBG 50

Figure 8. 121 Gain select register 5 (PAGE1 – RD0h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 66	DBG 65	DBG 64	DBG 63	DBG 62	DBG 61	DBG 60
R	1	0	DBG 66	DBG 65	DBG 64	DBG 63	DBG 62	DBG 61	DBG 60

Figure 8. 122 Gain select register 6 (PAGE1 – RD1h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 76	DBG 75	DBG 74	DBG 73	DBG 72	DBG 71	DBG 70
R	1	0	DBG 76	DBG 75	DBG 74	DBG 73	DBG 72	DBG 71	DBG 70

Figure 8. 123 Gain select register 7 (PAGE1 – RD2h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DBG 86	DBG 85	DBG 84	DBG 83	DBG 82	DBG 81	DBG 80
R	1	0	DBG 86	DBG 85	DBG 84	DBG 83	DBG 82	DBG 81	DBG 80

Figure 8. 124 Gain select register 8 (PAGE1 – RD3h)

I

DBG0~8[6:0] : Gain select register 0~8

DBGX	Duty	DBGX	Duty	DBGX	Duty
20	100.00%	30	66.67%	40	49.80%
21	96.86%	31	65.10%		
22	94.12%	32	63.92%		
23	91.37%	33	62.75%		
24	89.02%	34	61.57%		
25	86.27%	35	60.39%		
26	84.31%	36	59.22%		
27	81.96%	37	58.04%		
28	80.00%	38	56.86%		
29	78.04%	39	56.08%		
2A	76.08%	3A	54.90%		
2B	74.51%	3B	54.12%		
2C	72.55%	3C	53.33%		
2D	70.98%	3D	52.16%		
2E	69.41%	3E	51.37%		
2F	67.84%	3F	50.59%		

	UI	ST	MV
DBG0	24	40	40
DBG1	24	3C	3C
DBG2	24	38	38
DBG3	23	34	34
DBG4	23	33	33
DBG5	23	32	32
DBG6	22	2B	2D
DBG7	22	24	2B
DBG8	22	22	28

8.48 Power saving counter 1~4 (PAGE0 – RE4h~E7h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EQVCI_M17	EQVCI_M16	EQVCI_M15	EQVCI_M14	EQVCI_M13	EQVCI_M12	EQVCI_M11	EQVCI_M10
R	1	EQVCI_M17	EQVCI_M16	EQVCI_M15	EQVCI_M14	EQVCI_M13	EQVCI_M12	EQVCI_M11	EQVCI_M10

Figure 8. 125 Power saving register 1 (PAGE0 – RE4h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EQGND_M17	EQGND_M16	EQGND_M15	EQGND_M14	EQGND_M13	EQGND_M12	EQGND_M11	EQGND_M10
R	1	EQGND_M17	EQGND_M16	EQGND_M15	EQGND_M14	EQGND_M13	EQGND_M12	EQGND_M11	EQGND_M10

Figure 8. 126 Power saving register 2 (PAGE0 – RE5h)

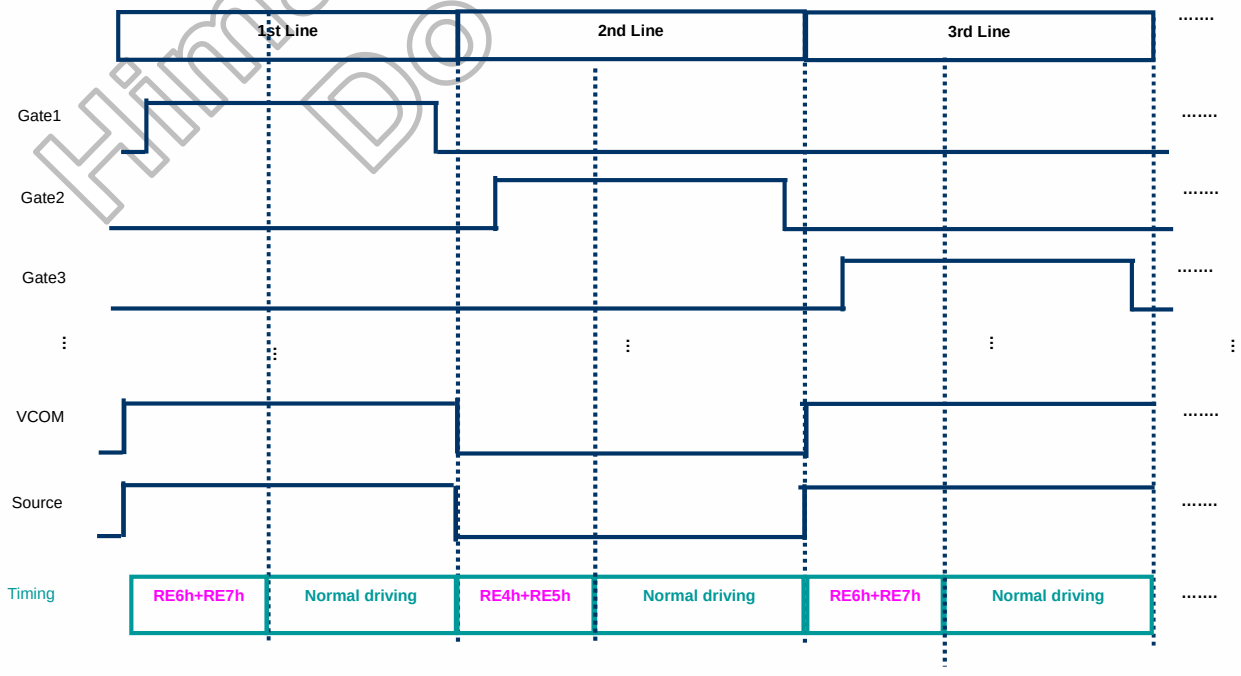
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EQVCI_M07	EQVCI_M06	EQVCI_M05	EQVCI_M04	EQVCI_M03	EQVCI_M02	EQVCI_M01	EQVCI_M00
R	1	EQVCI_M07	EQVCI_M06	EQVCI_M05	EQVCI_M04	EQVCI_M03	EQVCI_M02	EQVCI_M01	EQVCI_M00

Figure 8. 127 Power saving register 3 (PAGE0 – RE6h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EQGND_M07	EQGND_M06	EQGND_M05	EQGND_M04	EQGND_M03	EQGND_M02	EQGND_M01	EQGND_M00
R	1	EQGND_M07	EQGND_M06	EQGND_M05	EQGND_M04	EQGND_M03	EQGND_M02	EQGND_M01	EQGND_M00

Figure 8. 128 Power saving register 4 (PAGE0 – RE7h)

EQVCI_M1[7:0]: used to tuned the timing of EQ function to save power.
EQGND_M1[7:0]: used to tuned the timing of EQ function to save power.
EQVCI_M0[7:0]: used to tuned the timing of EQ function to save power.
EQGND_M0[7:0]: used to tuned the timing of EQ function to save power.



9. Layout Recommendation

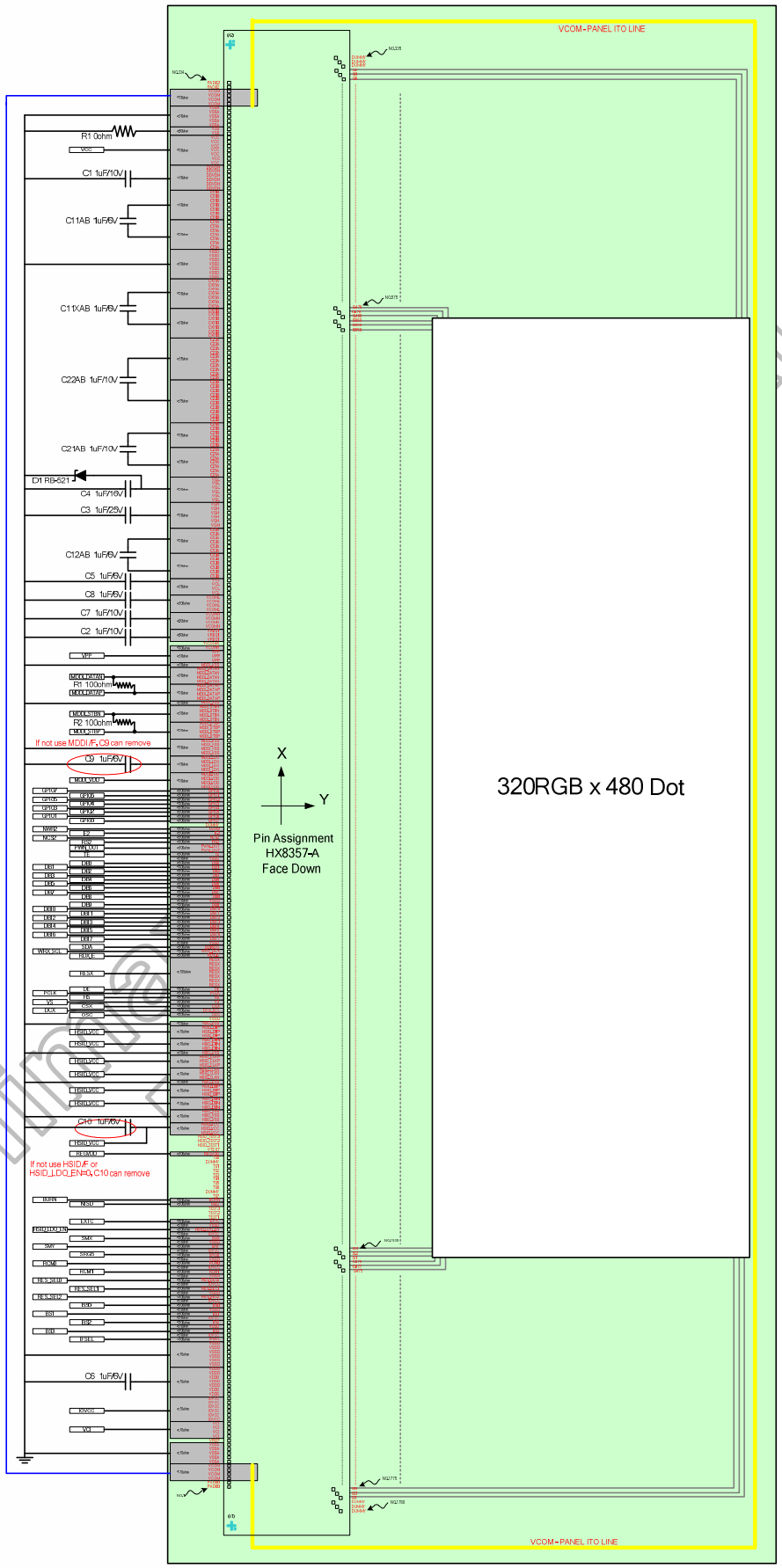


Figure 9. 1 Layout Recommendation of HX8357-A

9.1 Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VPP	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
MDDI_VDD	Power supply	10	Ω
MDDI_VSS	Power supply	10	Ω
HSID_VCC	Power supply or Capacitor connection	10	Ω
HSID_VSS	Power supply	10	Ω
OSC	Input	100	Ω
BS[3:0], BURN, REGVDD,RES_SEL[2:0], BURN, HSID_LDO_EN	Input	100	Ω
RDX_E, WRX_DCX, DCX_SCL, CSX, RESX	Input	100	Ω
PCLK, DE, VS, HS	Input	100	Ω
MDDI_STBP, MDDI_STBN, MDDI_DATAP, MDDI_DATAN	Input	10	Ω
HSID_CLKP, HSID_CLKN, HSID_D0P, HSID_D0N, HSID_D1P, HSID_D1N	Input	10	Ω
VCOMR	Input	100	Ω
VGS	Input	30	Ω
TEST[3:1]	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
DDVDH	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1	Capacitor connection	30	Ω
MDDI_LDO	Capacitor connection	10	Ω
VCOM, VCOMH, VCOML	Capacitor connection	10	Ω
C11A, C11B, CX11A, CX11B	Capacitor connection	10	Ω
C12A, C12B	Capacitor connection	10	Ω
C21A, C21B	Capacitor connection	15	Ω
C22A, C22B	Capacitor connection	15	Ω
NCS2, RS2, NWR2, E2, TE, NISD, PWM_OUT, VREF.	Output	100	Ω
GPIO7-0, SDA, DB[17:0]	Input/Output	100	Ω

Table 9. 1 Maximum Layout Resistance

9.2 External Components Connection

Capacitor	Recommended voltage	Capacity
C1 (DDVDH-VSSA)	10V	1 µF (B characteristics)
C2 (VREG1-VSSA)	10V	1 µF (B characteristics)
C3 (VGH-VSSA)	25V	1 µF (B characteristics)
C4 (VGL-VSSA)	16V	1 µF (B characteristics)
C5 (VCL-VSSA)	6V	1 µF (B characteristics)
C6(VDDD-VSSA)	6V	1 µF (B characteristics)
C11AB (C11A/B)	6V	1 µF (B characteristics)
CX11AB (CX11A/B)	6V	1 µF (B characteristics)
C12AB (C12A/B)	6V	1 µF (B characteristics)
C21AB (C21A/B)	10V	1 µF (B characteristics)
C22AB (C22A/B)	10V	1 µF (B characteristics)
C8 (VCOML-VSSA)	6V	1 µF (B characteristics)
C7 (VCOMH-VSSA)	10V	1 µF (B characteristics)
C9 (MDDI_LDO-MDDI_VSS)	6V	1 µF (B characteristics)
C10 (HSID_VCC-HSID_VSS)	6V	1 µF (B characteristics)
D1 (VGL-VSSA)	Schottky Diode	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: RB521S-30)
R1, R2	Resistor	100 ohm

Note: (1) If not use MDDI I/F, the C19, R1, R2 can remove.
(2) If not use HSID I/F or HSID_LDO_EN=0, the C10 can removed.

10. OTP Programming

10.1 OTP Table

OTP_INDEX	D7	D6	D5	D4	D3	D2	D1	D0
0x00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
0x01h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
0x02h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
0x03h	VMF17	VMF16	VMF15	VMF14	VMF13	VMF12	VMF11	VMF10
0x04h	VMF27	VMF26	VMF25	VMF24	VMF23	VMF22	VMF21	VMF20
0x05h	VMF37	VMF36	VMF35	VMF34	VMF33	VMF32	VMF31	VMF30
0x06h	VMH7	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0
0x07h	VML7	VML6	VML5	VML4	VML3	VML2	VML1	VML0
0x08h	Vaild_ID	(no use)	(no use)	Valid_VML	Valid_VMH	Valid_VMF3	Valid_VMF2	Valid_VMF1
0x09h	Himax internal use (not open)							
0x0Ah	Himax internal use (not open)							
0x0Bh	Himax internal use (not open)							
0x0Ch	Himax internal use (not open)							
0x0Dh	Himax internal use (not open)							
0x0Eh	Himax internal use (not open)							
0x0Fh	Himax internal use (not open)							
0x10h	Himax internal use (not open)							
0x11h	Himax internal use (not open)							
0x12h	Himax internal use (not open)							
0x13h	Himax internal use (not open)							
0x14h	Himax internal use (not open)							
0x15h	Himax internal use (not open)							
0x16h	Himax internal use (not open)							
0x17h	Himax internal use (not open)							
0x18h	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
0x19h	Himax internal use (not open)							
0x1Ah	Himax internal use (not open)							
0x1Bh	Himax internal use (not open)							
0x1Ch	Himax internal use (not open)							
0x1Dh	Himax internal use (not open)							
0x1Eh	Himax internal use (not open)							
0x1Fh	Himax internal use (not open)							
0x20h	Himax internal use (not open)							
0x21h	Himax internal use (not open)							
0x22h	Himax internal use (not open)							
0x23h	Valid_gamma1	(no use)	VRP0[5:0]					
0x24h	(no use)	(no use)	VRP1[5:0]					
0x25h	(no use)	(no use)	VRP2[5:0]					
0x26h	(no use)	(no use)	VRP3[5:0]					
0x27h	(no use)	PRP0[6:0]						
0x28h	(no use)	RPR1[6:0]						
0x29h	VRP4[5:0]		PKP0[4:0]					
0x2Ah			PKP1[4:0]					
0x2Bh	VRP5[5:0]		PKP2[4:0]					
0x2Ch			PKP3[4:0]					
0x2Dh	(no use)	(no use)	(no use)	PKP4[4:0]				
0x2Eh	(no use)	(no use)	VRN0[5:0]					
0x2Fh	(no use)	(no use)	VRN1[5:0]					
0x30h	(no use)	(no use)	VRN2[5:0]					

0x31h	(no use)	(no use)	VRN3[5:0]		
0x32h	(no use)	PRN0[6:0]			
0x33h	(no use)	PRN1[6:0]			
0x34h	VRN4[5:0]		PKN0[4:0]		
0x35h			PKN1[4:0]		
0x36h	VRN5[5:0]		PKN2[4:0]		
0x37h			PKN3[4:0]		
0x38h	(no use)	(no use)	(no use)	PKN4[4:0]	
0x39h	CGMN1[1:0]		CGMN0[1:0]	CGMP1[1:0]	CGMP0[1:0]
0x3Ah	Valid_gamma2	(no use)	VRP0[5:0]		
0x3Bh	(no use)	(no use)	VRP1[5:0]		
0x3Ch	(no use)	(no use)	VRP2[5:0]		
0x3Dh	(no use)	(no use)	VRP3[5:0]		
0x3Eh	(no use)	PRP0[6:0]			
0x3Fh	(no use)	RPR1[6:0]			
0x40h	VRP4[5:0]		PKP0[4:0]		
0x41h			PKP1[4:0]		
0x42h	VRP5[5:0]		PKP2[4:0]		
0x43h			PKP3[4:0]		
0x44h	(no use)	(no use)	(no use)	PKP4[4:0]	
0x45h	(no use)	(no use)	VRN0[5:0]		
0x46h	(no use)	(no use)	VRN1[5:0]		
0x47h	(no use)	(no use)	VRN2[5:0]		
0x48h	(no use)	(no use)	VRN3[5:0]		
0x49h	(no use)	PRN0[6:0]			
0x4Ah	(no use)	PRN1[6:0]			
0x4Bh	VRN4[5:0]		PKN0[4:0]		
0x4Ch			PKN1[4:0]		
0x4Dh	VRN5[5:0]		PKN2[4:0]		
0x4Eh			PKN3[4:0]		
0x4Fh	(no use)	(no use)	(no use)	PKN4[4:0]	
0x50h	CGMN1[1:0]		CGMN0[1:0]	CGMP1[1:0]	CGMP0[1:0]
0x51h	Valid_gamma3	(no use)	VRP0[5:0]		
0x52h	(no use)	(no use)	VRP1[5:0]		
0x53h	(no use)	(no use)	VRP2[5:0]		
0x54h	(no use)	(no use)	VRP3[5:0]		
0x55h	(no use)	PRP0[6:0]			
0x56h	(no use)	RPR1[6:0]			
0x57h	VRP4[5:0]		PKP0[4:0]		
0x58h			PKP1[4:0]		
0x59h	VRP5[5:0]		PKP2[4:0]		
0x5Ah			PKP3[4:0]		
0x5Bh	(no use)	(no use)	(no use)	PKP4[4:0]	
0x5Ch	(no use)	(no use)	VRN0[5:0]		
0x5Dh	(no use)	(no use)	VRN1[5:0]		
0x5Eh	(no use)	(no use)	VRN2[5:0]		
0x5Fh	(no use)	(no use)	VRN3[5:0]		
0x60h	(no use)	PRN0[6:0]			
0x61h	(no use)	PRN1[6:0]			
0x62h	VRN4[5:0]		PKN0[4:0]		
0x63h			PKN1[4:0]		
0x64h	VRN5[5:0]		PKN2[4:0]		

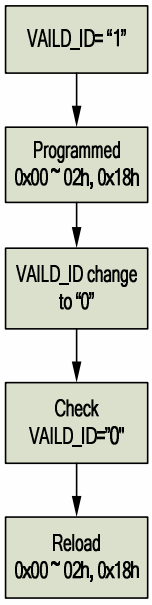
0x65h				PKN3[4:0]				
0x66h	(no use)	(no use)	(no use)	PKN4[4:0]				
0x67h	CGMN1[1:0]		CGMN0[1:0]		CGMP1[1:0]		CGMP0[1:0]	
0x68h	Valid_gamma4	(no use)	VRP0[5:0]					
0x69h	(no use)	(no use)	VRP1[5:0]					
0x6Ah	(no use)	(no use)	VRP2[5:0]					
0x6Bh	(no use)	(no use)	VRP3[5:0]					
0x6Ch	(no use)	PRP0[6:0]						
0x6Dh	(no use)	RPR1[6:0]						
0x6Eh	VRP4[5:0]		PKP0[4:0]					
0x6Fh			PKP1[4:0]					
0x70h	VRP5[5:0]		PKP2[4:0]					
0x71h			PKP3[4:0]					
0x72h	(no use)	(no use)	(no use)	PKP4[4:0]				
0x73h	(no use)	(no use)	VRN0[5:0]					
0x74h	(no use)	(no use)	VRN1[5:0]					
0x75h	(no use)	(no use)	VRN2[5:0]					
0x76h	(no use)	(no use)	VRN3[5:0]					
0x77h	(no use)	PRN0[6:0]						
0x78h	(no use)	PRN1[6:0]						
0x79h	VRN4[5:0]		PKN0[4:0]					
0x7Ah			PKN1[4:0]					
0x7Bh	VRN5[5:0]		PKN2[4:0]					
0x7Ch			PKN3[4:0]					
0x7Dh	(no use)	(no use)	(no use)	PKN4[4:0]				
0x7Eh	CGMN1[1:0]		CGMN0[1:0]		CGMP1[1:0]		CGMP0[1:0]	
0x7Fh	Himax internal use (not open)							

Note: (1) The default value of OTP memory bits are all "1".

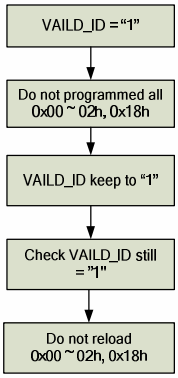
(2)VALID_xxx bit decide the OPT reload Enable/Disable, the default value is "1". If Valid_xxx correlation OTP_Mask bit is "0" and set OTP_PORG to "1", the VALID_xxx bit will be changed to "0" automatically and execute the OTP reload.

For example:

Condition 1: Programmed all index of 0x00h ~ 0x2h and 0x18h and Index-0x08h's bit 7.



Condition 2: Do not program all index of 0x00h ~ 0x2h and 0x18h



Note 3: There are some conditions that HX8357-A can reload OTP.
1. Hardware reset

Note 4: VMF can be programed 3 times: Default Valid_VMF1 will be programed when CP.

The value of Valid_VMF3~1	Status of index 0x03h ~ 0x05h
Valid_VMF3~1="111"	Not program any VMF1~3[7:0],
Valid_VMF3~1="110"	Only program VMF1[7:0] and reload VMF1[7:0]
Valid_VMF3~1="101"	Only program VMF2[7:0] and reload VMF2[7:0]
Valid_VMF3~1="100"	Already program VMF1~2[7:0] and reload VMF2[7:0]
Valid_VMF3~1="011"	Only program VMF3[7:0] and reload VMF3[7:0]
Valid_VMF3~1="010"	Already program VMF1[7:0], VMF3[7:0] and reload VMF3[7:0]
Valid_VMF3~1="001"	Already program VMF2~3[7:0] and reload VMF3[7:0]
Valid_VMF3~1="000"	Already program VMF1~3[7:0] and reload VMF3[7:0]

10.2 OTP programming flow

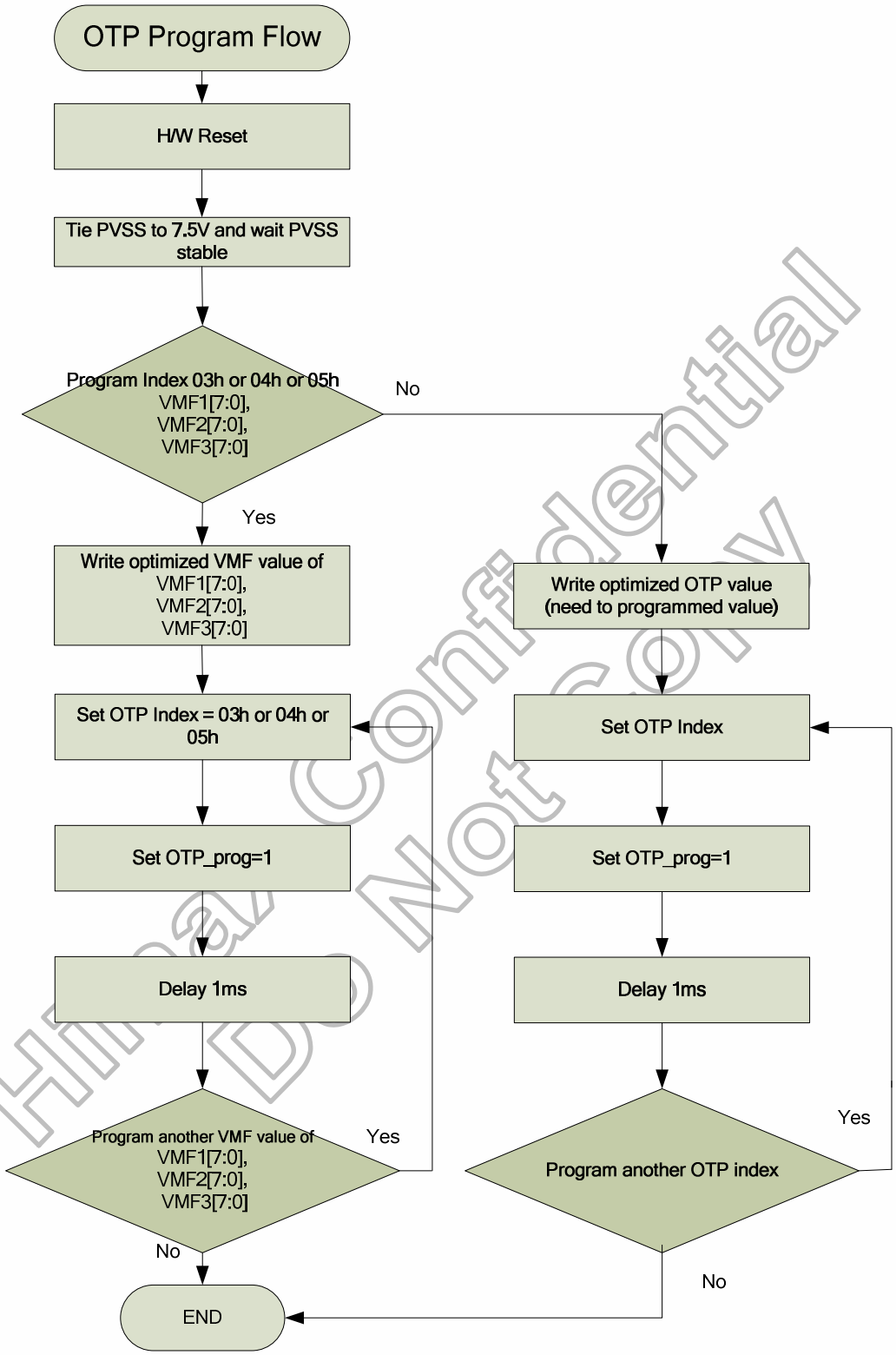


Figure 10. 1 OTP Programming Sequence

For example: ID1~ID4 programming flow

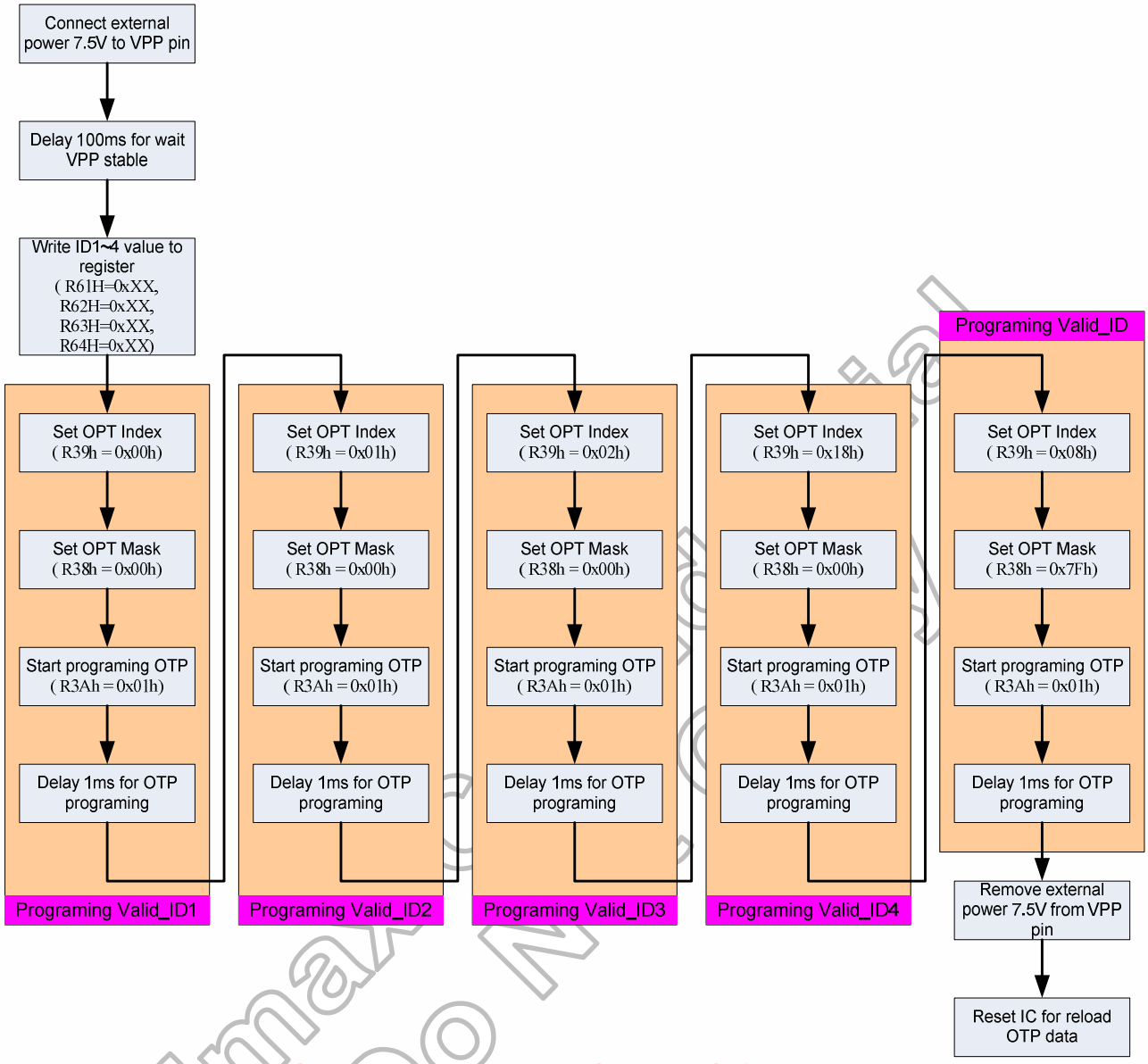


Figure 10. 2 OTP Programming example for ID1~ID4

10.3 OTP Programming sequence

<table>
<tr><th>Step</th><th>Operation</th></tr>
<tr><td>1</td><td>Power on and reset the module</td></tr>
<tr><td>2</td><td>Connect external power 7.5V to VPP pin</td></tr>
<tr><td>3</td><td>Wait 100ms for VPP stable</td></tr>
<tr><td>4</td><td>Write optimized value to related register
<table>
<tr><th>Command</th><th>Register</th><th>Description</th></tr>
<tr><td>ID1 (R61h)</td><td>ID1[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>ID2 (R62h)</td><td>ID2[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>ID3 (R63h)</td><td>ID3[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>VCOM Control 1 (R23h)</td><td>VMF[7:0],</td><td>Vcom offset voltage for normal mode, Idle mode and Partial Idle mode (High level voltage of VCOM)</td></tr>
<tr><td>VCOM Control 2 (R24h)</td><td>VMH[7:0]</td><td>VcomH voltage for normal mode, Idle mode and Partial Idle mode (High level voltage of VCOM)</td></tr>
<tr><td>VCOM Control 3 (R25h)</td><td>VML[7:0]</td><td>VcomL voltage for normal mode, Idle mode and Partial Idle mode (Low level voltage of VCOM)</td></tr>
<tr><td>ID4 (R64h)</td><td>ID4[7:0]</td><td>LCD module/driver version</td></tr>
<tr><td>GAMMA(R40h~R5Dh)</td><td>Gamma value</td><td>Set gamma parameter</td></tr>
</table></td></tr>
<tr><td>5</td><td>Specify OTP_index (note 1)
<table>
<tr><th>OTP_index (Write – For Program)</th><th>Parameter</th></tr>
<tr><td>0x00h</td><td>ID1[7:0]</td></tr>
<tr><td>0x01h</td><td>ID2[7:0]</td></tr>
<tr><td>0x02h</td><td>ID3[7:0]</td></tr>
<tr><td>0x03h</td><td>VMF1[7:0],</td></tr>
<tr><td>0x04h</td><td>VMF2[7:0]</td></tr>
<tr><td>0x05h</td><td>VMF37:0]</td></tr>
<tr><td>0x06h</td><td>VMH[7:0]</td></tr>
<tr><td>0x07h</td><td>VML[7:0]</td></tr>
<tr><td>0x08h</td><td>Vaild_ID, Valid_VML, Valid_VMH, Valid_VMF3, Valid_VMF2, Valid_VMF1</td></tr>
<tr><td>0x18h</td><td>ID4[7:0]</td></tr>
<tr><td>23h ~ 7Eh</td><td>Gamma value</td></tr>
</table></td></tr>
<tr><td>6</td><td>Set OTP_Mask=0xXXh, programming the entire bit of one parameter.</td></tr>
<tr><td>7</td><td>Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.</td></tr>
<tr><td>8</td><td>Wait 1 ms</td></tr>
<tr><td>9</td><td>Complete programming one parameter to OTP. If continue to programming other parameter, return to step (5). Otherwise, power off the module and remove the external power on VPP pin.</td></tr>
<tr><td>10</td><td>Remove external power 7.5V from VPP pin</td></tr>
</table>

Note: (1) When do the OTP program on gamma setting (G1: 23h~39h, G2: 3Ah~50h, G3: 51h~67h, G4: 68h~7Eh), user just specify the 23h, the all settings of G1 will be programmed. Similarly the same condition is also on programming G2, G3 and G4. (G2: 3Ah, G3: 51h, G4: 68h).

10.4 OTP Read flow

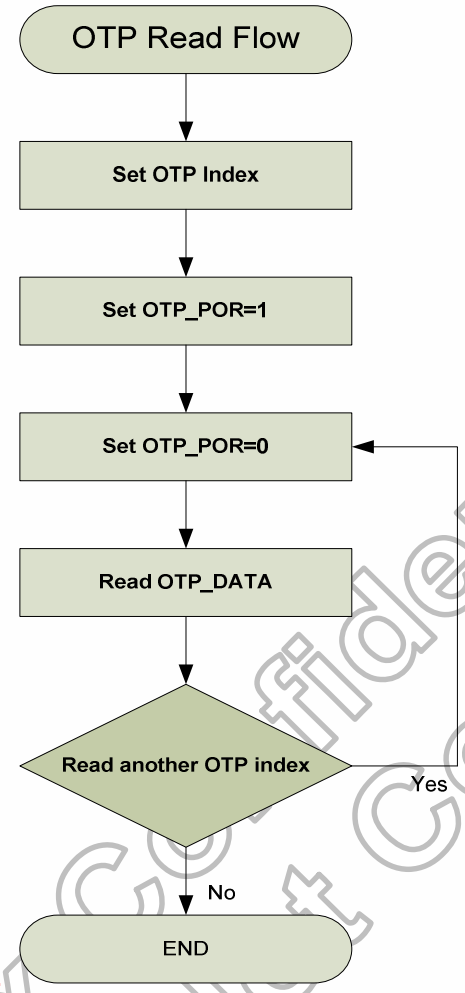


Figure 10. 3 OTP Read Sequence

For example: OTP ID1 read flow

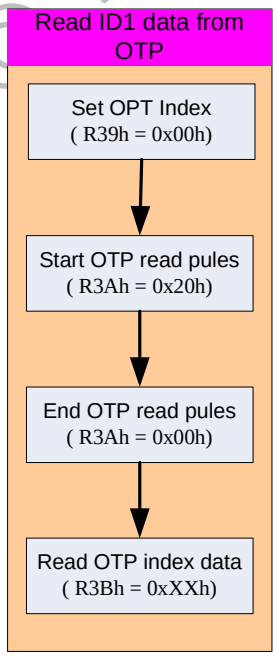
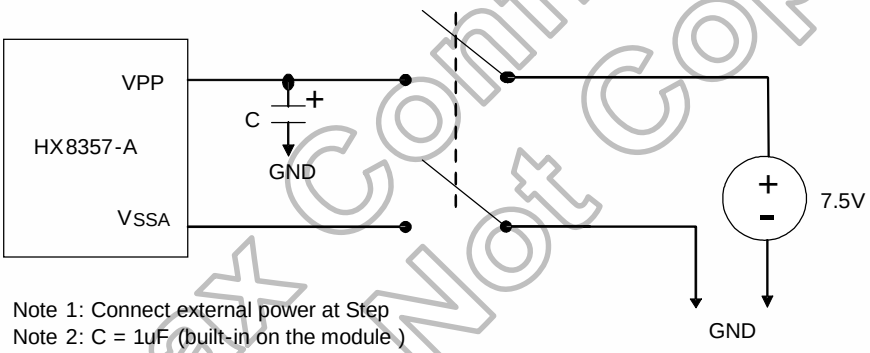


Figure 10. 4 OTP read example for ID1

10.5 OTP Read sequence

Step	Operation	
1	Specify OTP_index	
	OTP_index (Read – For get OTP value)	Parameter
	0x00h	ID1[7:0]
	0x01h	ID2[7:0]
	0x02h	ID3[7:0]
	0x03h	VMF1[7:0],
	0x04h	VMF2[7:0]
	0x05h	VMF37:0]
	0x06h	VMH[7:0]
	0x07h	VML[7:0]
	0x08h	Vaild_ID, Valid_VML, Valid_VMH, Valid_VMF3, Valid_VMF2, Valid_VMF1
	0x18h	ID4[7:0]
	23h ~ 7Eh	Gamma value
2	Set OTP_POR=1.	
3	Set OTP_POR=0.	
4	Read OTP_DATA.	

10.6 Programming circuitry



Note 1: Connect external power at Step
Note 2: C = 1uF (built-in on the module)

11. Electrical Characteristic

11.1 Absolute maximum ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3 to +4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3 to +4.6	Note(1),(3)
Power Supply Voltage 3	VCC ~ VSSA	V	-0.3 to +4.6	Note(1),(4)
Power Supply Voltage 4	DDVDH ~ VSSA	V	-0.3 to +6.6	Note(5)
Power Supply Voltage 5	VSSA ~ VCL	V	-0.3 to +4.6	Note(6)
Power Supply Voltage 6	DDVDH ~ VCL	V	-0.3 to +9	Note(7)
Power Supply Voltage 7	VGH ~ VSSA	V	-0.3 to +18.5	Note(8)
Power Supply Voltage 8	VSSA ~ VGL	V	0 to -16.5	Note(9)
Input Voltage	V_{IN}	V	-0.3 to IOVCC+0.3	-
Operating Temperature	Topr	℃	-40 to +85	Note(10)
Storage Temperature	Tstg	℃	-55 to +110	Note(10)

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure VCC ≥ VSSA.
(5) To make sure DDVDH ≥ VSSA.
(6) To make sure VSSA ≥ VCL.
(7) To make sure DDVDH ≥ VCL.
(8) To make sure VGH ≥ VSSA.
(9) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(10) For die and wafer products, specified up to +85℃.

Table 11. 1 Absolute Maximum Ratings

11.2 ESD protection level

Mode	Test Condition	Protection Level	Unit
Human Body Model	C=100 pF, R=1.5 kΩ	±3.0K	V
Machine Model	C=200 pF, R=0.0 Ω	±300	V

Table 11. 2 ESD Protection Level

11.3 DC characteristics

Item	Symbol	Unit	Test Condition	Spec.			Note
				Min.	Typ.	Max.	
Input high voltage	V_{IH}	V	IOVCC= 1.65 ~ 3.3V	0.7xIOVCC	-	IOVCCc	-
Input low voltage	V_{IL}	V	IOVCC= 1.65 ~ 3.3V	-0.3V	-	0.3xIOVCC	-
Output high voltage (DB17-0 Pins)	V_{OH1}	V	I_{OH} = -0.1 mA	0.8xIOVCC	-	-	-
Output low voltage (DB17-0Pins)	V_{OL1}	V	IOVcc= 1.65 ~ 2.4V I_{OL} = 0.1mA	-	-	0.2xIOVCC	-
I/O leakage current	I_{Li}	µA	Vin = 0 ~ VCC	-1	-	1	-
Current consumption during normal operation (IOVCC-VSSD)	$I_{OP(IOVcc)}$	µA	VCC =2.8V ,IOVCC=2.8V Ta=25°C , GRAM data = 0000h, Frame rate = 70Hz, REV_panel=0, AP=100, FS0=00, FS1=11, BT=0100, VRH=011000, VCOMG=1 No panel load	-	TBD		-
Current consumption during normal operation (VCC– VSSD)	$I_{OP(Vcc)}$	mA		-	TBD	-	-
Current consumption during standby mode (IOVCC-VSSD)	$I_{ST(IOVcc)}$	µA	IOVCC=2.8V , VCC=2.8V Ta=25°C	-	7	25	-
Current consumption during standby mode (VCC– VSSD)	$I_{ST(Vcc)}$	µA			4	10	
Output voltage deviation	-	mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-	-	35	-

Table 11. 3 DC Characteristic (VCC=VCI= 2.5 ~ 3.3V, IOVCC = 1.65~3.3V, Ta = -40 ~ 85 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal shall be interpreted as a logic-one level.		0	50	mV
V_{IT-}	Receiver differential input low threshold voltage. Below this differential voltage the input signal shall be interpreted as a logic-zero level.	-50	0		
V_{IT+_hib}	Receiver differential input high threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal shall be interpreted as a logic-one level.		125	175	mV
V_{IT-_hib}	Receiver differential input low threshold voltage (offset for hibernation wake-up). Below this differential voltage the input signal shall be interpreted as a logic-zero level.	75	125		mV
$V_{Input-Range}$	Allowable receiver input voltage range with respect to client ground.	0		1.65	V
Power Consumption in Hibernation	Power consumption during the MDDI is in hibernation mode, and not data drive through MDDI path		TBD		uA
Power Consumption in Active mode	Power consumption during the MDDI is in Active mode. And host can control client through MDDI I/F.		TBD		mA

Table 11. 4 MDDI DC Characteristic (MDDI_VDD= 2.3 ~ 3.3V, Ta = -40 ~ 85 °C)

11.4 AC characteristics

11.4.1 Parallel interface characteristics (8080-series MPU)

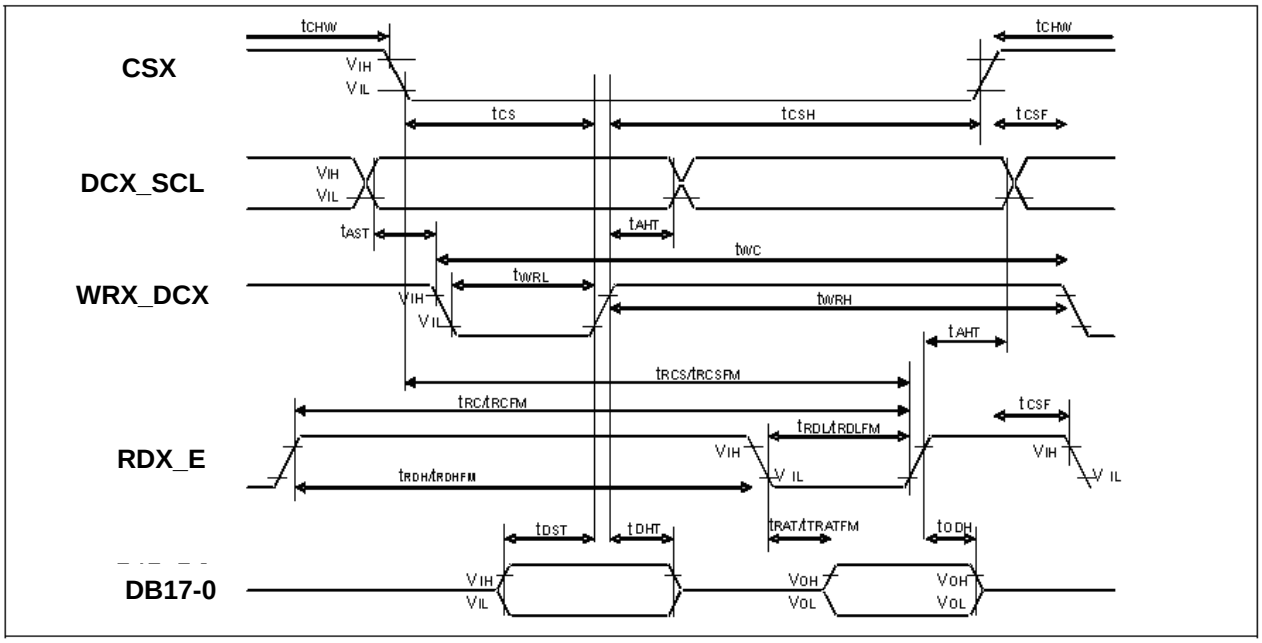


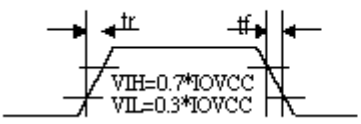
Figure 11. 1 Parallel Interface Characteristics (8080-series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V,Ta = -40 to 85°C)

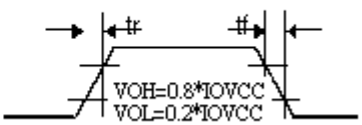
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX_SCL	t_{AST}	Address setup time	10	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
CSX	t_{CHW}	Chip select "H" pulse width	0	-	ns	-
	t_{CS}	Chip select setup time (Write)	35	-		
	t_{RCSFM}	Chip select setup time	355	-		
	t_{CSF}	Chip select wait time (Write/Read)	10	-		
	t_{CSH}	Chip select hold time	10	-		
WRX_DCX	t_{WC}	Write cycle	66	-	ns	-
	t_{WRH}	Control pulse "H" duration	15	-		
	t_{WRL}	Control pulse "L" duration	15	-		
RDX_E	t_{RCFM}	Read cycle	450	-	ns	When read from GRAM
	t_{RDHFM}	Control pulse "H" duration	90	-		
	t_{RDLFM}	Control pulse "L" duration	355	-		
DB17-0	t_{DST}	Data setup time	15	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DHT}	Data hold time	10	-		
	t_{RATFM}	Read access time	-	340		
	t_{ODH}	Output disable time	20	80		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



Output Signal Slope



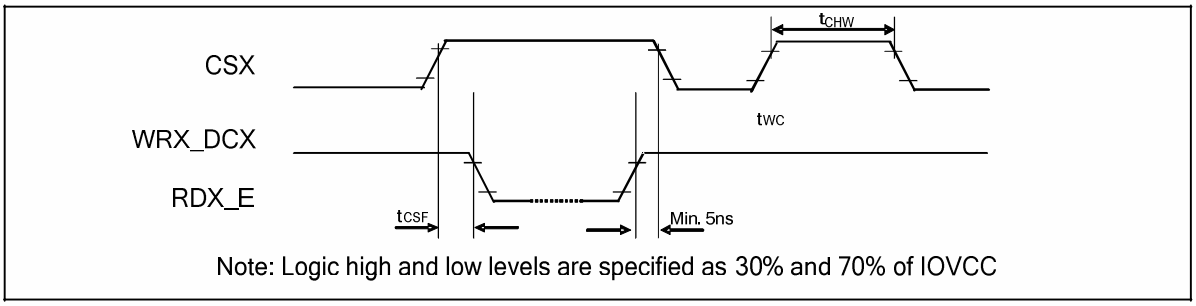


Figure 11. 2 Chip Select Timing

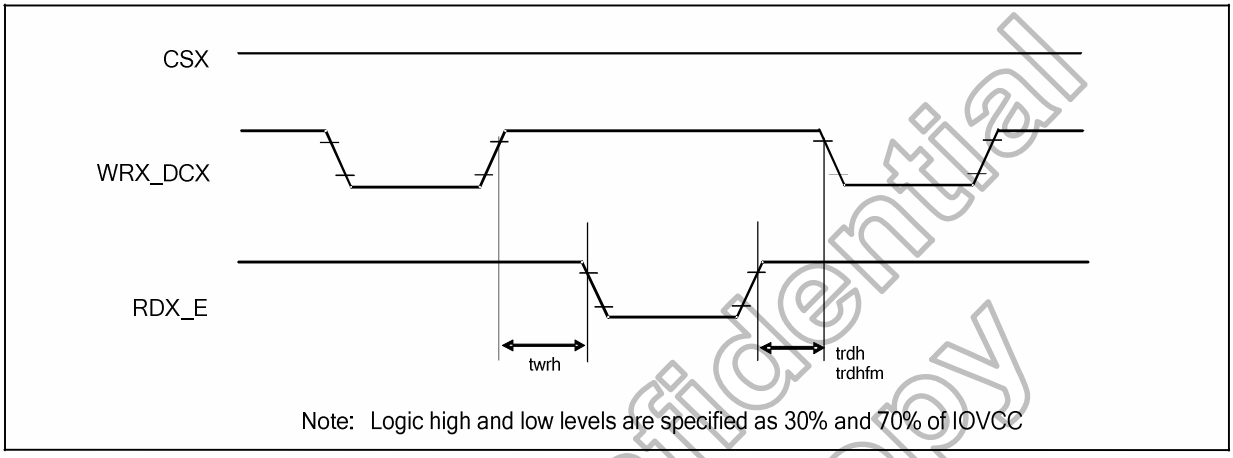


Figure 11. 3 Write to Read and Read to Write Timing

11.4.2 Serial interface characteristics

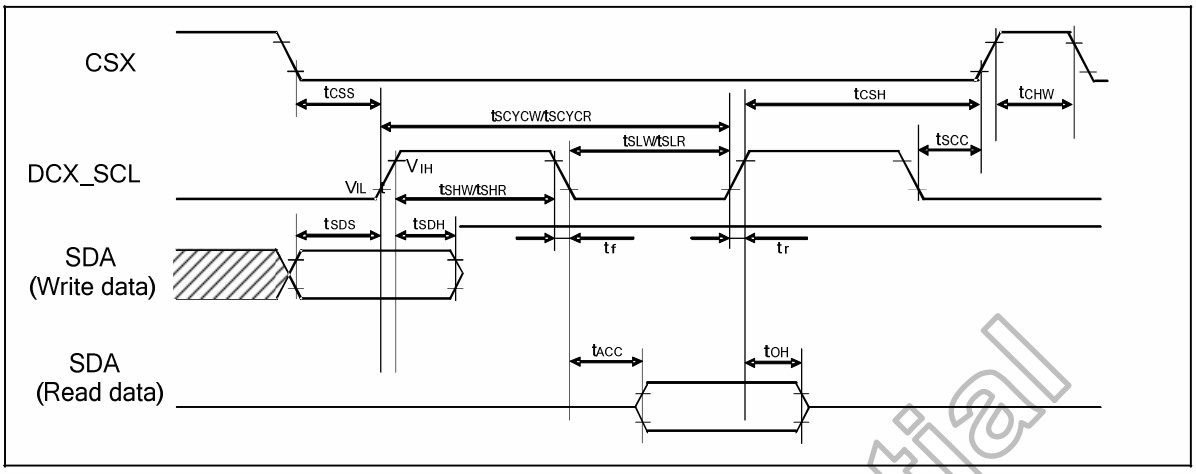
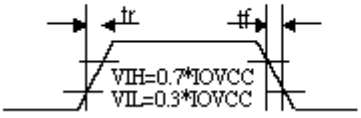


Figure 11. 4 Serial Interface Characteristics

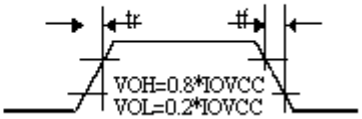
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Serial clock cycle (Write) DCX_SCL "H" pulse width (Write) DCX_SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	DCX_SCL	100 35 35	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDA	30 30	- -	- -	ns
Serial clock cycle (Read) DCX_SCL "H" pulse width (Read) DCX_SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	DCX_SCL	150 60 60	- - -	- - -	ns
Access Time	t_{ACC}	SDA for maximum C_L=30pF For minimum C_L=8pF	45	-	100	ns
Output disable time	t_{OH}	SDA For maximum C_L=30pF For minimum C_L=8pF	15	-	100	ns
DCX_SCL to Chip select	t_{SCC}	DCX_SCL, CSX	15	-	-	ns
CSX "H" pulse width	t_{CHW}	CSX	45	-	-	ns
Chip select setup time Chip select hold time	t_{CSS} t_{CSH}	CSX	60 65	- -	- -	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



Output Signal Slope



11.4.3 RGB interface characteristics

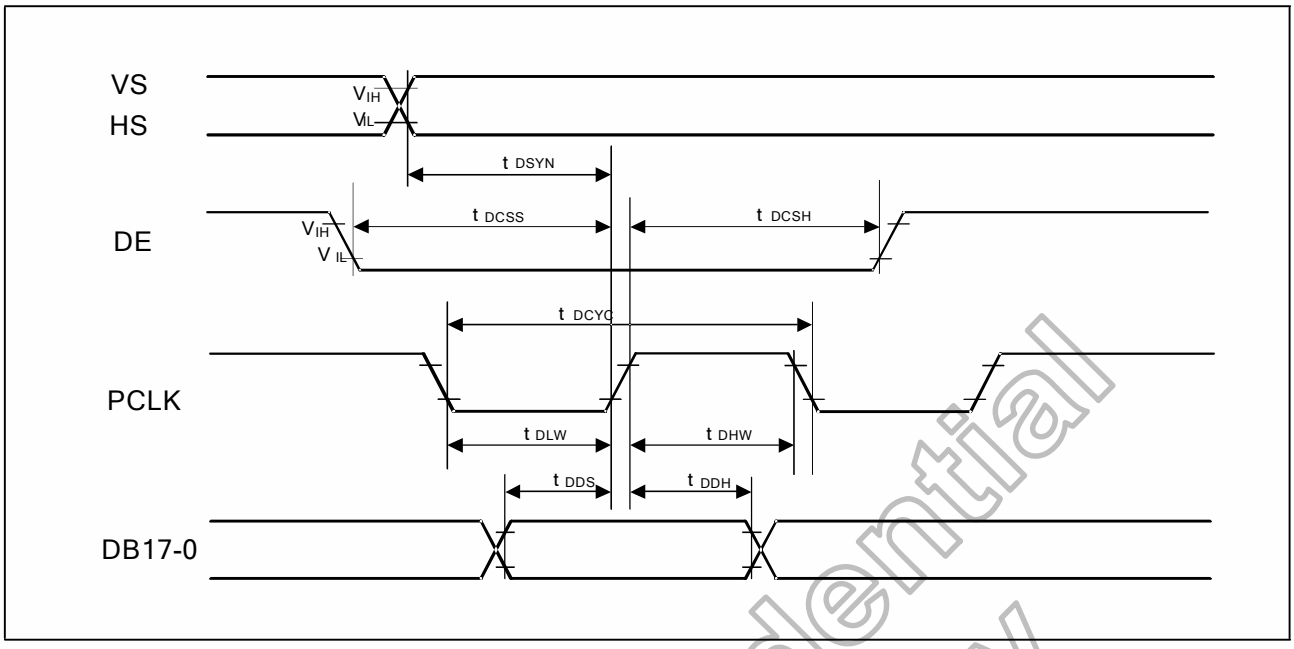
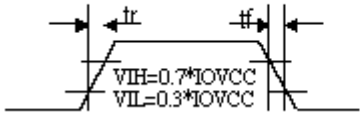


Figure 11. 5 RGB Interface Characteristics

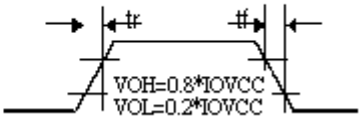
Symbol	Parameter	Conditions	Related Pins	Spec.			Unit
				Min.	Typ.	Max.	
t_{DCYC}	PCLK cycle time	VRR = Min . 50 Hz Max. 65 Hz	PCLK	60(2)	-	226(3)	ns
t_{DLW} t_{CHW}	PCLK Low time PCLK High time			15 15	-	- -	ns
t_{DDS} t_{DDH}	RGB Data setup time RGB Data hold time	-	PCLK, DB17-DB0	15 15	- -	- -	ns
t_{DCSS} t_{DCSH}	DE setup time DE hold Time	-	DE	15 15	-	-	ns
t_{DSYN}	SYNC setup time	-	PCLK, HS, VS	15	-	-	ns

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) 16.6 MHz
(3) 4.4MHz

Input Signal Slope



Output Signal Slope



11.4.4 Reset input timing

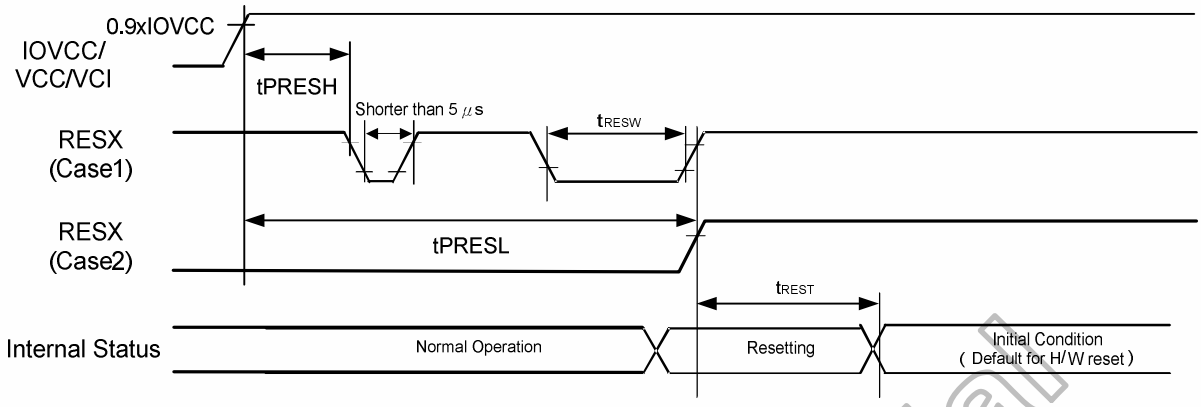


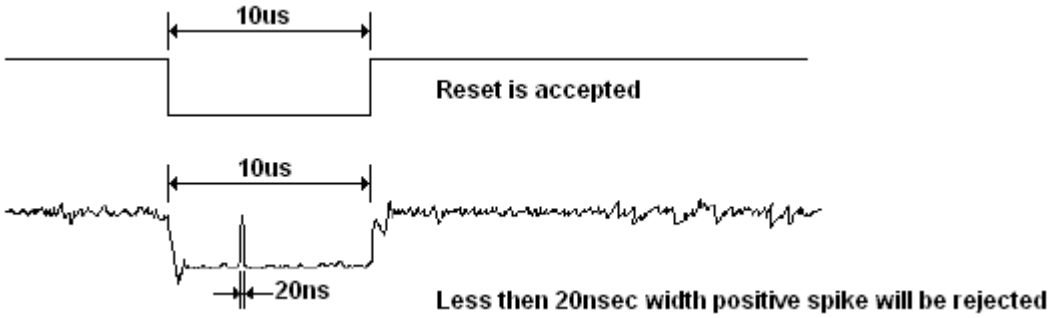
Figure 11. 6 Reset Input Timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	RESX	10	-	-	-	μs
tREST	Reset complete time(2)	-	-	-	10	When reset applied during STB mode	ms
		-		-	120	When reset applied during STB mode	ms
tPRESH	Reset goes high level after Power on time	RESX & IOVCC	1	-	-	Reset goes high level after Power on	ms
tPRESL	Reset goes low level in Power on time	RESX & IOVCC	5			Reset goes low level in Power on	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μ	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) It is necessary to wait 10msec after releasing RESX before sending commands. Also STB Out

11.4.5 MDDI interface characteristics

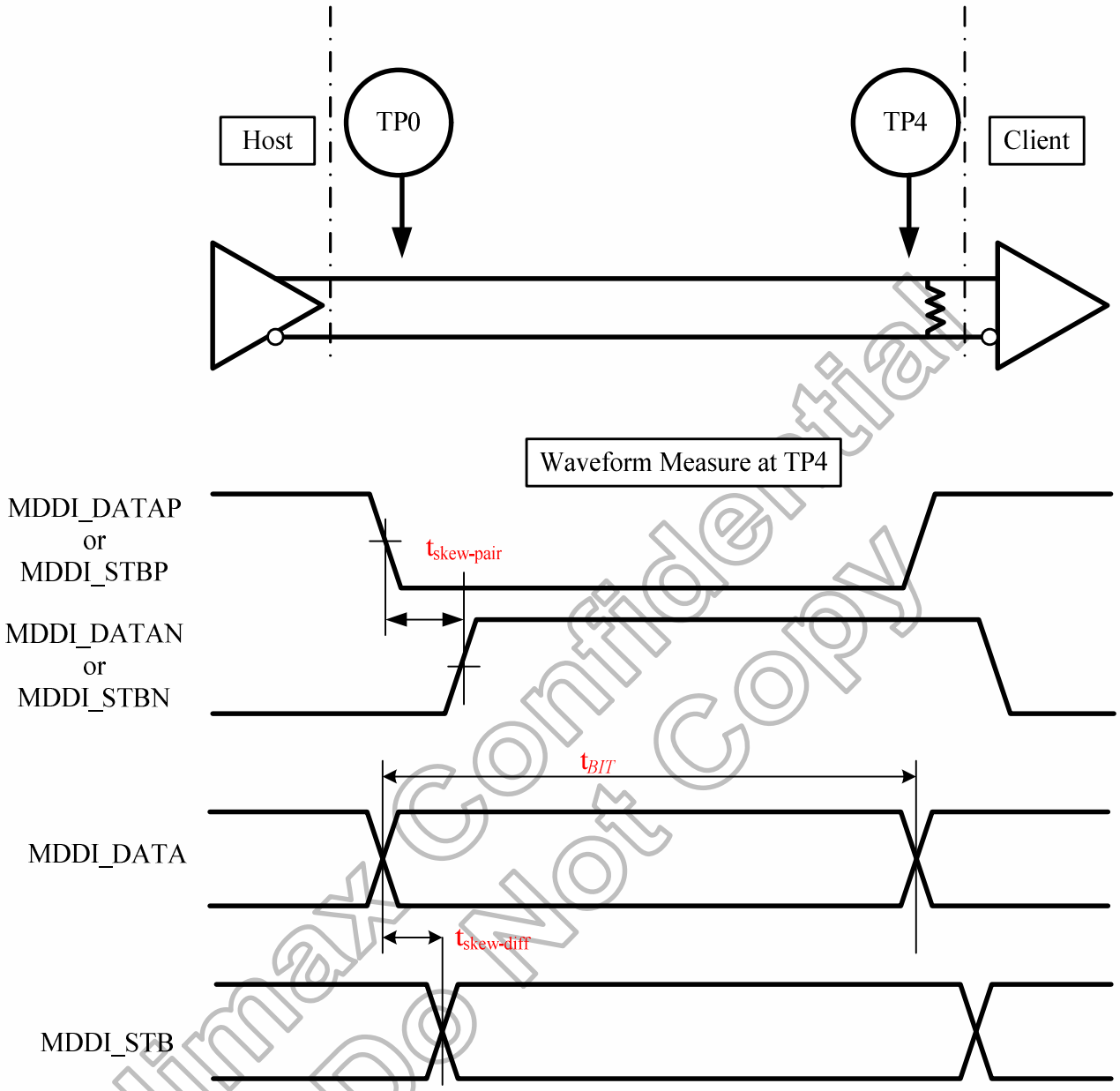


Figure 11. 7 MDDI Interface Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/t_{BIT}$		-	200	TBD	MHz
$t_{skew-pair}$	Skew between positive and negative inputs of the differential receiver of the same differential pair (intra-pair skew)	-0.25	0	0.25	ns
$t_{skew-diff}$	Peak delay skew between one differential pair and any other differential pair	-0.3	0	0.3	ns

12. Ordering Information

Part No.	Package
HX8357-A01000 PDxxx	PD : mean COG xxx : mean chip thickness (μm), (default: 300 μm)

13. Revision History

Version	Date	Description of Changes
01	2008/05/21	New setup
	2008/06/04	1. Update Figure 7.24 Gate Scan Mode.(P.148) 2. Update Memory access control register-SS and GS bit
	2008/06/24	1. Update RTN[3:0] and DUM[7:0] setting value(P.184) 2. Update Figure 5.32 and Figure 5.33 of RGB interface timing.(P52) 3. Update ISC[3:0] setting value(P.180) 4. Update Figure 9.1 Layout Recommendation of HX8357-A. (P.205)
	2008/07/24	1. Modify name.(P.19~P.22, P.205) Original → New PADA0 → PADB0 PADB1 → PADB2 SDI/SDO → SDA 2. Update Power on/off setting up flow.(P.154)
	2008/08/07	1. Modify name.(P.21) Original → New PVSS → VPP 2. Update BT[3:0] setting.(P.173)
	2008/08/25	1. Update HSID_TEST3-1 pin description.(P.19) 2. Add Sections “7.6 System Power On/Off Sequence”.(P149~P.151) 3. Add MDDI DC Characteristic.(P.219) 4. Add MDDI AC Characteristic.(P.225)
	2008/09/11	1. Update Gate pin use state in “4.1 Pin description”.(P.16) 2. Update RADJ setting value.(P.175~P.176)
	2008/10/29	1. Update Table 6.6 GRAM X Address and Display Panel Position.(P.100) 2. Update SMX, SMY pin description.(P.17) 3. Update OTP Programming.(P.216~P.224) 4. Update VRH[5:0] setting table.(P.178) 5. Update MDDI Video stream packet format.(P.65) 6. Update 11.4.4 Reset input timing.(P.231) 7. Add CABC Register5~7, Gain select register 0~8 and Power saving counter 1~4 command.(P.209~P.212)