APPLICATION NOTE

(DOC No. HX8357-A(T)-AN)

HX8357-A

320RGB x 480 dot, 262K color, with internal GRAM, TFT Mobile Single Chip Driver

Preliminary version 01 April, 2009

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http://www.himax.com.tw

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1. Introduction

This document describes HX8357-A is 320RGBx480 dots resolution driving controller. The HX8357-A is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 320RGBx480 dots at maximum.

The HX8357-A can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8357-A also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8357-A supports two interface groups: Command-Parameter interface group, Register-Content interface group. The interface groups are selected by the external pin IFSEL setting. This manual description focuses on Register-Content interface group. About the Command-Parameter interface group, please refer to the HX8357-A(N) application note for detail.

The HX8357-A is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

2. HX8357-A PAD Assignment

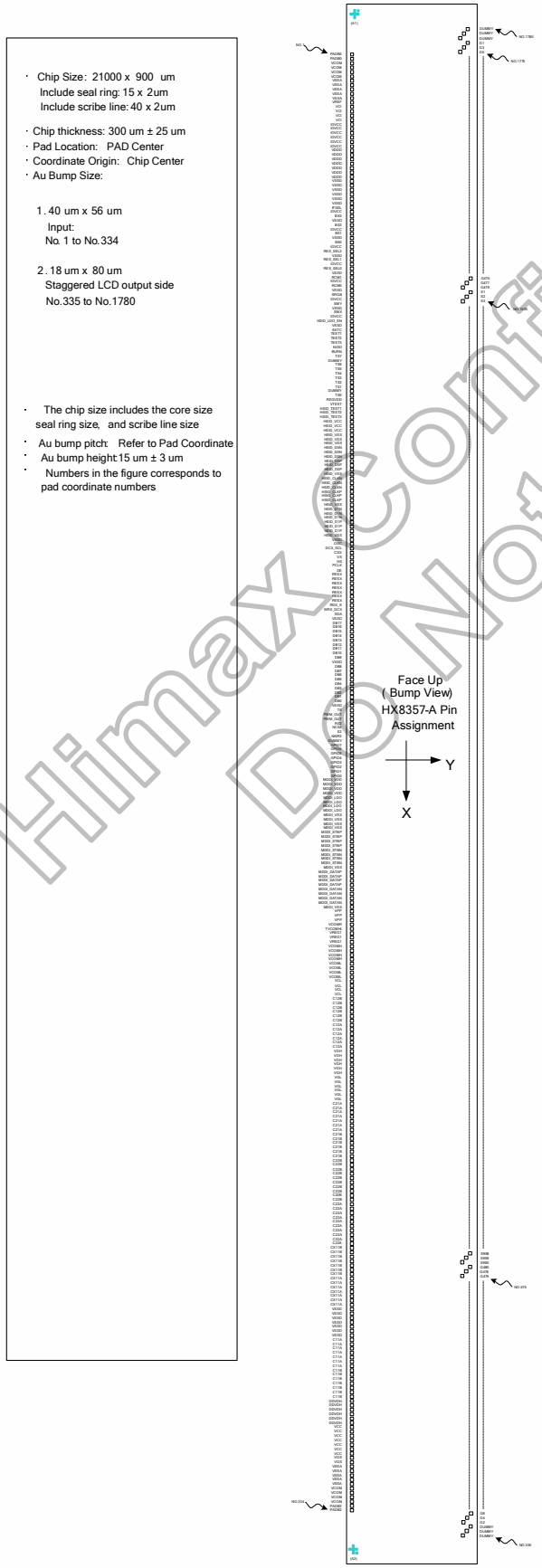
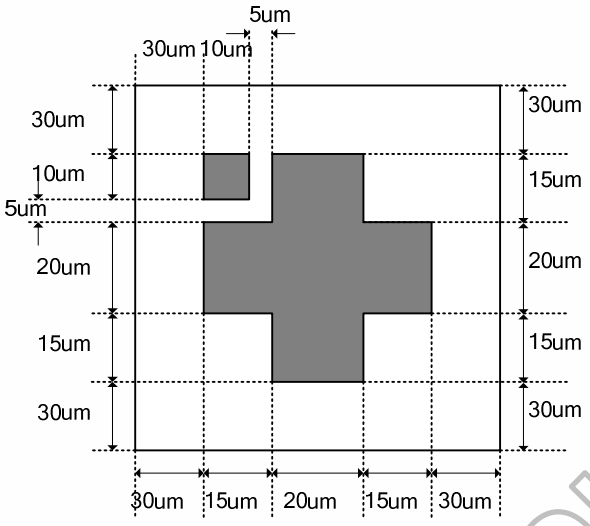


Figure 2.1 HX8357-A pad assignment

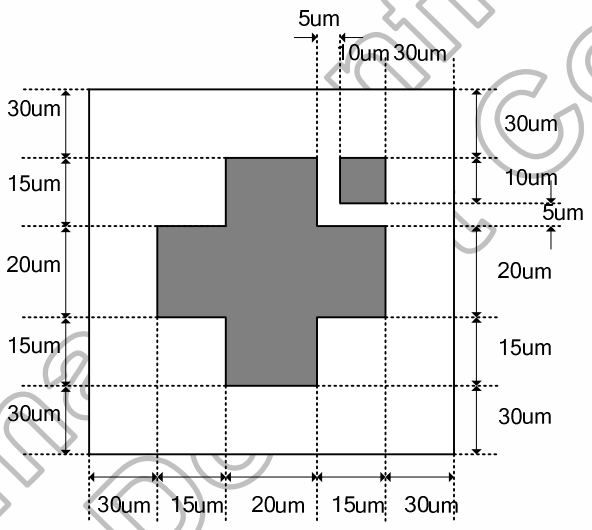
2.1 Alignment mark

A_MARK (A1)



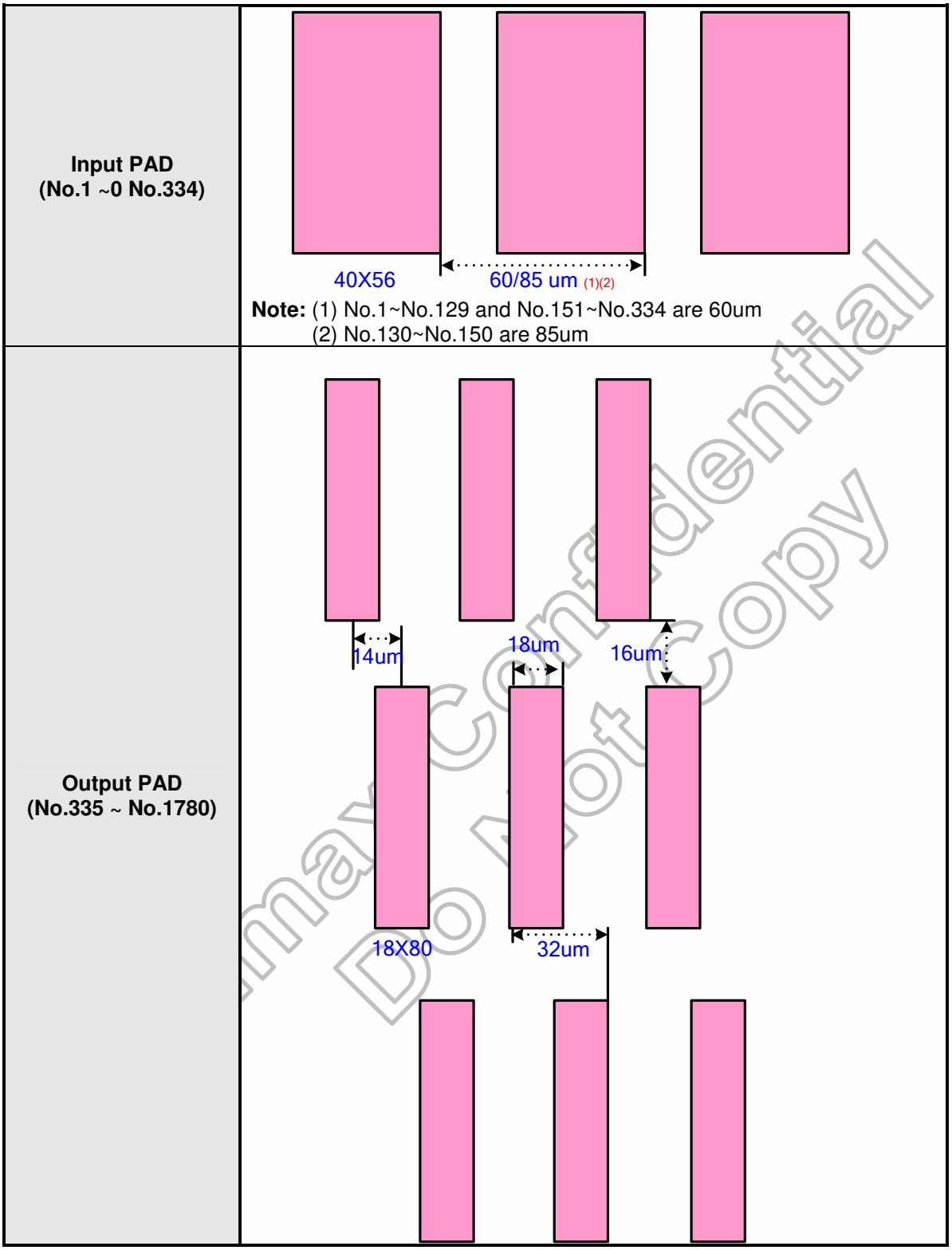
A1(-10390,-340)

A_MARK (A2)



A2 (10390,-340)

2.2 Bump size



3. Pin Description

<table>
<tr><th colspan="5">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>BS3, BS2, BS1, BS0</td><td>I</td><td>4</td><td>VSSD/ IOVCC</td><td>System interface select.
<table>
<tr><th>BS3</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 16-bits Parallel type I</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 8-bits Parallel type I</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-bits Parallel type II</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 8-bits Parallel type II</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>3-wire Serial interface</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>-</td><td>4-wire Serial interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 18-bits Parallel type I</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 9-bits Parallel type I</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bits Parallel type II</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-bits Parallel type II</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>MDDI Interface</td></tr>
</table>
If not used, please fix this pin to IOVCC or VSSD level.</td></tr>
<tr><td>IFSEL</td><td>I</td><td>1</td><td>MPU</td><td>Interface format select pin
<table>
<tr><th>IFSEL</th><th>Interface Format Selection</th></tr>
<tr><td>1</td><td>Command-Parameter interface mode</td></tr>
<tr><td>0</td><td>Register-content interface mode</td></tr>
</table></td></tr>
<tr><td>EXTC</td><td>I</td><td>1</td><td>MPU</td><td>When operate in Register-content interface mode, the EXTC has to be connected to IOVCC or VSSD.</td></tr>
<tr><td>RES_SEL2~0</td><td>I</td><td>3</td><td>MPU</td><td>Panel Resolution select pin.
<table>
<tr><th>RES_SEL2</th><th>RES_SEL1</th><th>RES_SEL0</th><th>Panel Resolution</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>320RGB x 480 dot</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>320RGB x 432 dot</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>320RGB x 426 dot</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>320RGB x 400 dot</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>320RGB x 320 dot</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>320RGB x 240 dot</td></tr>
</table></td></tr>
<tr><td>CSX</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>RESX</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>WRX_DCX</td><td>I</td><td>1</td><td>MPU</td><td>I80 I/F mode: Serves as a write signal and write data at the low level.
M68 I/F mode: 0: Read/Write disable, 1: Read/Write enable.
When under 4-wire SPI interface, it servers as DCX(Data / Command Selection)
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>RDX_E</td><td>I</td><td>1</td><td>MPU</td><td>I80 I/F mode: Serves as a read signal and read data at the low level.
M68 I/F mode: Read/Write disable, 1: Read/Write enable.
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>DCX_SCL</td><td>I</td><td>1</td><td>MPU</td><td>Data / Command Selection pin
When under SPI interface, it servers as SCL (Serial Clock)
If not use, let it open or connected to IOVCC.</td></tr>
<tr><td>BURN</td><td>I</td><td>1</td><td>MPU</td><td>Free Running mode
If BURN=Hi, this can enable free running mode for burn in test.
The display data alternates between full black and full white independent of input data in free running mode. (weak pull low)</td></tr>
<tr><td>VS</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal for RGB I/F mode.
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>HS</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal for RGB I/F mode.
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>PCLK</td><td>I</td><td>1</td><td>MPU</td><td>Pixel clock signal for RGB I/F mode.
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal for RGB I/F mode.
Must be connected to VSSD or IOVCC.</td></tr>
</table>

Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
OSC	I	1	Oscillation Resistor	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.
VCOMR	I	1	Resistor or open	A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VREG1 and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8357-A.
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.
RCM1, RCM0	I	2	MCU	RGB and System interface mode selection pin. **RCM1, RCM0** / **MCU and RGB Interface Mode Select** 0x / System Interface (1) 10 / RGB Interface (1) (VS+HS+DE) 11 / RGB Interface (2) (VS+HS) As internal RCM[1:0] bits are written, the external pin RCM[1:0] control is invalid, and RGB and System interface mode selection is controlled by internal RCM[1:0] bits. **If not used, please fix this pin to GND.**
SRGB	I	1	MCU	RGB direction select H/W pin for Color filter default setting. **SRGB** / **RGB Filter Order for Color Filter Default Setting** 0 / S1, S2, S3 filter order = '**B**', '**G**', '**R**' 1 / S1, S2, S3 filter order = '**R**', '**G**', '**B**' As internal SRGB bits are written, the external pin SRGB control is invalid and the color filter setting will be controlled by SRGB bit. **If not used, please fix this pin to GND.**
SMX	I	1	MCU	Module source output direction H/W select pin. **SMX** / **Module Source Output Direction** 0 / S960 -> **S1** 1 / **S1** -> S960 As internal SS_Panel bits are written, the external pin SMX control is invalid and the color filter setting will be controlled by SS_Panel bit. **If not used, please fix this pin to GND.**
SMY	I	1	MCU	Module Gate output direction H/W select pin. **SMY** / **Module Gate Output Direction** 0 / **G1** -> G480 1 / G480 -> **G1** As internal GS_Panel bits are written, the external pin SMY control is invalid and the color filter setting will be controlled by GS_Panel bit. **If not used, please fix this pin to GND.**

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~S960	O	960	LCD	Output voltages applied to the liquid crystal.
G1~G480	O	480	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open)
VCOM	O	1	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
TE	O	1	MPU	Tearing effect output. If not used, please open this pin.
NISD	O	1	Open	Image Sticking Discharge signal. This pin is used for monitoring image sticking discharge phenomena. When the NISD goes low, the VGL, Source and VCOM would be discharged to VSSA. When the NISD goes high, the VGL, Source and VCOM are normal operation.
PWM_OUT	O	1	LED driver IC	Backlight On/Off control pin. If use ABC function, the pin can connect to external LED driver IC. The output voltage rage = VSSD~ IOVCC.

NWR2	O	1	Sub Panel	80-interface NWR signal output pin for Sub Panel
E2	O	1	Sub Panel	68-interface Enable signal output pin for Sub Panel
NCS2	O	1	Sub Panel	The signal is Chip select for Sub Panel.
RS2	O	1	Sub Panel	The signal is register index or register parameter select for Sub Panel

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B CX11A,CX11B	I/O	4	Step-up Capacitor	Connect to the step-up capacitors according to the step-up 1 factor. Leave this pin open if the internal step-up circuit is not used.
C12A, C12B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	I/O	4	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
DB17~0 (DBS17~0)	I/O	18	MPU	When Operates in MPU interface mode, it is used liked an 18-bit bi-directional data bus. About data bus format, please refer “Table4. 2 Input Bus Format Selection of System Interface Circuit”. When Operation in RGB interface mode, it is an 18-bit bus RGB data bus. About RGB data bus format, please refer “Table 4. 3 RGB interface Bus Width Set Table” If use MDDI interface, these pins are sub panel data bus (DBS17~DBS0). Let unused pins to the open.
SDA	I/O	1	MPU	Serial data input pin and output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal. If not used, please open this pin.
GPIO7~0	I/O	8	-	Standard Input/Output pin As for GPIO7 to 0 terminal, setting of an input and output direction is possible.

High Speed Interface Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
HSID_CLKP, HSID_CLKN	-	2	High speed Host	High Speed Interface clock differential signal input pins
HSID_D0P, HSID_D0N, HSID_D1P, HSID_D1N	-	4	High speed Host	High Speed Interface Data differential signal input pins.
HSID _VCC	P	1	Power supply or Capacitor	Power supply for the High Speed Interface analog power. HSID_VCC = 1.2V ~ 1.3V
HSID _VSS	P	1	Ground	High Speed Interface analog ground. HSID_VSS = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
HSID _LDO_EN	I	1	VSSD/ IOVCC	If HSID _LDO_EN = high, the internal HSID _VCC regulator will be turned on. If HSID _LDO_EN = low, the internal HSID _VCC regulator will be turned off, HSID _VCC should connect to external power supply, the voltage range 1.2V~1.3V. Must be connected to IOVCC or VSSD. (weak pull low)

MDDI Interface Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
MDDI_STBP, MDDI_STBN	-	2	MDDI Host	MDDI Strobe differential signal input pins. STB+ pin for Strobe+, STB- pin for Strobe-. Connect to a terminal resistance (100Ω) between STB+ and STB-. If not used, please let it connected to VSSD.
MDDI_DATAP MDDI_DATAN	-	2	MDDI Host	MDDI Data differential signal input pins. DATA+ pin for Data+, DATA- pin for Data-. Connect to a terminal resistance (100Ω) between DATA+ and DATA-. If not used, please let it connected to VSSD.
MDDI_VDD	P	1	Power Supply	MDDI I/O power supply pin, 2.3V~3.3V.
MDDI_VSS	P	1	Ground	MDDI I/O ground pin.
MDDI_LDO	O	1	Capacitor	MDDI regulator output pin. Connect to a stabilizing capacitor between MDDI_VSS and MDDI_LDO If not used, please open these pins.

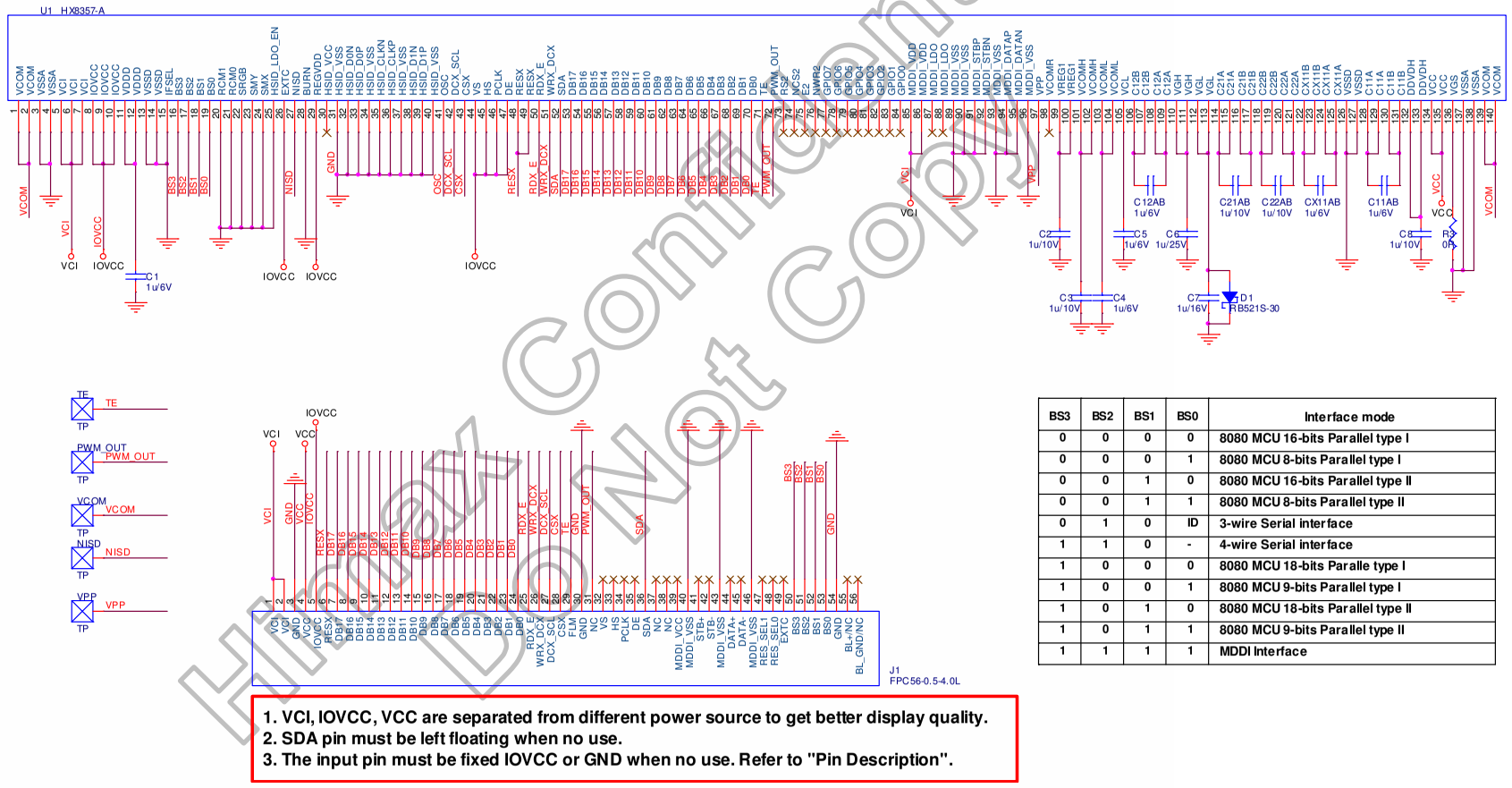
Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	1	Power Supply	IO Pad and Digital power supply, 1.65V~3.3V
VCC	P	1	Power Supply	Analog power supply, 2.3V~3.3V
VCI	P	1	Power Supply	Analog power supply, 2.3V~3.3V
VPP	P	1	Power Supply	Power supply pin used in OTP program mode and operates at 7.5V ．0.2. If not in OTP program mode, please let it open.
VSSD	P	1	Ground	Digital ground
VSSA	P	1	Ground	Analog ground
VDDD	O	1	Stabilizing Capacitor	Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor
REGVDD	I	1	VSSD/ IOVCC	If REGVDD = high, the internal VDDD regulator will be turned on. If REGVDD = low, the internal VDDD regulator will be turned off, VDDD should connect to external power supply, the voltage range 1.65~1.95V. Must be connected to IOVCC or VSSD. (weak pull high)
VREG1	P	1	Stabilizing Capacitor	Internal generated stable power for source driver unit.
VREF	O	1	Open	Internal reference voltage output pin, please open this pin.
VCOMH	P	1	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	P	1	Stabilizing capacitor	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.
VCL	P	1	Stabilizing capacitor	A negative voltage for VCOML circuit, VCL=-VCI
DDVDH	P	1	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH.
VGH	P	1	Stabilizing capacitor	An output from the step-up circuit2.or 4 ~ 6 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGH.
VGL	P	1	Stabilizing capacitor	An output from the step-up circuit2.or –3~ -5 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGL. Place a schottkey barrier diode between VSSD and VGL. Place a schottkey barrier diode (see “configuration of the power supply”).

Test Pin and Others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST3-1	I	3	GND	Test pin input (Internal pull low)
HSID_TEST3-1	-	3	Open	A test pin. Disconnect it.
TS7~0	O	8	Open	A test pin. Disconnect it.
VTEST	O	1	Open	A test pin. Disconnect it.
TVCOMHI	O	8	Open	A test pin. Disconnect it.
PADB0	I	2	Open	A test pin. Available for measuring the COG contact resistance. PADB0 are short-circuited within the chip.
PADB2	I	2	Open	A test pin. Available for measuring the COG contact resistance. PADB2 are short-circuited within the chip.

4. HX8357-A Reference FPC circuit

4.1 Reference FPC circuit for CMO's F03002-01U panel

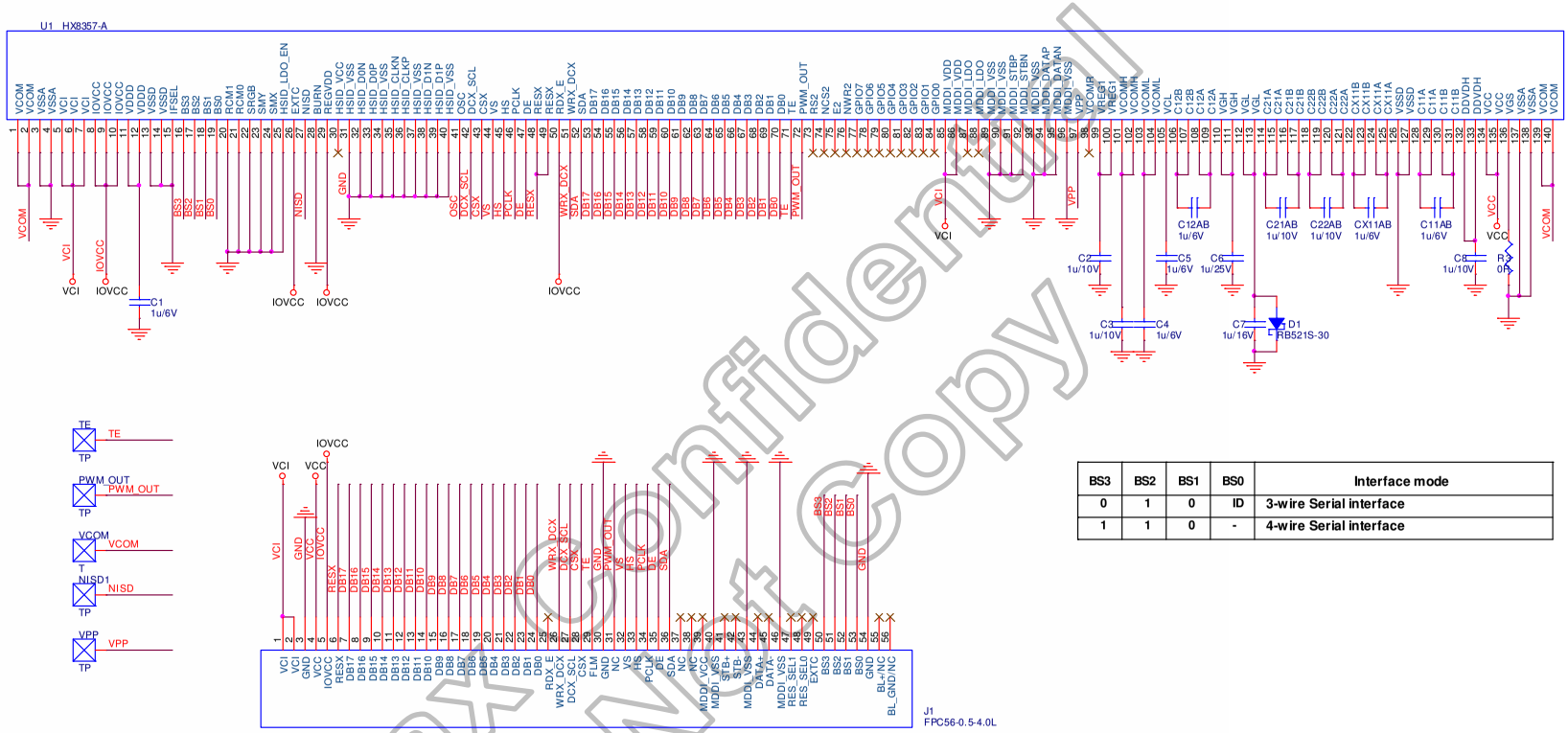
4.1.1 MPU mode reference FPC circuit for CMO's F03002-01U panel



BS3	BS2	BS1	BS0	Interface mode
0	0	0	0	8080 MCU 16-bits Parallel type I
0	0	0	1	8080 MCU 8-bits Parallel type I
0	0	1	0	8080 MCU 16-bits Parallel type II
0	0	1	1	8080 MCU 8-bits Parallel type II
0	1	0	ID	3-wire Serial interface
1	1	0	-	4-wire Serial interface
1	0	0	0	8080 MCU 18-bits Paralle type I
1	0	0	1	8080 MCU 9-bits Parallel type I
1	0	1	0	8080 MCU 18-bits Parallel type II
1	0	1	1	8080 MCU 9-bits Parallel type II
1	1	1	1	MDDI Interface

Figure 4.1 MPU mode Reference FPC Circuit for CMO's F03002-01U panel

4.1.2 RGB+SPI mode reference FPC circuit for CMO's F03002-01U panel



BS3	BS2	BS1	BS0	Interface mode
0	1	0	ID	3-wire Serial interface
1	1	0	-	4-wire Serial interface

1. VCI, IOVCC, VCC are separated from different power source to get better display quality.
2. SDA pin must be left floating when no use.
3. The input pin must be fixed IOVCC or GND when no use. Refer to "Pin Description".

Figure 4.2 RGB+SPI mode Reference FPC Circuit for CMO's F03002-01U panel

4.1.3 MDDI mode reference FPC circuit for CMO's F03002-01U panel

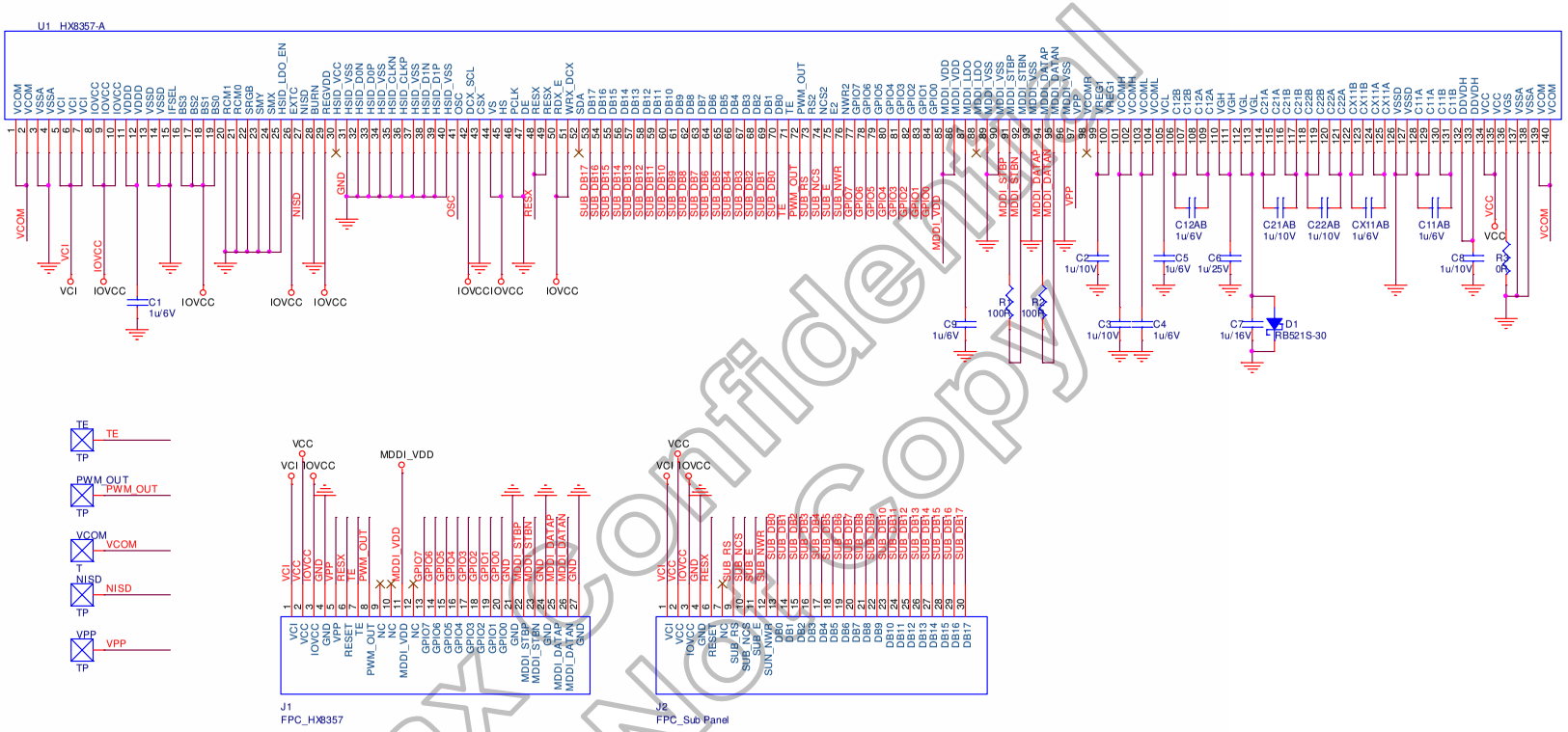
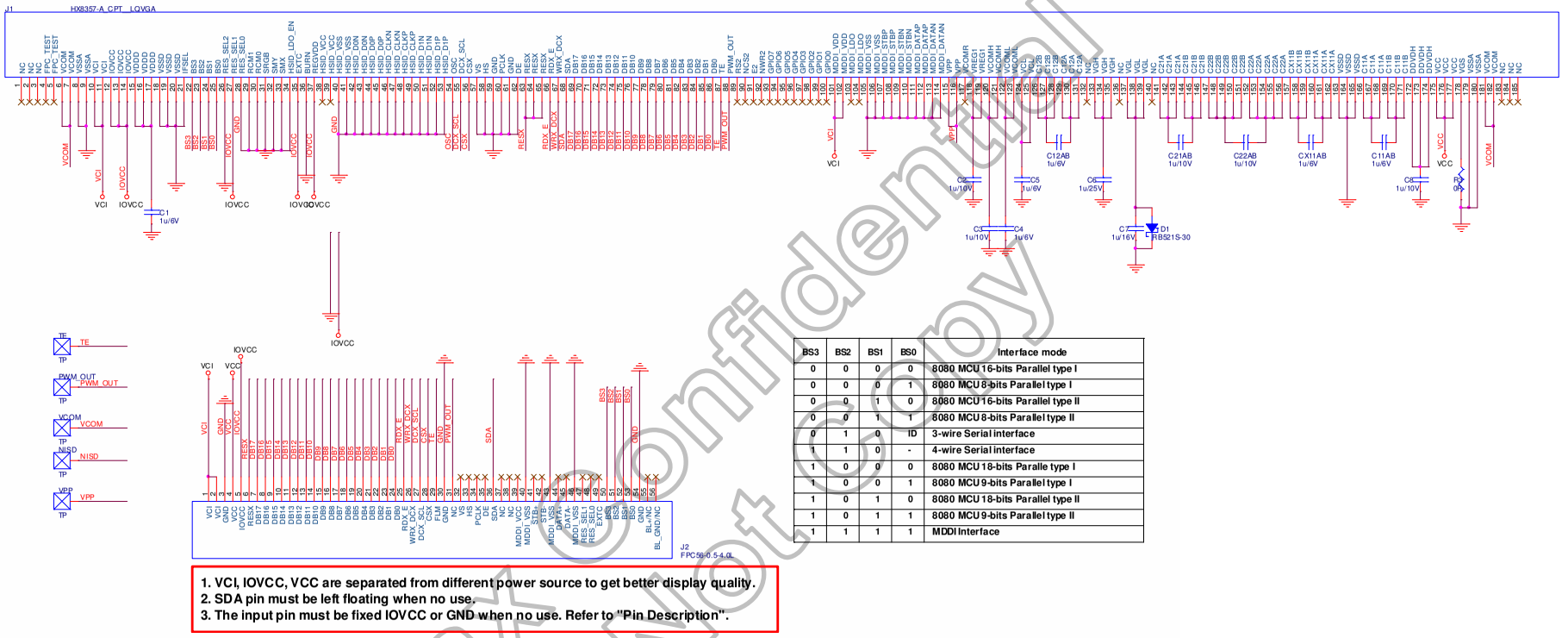


Figure 4.3 MDDI mode Reference FPC Circuit for CMO's F03002-01U panel

4.1.4 MPU mode reference FPC circuit for WINTEK's WK-FHE47C panel

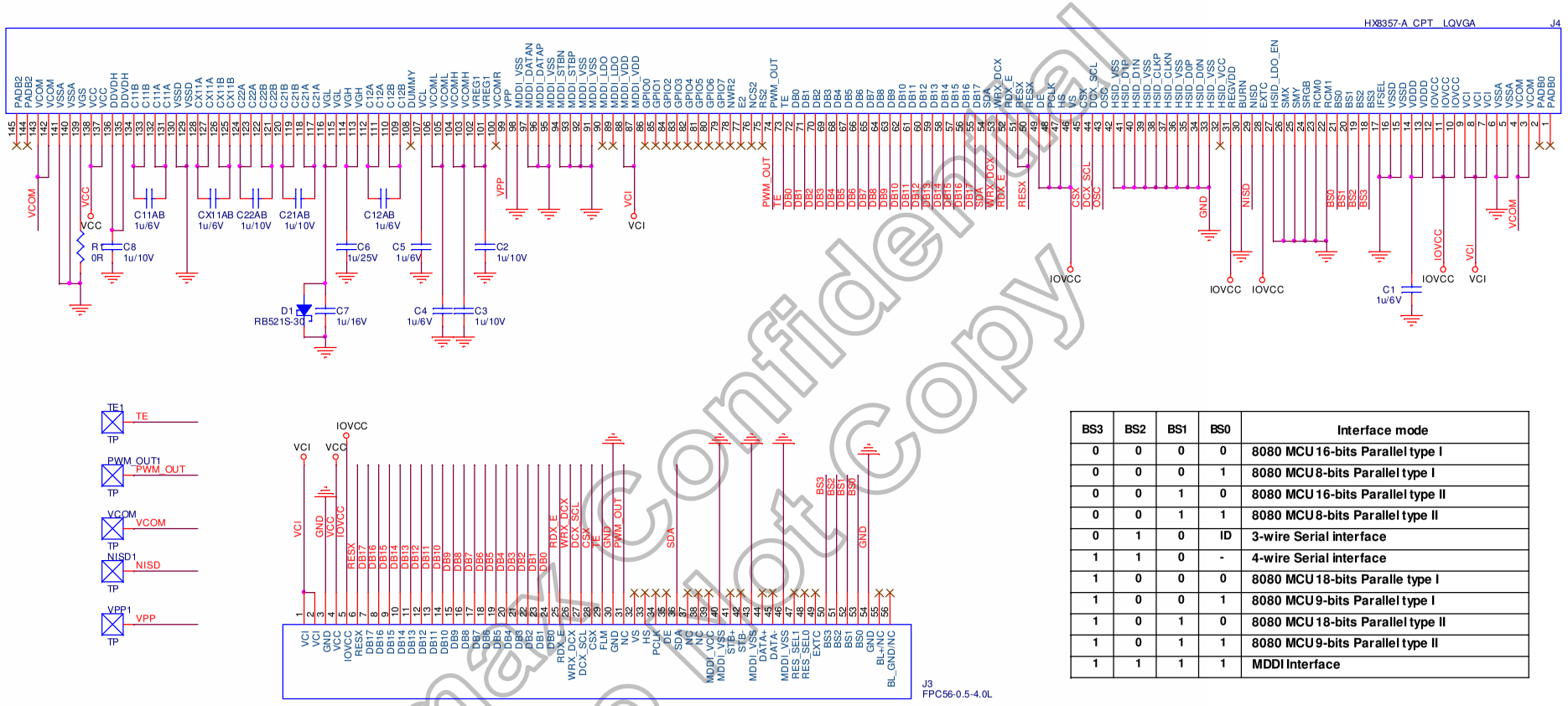


BS3	BS2	BS1	BS0	Interface mode
0	0	0	0	8080 MCU 16-bits Parallel type I
0	0	0	1	8080 MCU 8-bits Parallel type I
0	0	1	0	8080 MCU 16-bits Parallel type II
0	0	1	1	8080 MCU 8-bits Parallel type II
0	1	0	ID	3-wire Serial interface
1	1	0	-	4-wire Serial interface
1	0	0	0	8080 MCU 18-bits Paralle type I
1	0	0	1	8080 MCU 9-bits Parallel type I
1	0	1	0	8080 MCU 18-bits Parallel type II
1	0	1	1	8080 MCU 9-bits Parallel type II
1	1	1	1	MDDI Interface

1. VCI, IOVCC, VCC are separated from different power source to get better display quality.
2. SDA pin must be left floating when no use.
3. The input pin must be fixed IOVCC or GND when no use. Refer to "Pin Description".

Figure 4.4 MPU mode Reference FPC Circuit for WINTEK's WK-FHE47C panel

4.1.5 MPU mode reference FPC circuit for CPT's 024GP21 panel



BS3	BS2	BS1	BS0	Interface mode
0	0	0	0	8080 MCU 16-bits Parallel type I
0	0	0	1	8080 MCU 8-bits Parallel type I
0	0	1	0	8080 MCU 16-bits Parallel type II
0	0	1	1	8080 MCU 8-bits Parallel type II
0	1	0	ID	3-wire Serial interface
1	1	0	-	4-wire Serial interface
1	0	0	0	8080 MCU 18-bits Paralle type I
1	0	0	1	8080 MCU 9-bits Parallel type I
1	0	1	0	8080 MCU 18-bits Parallel type II
1	0	1	1	8080 MCU 9-bits Parallel type II
1	1	1	1	MDDI Interface

1. VCI, IOVCC, VCC are separated from different power source to get better display quality.
2. SDA pin must be left floating when no use.
3. The input pin must be fixed IOVCC or GND when no use. Refer to "Pin Description".

Figure 4.5 MPU mode Reference FPC Circuit for CPT's panel

4.2 The specification of FPC circuit and pins connection is shown as following table

Capacitor	Recommended voltage	Capacity
C1 (VDDD-VSSA)	6V	1 µF (B characteristics)
C2 (VREG1-VSSA)	10V	1 µF (B characteristics)
C3 (VCOMH-VSSA)	10V	1 µF (B characteristics)
C4 (VCOML-VSSA)	6V	1 µF (B characteristics)
C5 (VCL-VSSA)	6V	1 µF (B characteristics)
C6(VGH-VSSA)	25V	1 µF (B characteristics)
C7 (VGL-VSSA)	16V	1 µF (B characteristics)
C8 (VDDVDH-VSSA)	10V	1 µF (B characteristics)
C9 (MDDI_LDO-MDDI_VSS)	6V	1 µF (B characteristics)
C11AB (C11A/B)	6V	1 µF (B characteristics)
CX11AB (CX11A/B)	6V	1 µF (B characteristics)
C12AB (C12A/B)	6V	1 µF (B characteristics)
C21AB (C21A/B)	10V	1 µF (B characteristics)
C22AB (C22A/B)	10V	1 µF (B characteristics)
D1 (VGL-VSSA)	Schottky Diode	VF < 0.4V / 20mA at 25℃, VR ≥30V (Recommended diode: RB521S-30)
R1, R2	Resistor	100Ω
R3	Resistor	0Ω

Note: (1) If not use MDDI I/F, the C19, R1, R2 can remove.

Table 4.1 Connected Capacitor

4.3 Input Bus Format Selection of System Interface Circuit

BS3	BS2	BS1	BS0	Interface	WRX_DCX	DCX_SCL	Data Bus use	
							Register/ Content	GRAM
0	0	0	0	8080 MCU 16-bits Parallel type I	WRX	DCX	DB7-DB0	DB15-DB0: 16-bit data
0	0	0	1	8080 MCU 8-bits Parallel type I	WRX	DCX	DB7-DB0	DB7-DB0: 8-bits Data
0	0	1	0	8080 MCU 16-bits Parallel type II	WRX	DCX	DB8-DB1	DB17-DB10, DB8-DB1: 16-bit data
0	0	1	1	8080 MCU 8-bits Parallel type II	WRX	DCX	DB17-DB10	DB17-DB10: 8-bits Data
0	1	0	ID	3-wire Serial interface	x	SCL	SDA	
1	1	0	-	4-wire Serial interface	DCX	SCL	SDA	
1	0	0	0	8080 MCU 18-bits Parallel type I	WRX	DCX	DB7-DB0	DB17-DB0: 18-bits Data
1	0	0	1	8080 MCU 9-bits Parallel type I	WRX	DCX	DB7-DB0	DB8-DB0: 9-bits Data
1	0	1	0	8080 MCU 18-bits Parallel type II	WRX	DCX	DB8-DB1	DB17-DB0: 18-bits Data
1	0	1	1	8080 MCU 9-bits Parallel type II	WRX	DCX	DB17-DB10	DB17-DB9: 9-bits Data
1	1	1	1	MDDI Interface	x	x	MDDI	MDDI
Other Setting				Setting Invalid				

Table 4.2 Input Bus Format Selection of System Interface Circuit

4.4 RGB Interface Bus Width Set Table

17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
50h	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	16-bits data
60h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bits data
17H	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus width
E0h	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	6-bits data
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note: (1) When 17H=”E0h”, 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
(2) Only 17H= “50h”,”60h”, “E0h” are valid on RGB I/F, Others are invalid.
(3) ‘x’ don’t care, but need to set IOVCC or VSSD level.

Table 4.3 RGB Interface Bus Width Set Table

5. Initial Code For Reference

5.1 The reference setting of normal display

5.1.1 The reference setting of normal display for CMO's Panel(for MPU mode)

```
Void HX8357-A_CMO_F03002-01U_initial_code(void)
{
// SUB_SEL for HX8357-A in use MDDI I/F
//Add the two setting below while using MDDI I/F
        Set_LCD_8B_REG(0xFF,0x00); // Command page 0
        Set_LCD_8B_REG(0x72,0xF6); // SUB_SEL=0xF6

// Power saving for HX8357-A
        Set_LCD_8B_REG(0xFF,0x00); // Command page 0
        Set_LCD_8B_REG(0xF2,0x00); // GENON=0x00
        Set_LCD_8B_REG(0xE4,0x00); // EQVCI_M1=0x00
        Set_LCD_8B_REG(0xE5,0x1C); // EQGND_M1=0x1C
        Set_LCD_8B_REG(0xE6,0x00); // EQVCI_M0=0x1C
        Set_LCD_8B_REG(0xE7,0x1C); // EQGND_M0=0x1C
        Set_LCD_8B_REG(0xEE,0x42); // For GRAM read/write speed
        Set_LCD_8B_REG(0xEF,0xDB); // For GRAM read/write speed
        Set_LCD_8B_REG(0x2E,0x98); //For Gate timing, prevent the display abnormal in RGB I/F

// Gamma
        Set_LCD_8B_REG(0x40,0x07);
        Set_LCD_8B_REG(0x41,0x2E);
        Set_LCD_8B_REG(0x42,0x2C);
        Set_LCD_8B_REG(0x43,0x3D);
        Set_LCD_8B_REG(0x44,0x38);
        Set_LCD_8B_REG(0x45,0x3D);
        Set_LCD_8B_REG(0x46,0x27);
        Set_LCD_8B_REG(0x47,0x76);
        Set_LCD_8B_REG(0x48,0x08);
        Set_LCD_8B_REG(0x49,0x06);
        Set_LCD_8B_REG(0x4A,0x06);
        Set_LCD_8B_REG(0x4B,0x0C);
        Set_LCD_8B_REG(0x4C,0x17);

        Set_LCD_8B_REG(0x50,0x02);
        Set_LCD_8B_REG(0x51,0x07);
        Set_LCD_8B_REG(0x52,0x02);
        Set_LCD_8B_REG(0x53,0x13);
        Set_LCD_8B_REG(0x54,0x11);
        Set_LCD_8B_REG(0x55,0x3D);
        Set_LCD_8B_REG(0x56,0x09);
        Set_LCD_8B_REG(0x57,0x58);
        Set_LCD_8B_REG(0x58,0x08);
        Set_LCD_8B_REG(0x59,0x13);
        Set_LCD_8B_REG(0x5A,0x19);
        Set_LCD_8B_REG(0x5B,0x19);
        Set_LCD_8B_REG(0x5C,0x17);
        Set_LCD_8B_REG(0x5D,0x3C);

// Set GRAM area 320x480
        Set_LCD_8B_REG(0x02,0x00);
        Set_LCD_8B_REG(0x03,0x00);
        Set_LCD_8B_REG(0x04,0x01);
        Set_LCD_8B_REG(0x05,0x3F);
        Set_LCD_8B_REG(0x06,0x00);
```

```
        Set_LCD_8B_REG(0x07,0x00);
        Set_LCD_8B_REG(0x08,0x01);
        Set_LCD_8B_REG(0x09,0xDF);

// Power Setting
        Set_LCD_8B_REG(0x24,0x64); // Set VCOMH voltage, VHH=0x64
        Set_LCD_8B_REG(0x25,0x71); // Set VCOML voltage, VML=0x71
        Set_LCD_8B_REG(0x23,0x52); // Set VCOM offset, VMF=0x52
        Set_LCD_8B_REG(0x1B,0x1E);// Set VERG1 voltage, VRH[5:0]=0x1E
        Set_LCD_8B_REG(0x1D,0x11);// FS0[1:0]=01, Set the operating frequency of the step-up circuit 1

// Power on Setting
        Set_LCD_8B_REG(0x19,0x01); // OSC_EN=1, Start to Oscillate
        Set_LCD_8B_REG(0x1C,0x03);// AP=011
        Set_LCD_8B_REG(0x01,0x00); // Normal display(Exit Deep standby mode)
        Set_LCD_8B_REG(0x1F,0x80); // Exit standby mode and Step-up circuit 1 enable
        // GAS_EN=1, VCOMG=0, PON=0, DK=0, XDK=0, DDVDH_TRI=0, STB=0
        DelayX1ms(5);

        Set_LCD_8B_REG(0x1F,0x90); // Step-up circuit 2 enable
        // GAS_EN=1, VCOMG=0, PON=1, DK=0, XDK=0, DDVDH_TRI=0, STB=0
        DelayX1ms(5);

        Set_LCD_8B_REG(0x1F,0xD4);
        // GAS_EN=1, VCOMG=1, PON=1, DK=0, XDK=1, DDVDH_TRI=0, STB=0
        DelayX1ms(5);

// Display ON Setting
        Set_LCD_8B_REG(0x28,0x08); // GON=0, DTE=0, D[1:0]=01
        DelayX1ms(40);
        Set_LCD_8B_REG(0x28,0x38); // GON=1, DTE=1, D[1:0]=10
        DelayX1ms(40);
        Set_LCD_8B_REG(0x28,0x3C);// GON=1, DTE=1, D[1:0]=11

        Set_LCD_8B_REG(0x17,0x06); // 18-bit/pixel

        HX8357-A_Update_GRAM();
}
```

5.2 The reference setting of Display OFF

```
Void HX8357-A_Display-OFF_code(void)
{

    Set_LCD_8B_REG(0xFF,0x00);     //Select Command Page 0

// Display OFF Setting
    Set_LCD_8B_REG(0x28,0x38);     //GON=1, DTE=1, D[1:0]=10
    DelayX1ms(40);

    Set_LCD_8B_REG(0x28,0x24);     //GON=1, DTE=0, D[1:0]=01
    DelayX1ms(40);

    Set_LCD_8B_REG(0x28,0x04);     //GON=0, DTE=0, D[1:0]=01

}
```

5.3 The reference setting of Enter Standby mode

```
Void HX8357-A_Enter-Standby_code(void)
{
    Set_LCD_8B_REG(0xFF,0x00); //Select Command Page 0

// Display off Setting
    Set_LCD_8B_REG(0x28,0x38);    // GON=1, DTE=1, D[1:0]=10
    DelayX1ms(40);
    Set_LCD_8B_REG(0x28,0x04);    // GON=0, DTE=0, D[1:0]=01

// Power off Setting
    Set_LCD_8B_REG(0x1F,0x90);    // Stop VCOMG
    // GAS_EN=1, VCOMG=0, PON=1, DK=0, XDK=0, DDVDH_TRI=0, STB=0
    DelayX1ms(5);

    Set_LCD_8B_REG(0x1F,0x88);    // Stop step-up circuit
    // GAS_EN=1, VCOMG=1, PON=0, DK=1, XDK=1, DDVDH_TRI=0, STB=0
    Set_LCD_8B_REG(0x1C,0x00);    // AP=000

    Set_LCD_8B_REG(0x1F,0x89);    // Enter Standby mode
    //GAS_EN=1, VCOMG=0, PON=0, DK=1, XDK=0, DDVDH_TRI=0, STB=1
    Set_LCD_8B_REG(0x19,0x00); //OSC_EN=0, Stop to Oscillate
}
```

5.4 The reference setting of Exit Standby mode

```
Void HX8357-A_Exit_Standby_code(void)
{
    Set_LCD_8B_REG(0xFF,0x00); //Select Command Page 0

    Set_LCD_8B_REG(0x19,0x01); //OSC_EN=1, Start to Oscillate
    DelayX1ms(5);

    Set_LCD_8B_REG(0x1F,0x88);
    //GAS_EN=1, VCOMG=0, PON=0, DK=1, XDK=0, DDVDH_TRI=0, STB=0

// Power on Setting
    Set_LCD_8B_REG(0x1C,0x03);    // AP=011
    Set_LCD_8B_REG(0x1F,0x80);    // Exit standby mode and Step-up circuit 1 enable
    // GAS_EN=1, VCOMG=0, PON=0, DK=0, XDK=0, DDVDH_TRI=0, STB=0
    DelayX1ms(5);

    Set_LCD_8B_REG(0x1F,0x90);    // Step-up circuit 2 enable
    // GAS_EN=1, VCOMG=0, PON=1, DK=0, XDK=0, DDVDH_TRI=0, STB=0
    DelayX1ms(5);

    Set_LCD_8B_REG(0x1F,0xD4);
    // GAS_EN=1, VCOMG=1, PON=1, DK=0, XDK=1, DDVDH_TRI=0, STB=0
    DelayX1ms(5);

// Display on Setting
    Set_LCD_8B_REG(0x28,0x08);    // GON=0, DTE=0, D[1:0]=01
    DelayX1ms(40);
    Set_LCD_8B_REG(0x28,0x38);    // GON=1, DTE=1, D[1:0]=10
    DelayX1ms(40);
    Set_LCD_8B_REG(0x28,0x3C);    // GON=1, DTE=1, D[1:0]=11
}
```

5.5 The reference setting of Enter Deep-Standby mode

```
Void HX8357-A_Enter-Standby_code(void)
{
    Set_LCD_8B_REG(0xFF,0x00); //Select Command Page 0
// Display off Setting
    Set_LCD_8B_REG(0x28,0x38);    // GON=1, DTE=1, D[1:0]=10
    DelayX1ms(40);
    Set_LCD_8B_REG(0x28,0x04);    // GON=0, DTE=0, D[1:0]=01

// Power off Setting
    Set_LCD_8B_REG(0x1F,0x90);    // Stop VCOMG
    // GAS_EN=1, VCOMG=0, PON=1, DK=0, XDK=0, DDVDH_TRI=0, STB=0
    DelayX1ms(5);

    Set_LCD_8B_REG(0x1F,0x88);    // Stop step-up circuit
    // GAS_EN=1, VCOMG=1, PON=0, DK=1, XDK=1, DDVDH_TRI=0, STB=0
    Set_LCD_8B_REG(0x1C,0x00);    // AP=000

    Set_LCD_8B_REG(0x1F,0x89);    // Enter Standby mode
    //GAS_EN=1, VCOMG=0, PON=0, DK=1, XDK=0, DDVDH_TRI=0, STB=1
    Set_LCD_8B_REG(0x01,0xC0); //DP_STB[1:0]=11, Enter deep standby mode.
    Set_LCD_8B_REG(0x19,0x00); //OSC_EN=0, Stop to Oscillate
}
```

5.6 The reference setting of Exit Deep-Standby mode

```
Void HX8357-A_Exit_Deep-Standby_code(void)
{
    Set_LCD_8B_REG(0xFF,0x00); //Select Command Page 0

    Set_LCD_8B_REG(0x19,0x01); //OSC_EN=0, Start to Oscillate
    DelayX1ms(5);

    Set_LCD_8B_REG(0x01,0x00); //DP_STB=0, Exit deep standby mode.

// Power on Setting
    Set_LCD_8B_REG(0x1C,0x03);    // AP=011
    Set_LCD_8B_REG(0x1F,0x80);    // Exit standby mode and Step-up circuit 1 enable
    // GAS_EN=1, VCOMG=0, PON=0, DK=0, XDK=0, DDVDH_TRI=0, STB=0
    DelayX1ms(5);

    Set_LCD_8B_REG(0x1F,0x90);    // Step-up circuit 2 enable
    // GAS_EN=1, VCOMG=0, PON=1, DK=0, XDK=0, DDVDH_TRI=0, STB=0
    DelayX1ms(5);

    Set_LCD_8B_REG(0x1F,0xD4);
    // GAS_EN=1, VCOMG=1, PON=1, DK=0, XDK=1, DDVDH_TRI=0, STB=0
    DelayX1ms(5);

// Display ON Setting
    Set_LCD_8B_REG(0x28,0x08);    // GON=0, DTE=0, D[1:0]=01
    DelayX1ms(40);
    Set_LCD_8B_REG(0x28,0x38);    // GON=1, DTE=1, D[1:0]=10
    DelayX1ms(40);
    Set_LCD_8B_REG(0x28,0x3C);    // GON=1, DTE=1, D[1:0]=11
}
```

5.7 The reference setting of write display data to GRAM

```
Void HX8357-A_Update_GRAM(void)
{
// Set GRAM start address (0x0000, 0x0000)
    Set_LCD_8B_REG(0xFF,0x00); //Select Command Page 0
    // If command page not change, the RFFh can remove

    Set_LCD_8B_REG(0x80,0x00); // Set CAC=0x0000
    Set_LCD_8B_REG(0x81,0x00);
    Set_LCD_8B_REG(0x82,0x00); // Set RAC=0x0000
    Set_LCD_8B_REG(0x83,0x00);
    WR_8B_FORMAT(0x22); //Write GRAM command

    /* Please send 320 x 480 pixels data for CMO Panel*/
    /* Please send 320 x 480 pixels data for WINTEK & CPT Panel*/

}
```

5.8 The reference setting of normal display for Wintek's Panel(for MPU mode)

```
Void HX8357-A_Wintek_FHE47C_initial_code(void)
{
// SUB_SEL for HX8357-A in use MDDI I/F
//Add the two setting below while using MDDI I/F
        Set_LCD_8B_REG(0xFF,0x00); // Command page 0
        Set_LCD_8B_REG(0x72,0xF6); // SUB_SEL=0xF6

// Power saving for HX8357-A
        Set_LCD_8B_REG(0xFF,0x00); // Command page 0
        Set_LCD_8B_REG(0xF2,0x00); // GENON=0x00
        Set_LCD_8B_REG(0xE4,0x00); // EQVCI_M1=0x00
        Set_LCD_8B_REG(0xE5,0x1C); // EQGND_M1=0x1C
        Set_LCD_8B_REG(0xE6,0x00); // EQVCI_M0=0x1C
        Set_LCD_8B_REG(0xE7,0x1C); // EQGND_M0=0x1C
        Set_LCD_8B_REG(0xEE,0x42); // For GRAM read/write speed
        Set_LCD_8B_REG(0xEF,0xDB); // For GRAM read/write speed
        Set_LCD_8B_REG(0x2E,0x98); //For Gate timing, prevent the display abnormal in RGB I/F

// Gamma
        Set_LCD_8B_REG(0x40,0x00);
        Set_LCD_8B_REG(0x41,0x2D);
        Set_LCD_8B_REG(0x42,0x29);
        Set_LCD_8B_REG(0x43,0x2F);
        Set_LCD_8B_REG(0x44,0x2C);
        Set_LCD_8B_REG(0x45,0x33);
        Set_LCD_8B_REG(0x46,0x24);
        Set_LCD_8B_REG(0x47,0x76);
        Set_LCD_8B_REG(0x48,0x00);
        Set_LCD_8B_REG(0x49,0x03);
        Set_LCD_8B_REG(0x4A,0x07);
        Set_LCD_8B_REG(0x4B,0x11);
        Set_LCD_8B_REG(0x4C,0x11);

        Set_LCD_8B_REG(0x50,0x12);
        Set_LCD_8B_REG(0x51,0x13);
        Set_LCD_8B_REG(0x52,0x10);
        Set_LCD_8B_REG(0x53,0x16);
        Set_LCD_8B_REG(0x54,0x12);
        Set_LCD_8B_REG(0x55,0x3F);
        Set_LCD_8B_REG(0x56,0x09);
        Set_LCD_8B_REG(0x57,0x5B);
        Set_LCD_8B_REG(0x58,0x0E);
        Set_LCD_8B_REG(0x59,0x0E);
        Set_LCD_8B_REG(0x5A,0x18);
        Set_LCD_8B_REG(0x5B,0x1B);
        Set_LCD_8B_REG(0x5C,0x1F);
        Set_LCD_8B_REG(0x5D,0xC0);

// Set GRAM area 320x240
        Set_LCD_8B_REG(0x02,0x00);
        Set_LCD_8B_REG(0x03,0x00);
        Set_LCD_8B_REG(0x04,0x01);
        Set_LCD_8B_REG(0x05,0x3F);
        Set_LCD_8B_REG(0x06,0x00);
        Set_LCD_8B_REG(0x07,0x00);
        Set_LCD_8B_REG(0x08,0x00);
        Set_LCD_8B_REG(0x09,0xEF);

// Power Setting
        Set_LCD_8B_REG(0x24,0x22); // Set VCOMH voltage, VHH=0x64
```

```
        Set_LCD_8B_REG(0x25,0x64); // Set VCOML voltage, VML=0x71
        Set_LCD_8B_REG(0x23,0x97); // Set VCOM offset, VMF=0x52
        Set_LCD_8B_REG(0x1B,0x0E);// Set VERG1 voltage, VRH[5:0]=0x1E
        Set_LCD_8B_REG(0x1D,0x11);// FS0[1:0]=01, Set the operating frequency of the step-up circuit 1

// Power on Setting
        Set_LCD_8B_REG(0x19,0x01); // OSC_EN=1, Start to Oscillate
        Set_LCD_8B_REG(0x1C,0x03);// AP=011
        Set_LCD_8B_REG(0x01,0x00); // Normal display(Exit Deep standby mode)
        Set_LCD_8B_REG(0x1F,0x80); // Exit standby mode and Step-up circuit 1 enable
        // GAS_EN=1, VCOMG=0, PON=0, DK=0, XDK=0, DDVDH_TRI=0, STB=0
        DelayX1ms(5);

        Set_LCD_8B_REG(0x1F,0x90); // Step-up circuit 2 enable
        // GAS_EN=1, VCOMG=0, PON=1, DK=0, XDK=0, DDVDH_TRI=0, STB=0
        DelayX1ms(5);

        Set_LCD_8B_REG(0x1F,0xD4);
        // GAS_EN=1, VCOMG=1, PON=1, DK=0, XDK=1, DDVDH_TRI=0, STB=0
        DelayX1ms(5);

// Display ON Setting
        Set_LCD_8B_REG(0x28,0x08); // GON=0, DTE=0, D[1:0]=01
        DelayX1ms(40);
        Set_LCD_8B_REG(0x28,0x38); // GON=1, DTE=1, D[1:0]=10
        DelayX1ms(40);
        Set_LCD_8B_REG(0x28,0x3C);// GON=1, DTE=1, D[1:0]=11

        Set_LCD_8B_REG(0x17,0x06); // 18-bit/pixel

        HX8357-A_Update_GRAM();
}
```

5.9 The reference setting of normal display for CPT's Panel(for MPU mode)

```
Void HX8357-A_CPT_024GP21_initial_code(void)
{
// SUB_SEL for HX8357-A in use MDDI I/F
//Add the two setting below while using MDDI I/F
        Set_LCD_8B_REG(0xFF,0x00); // Command page 0
        Set_LCD_8B_REG(0x72,0xF6); // SUB_SEL=0xF6

// Power saving for HX8357-A
        Set_LCD_8B_REG(0xFF,0x00); // Command page 0
        Set_LCD_8B_REG(0xF2,0x00); // GENON=0x00
        Set_LCD_8B_REG(0xE4,0x00); // EQVCI_M1=0x00
        Set_LCD_8B_REG(0xE5,0x1C); // EQGND_M1=0x1C
        Set_LCD_8B_REG(0xE6,0x00); // EQVCI_M0=0x1C
        Set_LCD_8B_REG(0xE7,0x1C); // EQGND_M0=0x1C
        Set_LCD_8B_REG(0xEE,0x42); // For GRAM read/write speed
        Set_LCD_8B_REG(0xEF,0xDB); // For GRAM read/write speed
        Set_LCD_8B_REG(0x2E,0x98); //For Gate timing, prevent the display abnormal in RGB I/F

// Gamma
        Set_LCD_8B_REG(0x40,0x00);
        Set_LCD_8B_REG(0x41,0x2E);
        Set_LCD_8B_REG(0x42,0x2D);
        Set_LCD_8B_REG(0x43,0x3F);
        Set_LCD_8B_REG(0x44,0x3F);
        Set_LCD_8B_REG(0x45,0x3F);
        Set_LCD_8B_REG(0x46,0x2C);
        Set_LCD_8B_REG(0x47,0x7F);
        Set_LCD_8B_REG(0x48,0x07);
        Set_LCD_8B_REG(0x49,0x05);
        Set_LCD_8B_REG(0x4A,0x08);
        Set_LCD_8B_REG(0x4B,0x13);
        Set_LCD_8B_REG(0x4C,0x1E);

        Set_LCD_8B_REG(0x50,0x00);
        Set_LCD_8B_REG(0x51,0x00);
        Set_LCD_8B_REG(0x52,0x00);
        Set_LCD_8B_REG(0x53,0x12);
        Set_LCD_8B_REG(0x54,0x11);
        Set_LCD_8B_REG(0x55,0x3F);
        Set_LCD_8B_REG(0x56,0x00);
        Set_LCD_8B_REG(0x57,0x53);
        Set_LCD_8B_REG(0x58,0x01);
        Set_LCD_8B_REG(0x59,0x0C);
        Set_LCD_8B_REG(0x5A,0x17);
        Set_LCD_8B_REG(0x5B,0x1A);
        Set_LCD_8B_REG(0x5C,0x18);
        Set_LCD_8B_REG(0x5D,0xC3);

// Set GRAM area 320x240
        Set_LCD_8B_REG(0x02,0x00);
        Set_LCD_8B_REG(0x03,0x00);
        Set_LCD_8B_REG(0x04,0x01);
        Set_LCD_8B_REG(0x05,0x3F);
        Set_LCD_8B_REG(0x06,0x00);
        Set_LCD_8B_REG(0x07,0x00);
        Set_LCD_8B_REG(0x08,0x00);
        Set_LCD_8B_REG(0x09,0xEF);

// Power Setting
```

```
        Set_LCD_8B_REG(0x24,0x22); // Set VCOMH voltage, VHH=0x64
        Set_LCD_8B_REG(0x25,0x64); // Set VCOML voltage, VML=0x71
        Set_LCD_8B_REG(0x23,0x90); // Set VCOM offset, VMF=0x52
        Set_LCD_8B_REG(0x1B,0x0E);// Set VERG1 voltage, VRH[5:0]=0x1E
        Set_LCD_8B_REG(0x1D,0x11);// FS0[1:0]=01, Set the operating frequency of the step-up circuit 1

// Power on Setting
        Set_LCD_8B_REG(0x19,0x01); // OSC_EN=1, Start to Oscillate
        Set_LCD_8B_REG(0x1C,0x03);// AP=011
        Set_LCD_8B_REG(0x01,0x00); // Normal display(Exit Deep standby mode)
        Set_LCD_8B_REG(0x1F,0x80); // Exit standby mode and Step-up circuit 1 enable
        // GAS_EN=1, VCOMG=0, PON=0, DK=0, XDK=0, DDVDH_TRI=0, STB=0
        DelayX1ms(5);

        Set_LCD_8B_REG(0x1F,0x90); // Step-up circuit 2 enable
        // GAS_EN=1, VCOMG=0, PON=1, DK=0, XDK=0, DDVDH_TRI=0, STB=0
        DelayX1ms(5);

        Set_LCD_8B_REG(0x1F,0xD4);
        // GAS_EN=1, VCOMG=1, PON=1, DK=0, XDK=1, DDVDH_TRI=0, STB=0
        DelayX1ms(5);

// Display ON Setting
        Set_LCD_8B_REG(0x28,0x08); // GON=0, DTE=0, D[1:0]=01
        DelayX1ms(40);
        Set_LCD_8B_REG(0x28,0x38); // GON=1, DTE=1, D[1:0]=10
        DelayX1ms(40);
        Set_LCD_8B_REG(0x28,0x3C);// GON=1, DTE=1, D[1:0]=11

        Set_LCD_8B_REG(0x17,0x06); // 18-bit/pixel

        HX8357-A_Update_GRAM();
}
```

6. Revision History

Version	Date	Description of changes
01	2008/08/25	New setup
	2008/11/11	1. Update initial code.(P.17~P.18) 2. Add 5.7 The reference setting of write display data to GRAM.(P.20)
	2008/11/20	1. Update Reference FPC circuit for CMO's F03002-01U panel.(P.13~14)
	2008/12/16	1. Update initial code for CMO's Panel.(P17) 2. Update reference setting of Exit Standby mode.(P.19) 3. Update reference setting of Exit Deep-Standby mode.(P.20)
	2008/12/17	1. Update reference setting of Enter Standby mode.(P.19) 2. Update reference setting of Enter Deep-Standby mode. (P.20)
	2009/04/01	1. Update initial code for MDDI use 2. Update Reference FPC circuit for Wintek's panel.(P16) 3. Update Reference FPC circuit for CPT's panel.(P17) 4. Update Initial code for Display ON 5. Update Initial code for MDDI SUB_SEL(R72h)
	2009/04/13	1. Add Table4.1 ,Table 4.2 (P.18, P.19)
	2009/04/17	1. Add reference initial flow for WINTEK & CPT panel,(P.26)