Key Features

Processor Core

- RISC-V CPU, up to 1 GHz
- RISC-V MCU, up to 600 MHz

Video Encoding/Decoding Performance

- H.264 BP/MP/HP encoding
  - Supports I/P frame
  - Maximum resolution: 3072 x 3072
- Multi-stream real-time encoding capability:
  - Single-camera 1920x1080@30fps + 640x480@30fps
  - Dual-camera 1920x1080@15fps*2 + 640x480@15fps*2
- JPEG encoding/decoding
  - Maximum resolution: 8192x8192
  - Maximum performance: 1920x1080@60fps
- Supports simultaneous operation of H.264/MJPEG encoding and MJPEG decoding

ISP

- Maximum resolution:
  - Offline: 3456 x 1920
  - Online: 1920 x 1920
- Time Division Multiplexing (TDM) mode and maximum 2-lane multiplexing

Video Input

- 8/10/12-bit width parallel CSI interfaces
- 1*2-lane/2*1-lane MIPI CSI
  - Up to 1.0 Gbit/s per lane
  - Compliant with MIPI-CSI2 V1.1 and MIPI DPHY V1.0
  - Maximum resolution: 1920x1920

Video Output

- One serial RGB interface, up to 800 x 480@60fps

Audio

- 1 DAC and 1 ADC
- 1 x audio input: MICINP/N
- 1 x audio output: LINEOUTP/N
- Embedded 1 I2S/PCM interface, supporting maximum 16 channels, 8 kHz-384 kHz sample rate, and 8-bit to 32-bit width

Security

- AES, DES, and 3DES encryption and decryption algorithms
- MD5 and SHA256 tamper proofing
- 160-bit hardware pseudo random number generator(PRNG) with 192-bit seed
- 128-bit hardware true random number generator(TRNG)
- Integrated 2048-bit eFuse for chip ID and security application

Wi-Fi

- Compatible with IEEE 802.11b/g/n standard
- Single-band 2.4 GHz 1T1R mode
- Integrated LNA, PA, and T/R switch
- Security support for WPA/WPA2/WPA3 personal and WPS2.0
- Supports STA, SoftAP, STA+SoftAP, and monitor modes

Memory

- Embedded 64 MB DDR2
- SD2.0, eMMC4.41, and SPI NOR/NAND Flash for boot
- One SPI interface, supporting quad DTR mode

Peripherals Interfaces

- 1 x USB2.0 DRD, 3 x SPI, 3 x TWI, 4 x UART
- 1 x 10/100 Mbit/s Ethernet port with RMII interface
- 12-ch PWM, 3-ch GPADC

Device Summary

Orderable Device(s)	Package
V821L2-XXX V821M2-WXX V821L2-WXX	QFN 88 Pins Body size: 9 mm x 9 mm Maximum height: 0.95 mm

See Table 2-1 Device Differences for details.

Revision History

Revision	Date	Author	Description
0.90	November 15, 2024	AWA1896	Initial Version
0.91	January 9, 2025	AWA1896	1. Modify the maximum voltage of VDD-SYS from 0.99 V to 1.05 V in Table 5-2 Recommended Operating Conditions. 2. Update the T1 range in Table 5-32 Timing Parameters of Power-Up Sequence.

Content

Figures

Tables

About This Document

Purpose and Scope

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package of the V821 family.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Related Documentation

For a complete listing of related documentation and development-support tools for the device, contact the Allwinner FAE or access the Allwinner Customer Service Platform by visiting https://open.allwinnertech.com/.

Revision Number Definition

Revision 0.90-0.9x

This document is released based on the design completion products yet to be mass-produced. Therefore, the information in this document may be modified by reason of mass-produced verification.

All statements, information and recommendations in this document do not constitute any express or implied representation or warranty (including, but not limited to, the warranties of fitness for a particular purpose, merchantability, non-infringement, and accuracy and completeness of the document). Allwinner shall not be liable for any person's use of such information or/and this document.

If you have any questions about the document, please contact us to confirm and obtain the latest version.

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
CAUTION	A caution means that damage to equipment is possible.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

FT/QA/QC Test

All Allwinner chips provided for clients have passed the following tests.

Test Item	Description
FT Test	FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.
QA Test	QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

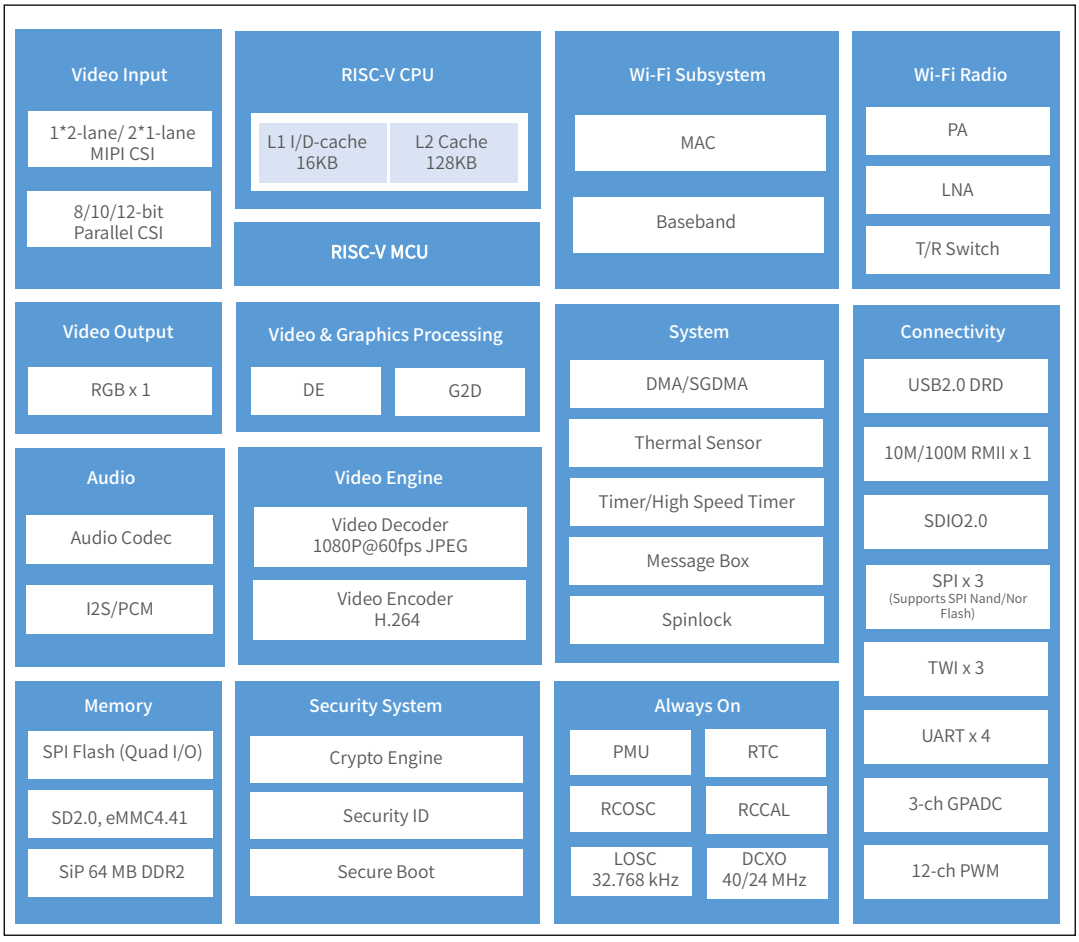
Test Item	Description
QC Test	QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

1 Overview

V821 is a highly integrated low-power multi-camera IPC SoC, featuring dual RISC-V architecture processors. This chip supports real-time dual-camera input and provides 1080P high-definition video processing capabilities with internal high-performance ISP and H.264 encoder. Additionally, V821 integrates Wi-Fi, LDO, IRCUT, and audio codec, offering a highly cost-effective IPC solution. With its excellent ISP processing performance, low power consumption, and high scalability, V821 can be applied in multi-camera IPCs, low-power doorbells, smart locks, and more products.

The following figure shows the system block diagram for the device.

Figure 1-1 System Block Diagram



NOTE

Some modules shown in this block diagram are not offered on all devices, please refer to Table 2-1 for details.

2 Device Differences

The following table provides the differences of orderable device(s) covered by this document.

Table 2-1 Device Differences

Features	V821L2-XXX	V821M2-WXX	V821L2-WXX
Video Output	-	-	√
RTC	√	-	√
Integrated Wi-Fi4	-	√	√
Lower-power Wi-Fi	-	-	√

"-" indicates this device does not support this feature.

"√" indicates this device supports this feature.

3 Features

3.1 Processors

- RISC-V CPU (CPU0), up to 1 GHz
  - 16 KB I-cache and 16 KB D-cache
  - 128 KB L2 cache
- RISC-V MCU (CPU1), up to 600 MHz
  - 16 KB I-cache and 8 KB D-cache

3.2 Memory

3.2.1 Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
  - SD Card
  - eMMC
  - SPI NOR Flash (Single Mode)
  - SPI NAND Flash
- Supports mandatory upgrade process through USB
- Supports GPIO pin and eFuse module to select the boot media type
- Supports normal boot and secure boot

3.2.2 SDRAM

- SiP 64 MB DDR2

3.2.3 SD/MMC Host Controller (SMHC)

- SD/MMC Host Controller (SMHC) interfaces
  - SMHC0, compliant with the protocol Secure Digital Memory (up to SD2.0)
  - SMHC0, compliant with the protocol Multimedia Card (up to eMMC4.41)
  - SMHC1, compliant with the protocol Secure Digital I/O (up to SDIO2.0)
- The SMHC0 and the SMHC1 support the following:
  - 1-bit or 4-bit data width
  - Maximum performance:
    - DDR mode 50 MHz@3.3 V IO pad
    - SDR mode 50 MHz@3.3 V IO pad
- Supports block size of 1 to 65535 bytes
- Supports hardware CRC generation and error detection

3.2.4 SPI Flash Controller (SPIF)

- Supports multiple SPI modes
  - Standard SPI
  - Dual-Input/Dual-Output SPI, and Dual-I/O SPI
  - Quad-Input/Quad-Output SPI, Quad-I/O SPI, and QPI
  - 3-wire SPI with programmable serial data frame length of 1 bit to 32 bits
- Supports STR mode and DTR mode
- High Speed Clock Frequency
  - 150MHz for STR Mode
  - 100MHz for DTR Mode
- Supports mode0, mode1, mode2 and mode3
- Supports control signal configuration
  - One chip select
  - Polarity and phase of the Chip Select (SPIF_CS) and SPI Clock (SPIF_CLK) are configurable

3.3 Image Processing

3.3.1 Image Signal Processor (ISP)

- Supports multiple sensors (up to 2) input
- Supports raw8/10/12
- Maximum resolution
  - Online: 1920 x 1920

  - Offline: 3456 x 1920
- Performance of one sensor:
  - Online: 2M@38fps (linear)
  - Offline: 3M@20fps (linear)
- Support multiple data stream (up to 4) output
  - YUV422/YUV420 output
  - Graphics mirror and flip
  - 1/16x to 1x scaling down
  - Rectangle bounding boxes
- Support ISP adjustment tool on the PC (online/offline/remote debugging)
- Supports Algorithm Features:
  - Crop
  - Dynamic Range Compression (DRC)
  - Tone Mapping
  - Black Level Correction
  - Digital Gain
  - White Balance
  - Len Shading Correction (LSC)
  - Gamma Correction
  - Defect Pixel Correction (DPC)
  - Cross Talk Correction (CTC)
  - Chromatic Aberration Correction (CAC)
  - Noise Reduction (2D/3D)
  - Bayer Interpolation
  - Sharpness
  - Color Enhancement
  - Adjustable 3A functions: Automatic White Balance (AWB), Automatic Exposure (AE), and Automatic Focus (AF)
  - Supports Anti-flick Detection Statistics
  - Histogram Statistics

3.4 Graphics Processing

3.4.1 Display Engine (DE)

- One display output, size up to 1280 x 800@60fps
- Two alpha blending channels
- One overlay layer in video channel, and has an independent scaler.
- Four overlay layers in UI channel and no scaler support
- Supports potter-duff compatible blending operation

- Input format
  - Semi-planar of YUV422/YUV420/YUV411
  - Planar of YUV422/YUV420/ YUV411
  - ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565
- Support Frame Packing/Top-and-Bottom/Side-by-Side Full format data.
- SmartColor2.0 for excellent display experience
  - Hue gain, saturation gain, and value gain controller
  - Fully programmable color matrix
  - Dynamic gamma
- Supports write back for verification

3.4.2 Graphic 2D (G2D)

- Supports layer size up to 1280 x 800 pixels
- The input formats supporting rotation function are as follows:
  - YUV422 (packed, semi-planar and planar format)
  - YUV420 (semi-planar and planar format)
  - P010, P210, P410, and Y8
  - A2R10G10B10, A2B10G10R10, R10G10B10A2, and B10G10R10A2
  - ARGB8888, RGBA8888, XRGB8888, RGBX8888, RGB888, RGB565, ARGB4444, RGBA4444, ARGB1555, and RGBA5551
  - ABGR8888, BGRA8888, XBGR8888, BGRX8888, BGR888, BGR565, ABGR4444, BGRA4444, ABGR1555, and BGRA5551
- For output formats:
  - RGB/ARGB color formats: the input and output formats are the same
  - YUV formats: the output format will be YUV420 after 90/270 degrees' rotation, otherwise the input and output formats are the same
- Multiple rotation types
  - Horizontal flip and vertical flip
  - 0, 90, 180, or 270 degrees' rotation in clockwise direction

3.5 Video Engine

3.5.1 Video Decoder

- JPEG baseline decoding
  - Supports 1920x1080@60fps
  - Maximum decoding resolution: 8192 x 8192
  - Supports two channels for output: the prior channel and the second channel
    - The prior channel supports online scale-down: 1/2, 1/4, 1/8, 1/16, 1/32
    - The second channel supports online scale-down: 1/2, 1/4, 1/8

  - The second can be enable when the prior channel output format is YUV420 and scale ratio is 1/1, 1/2 or 1/4, the prior channel scale ratio shall be larger than the second channel scale ratio.
- Supports translation: YUVV444 to YUV420, YUV422 to YUV420, YUV420T to YUV420, YUV to RGB
- Supports tile decoding (ROI Decoding, random rectangle region in the JPEG Picture. If tile decoding mode enable, the second shall be disabled)

3.5.2 Video Encoder

- H.264 BP/MP/HP encoding
  - Supports 1920x1080@38fps
  - Supports I/P frame type
  - Supports CBR, VBR, FIXEDQP, and QPMAP modes
  - Supports region of interest(ROI) encoding, a maximum of eight ROIs
  - Maximum resolution: 3072x3072
- JPEG baseline encoding
  - Supports 1920x1080@60fps
  - Supports YUV420, YUV422 and YUV444 format
  - Maximum resolution: 8192x8192
- MJPEG baseline encoding up to 1920x1080@60fps

3.6 Video Input Interfaces

3.6.1 MIPI CSI

- Complaint with MIPI CSI-2 specification v1.1 and MIPI D-PHY specification v1.0
- Up to 1.0 Gbit/s per lane, 2M@25fps/2M@38fps, size up to 1920 x 1920
- Configurable number of data lanes and sequence of data lanes for MIPI interface:
  - 1*2-lane
  - 2*1-lane
- Pixel formats
  - RAW8, RAW10, and RAW12
  - 8-bit YUV420 and YUV422
  - RGB888 and RGB565

3.6.2 Parallel CSI

- Supports 8/10/12-bit width
- Supports BT.601, BT.656, and Digital Camera (DC) protocol
- Dual Data Rate (DDR) sample mode with maximum pixel clock of 148.5MHz

- ITU-R BT.656 up to 4-ch 720P@30fps

3.7 Video Output Interfaces

3.7.1 RGB

- One RGB interface
  - Serial/dummy RGB mode, up to 800 x 480@60fps
  - 8-bit i8080 interface, up to 800x480@60fps
  - Dither function for RGB888, RGB666 and RGB565
  - Support BT.656 interface for NTSC and PAL
  - Supports Fsync (Frame Synchronization) for camera sensor

3.8 System Peripherals

3.8.1 PMU

- Switch and parameter configuration of DCDC/LDO/switch and other power supplies
- Opening and closing of each independent internal power supply circuits
- DCXO and RF control
- Supports power-on, power-off, sleep, wake-up and other usage scenarios. Each usage scenario is triggered by its own trigger source, and the PMU performs subsequent switching actions.

3.8.2 Clock Controller Unit (CCU)

- Up to 3 CCU controllers (CCU_APP, CCU_AON, CCU_WLAN)
- Supports clock configuration and clock generation for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules
- 6 PLLs
  - PLL_CPU, supporting dynamic FM
  - PLL_VIDEO, supporting spread spectrum and decimal division
  - PLL_PERI, supporting spread spectrum and decimal division
  - PLL_CSI, supporting spread spectrum and decimal division
  - PLL_DDR, supporting spread spectrum and decimal division
  - PLL_WIFI, supporting integer division and decimal division

3.8.3 Message Box (MSGBOX)

- Up to 2 message boxes
  - 2 message boxes for communication between two RISC-V cores

  - Each user has one MSGBOX and can only read or write in one communication
- 4 channels between every 2 users
- The FIFO depth of a channel is 8
- The FIFO width of a channel is 32 bits
- Supports interrupts

3.8.4 Global Power Reset Clock Management (GPRCM)

- 32.768 kHz clock selection and trimming
- Reset configuration
- RCO_calibration configuration
- PL3-PL7 pin wake-up configuration and PL0-PL2 pin PMC_EN configuration
- Over-temperature protection interrupt
- Under-voltage protection interrupt and reset
- WLAN HIF configuration

3.8.5 RTC

- One 48-bit counter that could be read and written by software
- Up to two alarm clocks (alarm0, alarm1)
  - Supports 2 alarm clocks configured as two different working mode
  - Supports interrupts of both 2 alarm clock
  - Days of the week for alarm1 are configurable
- Leap years and common years could be selected via software or automatically calculated via hardware
- Supports calendar timing for counting maximum 256 years. When leap years are calculated via hardware, counting starts with the year 1990.
- Supports software to update calendar in real time
- Supports software to select counting clocks
- Supports counting frequency of 32.000 kHz or 32.768 kHz

3.8.6 Spinlock

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

3.8.7 Thermal Sensor Controller (THS)

- Two thermal sensors
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

- Temperature accuracy: ±3 °C from 0 °C to 100°C, ±5°C from -25 °C to 125 °C

3.8.8 High Speed Timer (HSTimer)

- Single clock source: AHB with normal working frequency of 192 MHz and could provide clocks with higher accuracy
- Supports 7 prescale factors
- Configurable 56-bit down timer
- Supports 2 timing modes: periodic mode and one-shot mode
- Supports the test mode
- Generates an interrupt when the count is decreased to 0

3.8.9 Timer

- Two timers
  - Alternative count clock: SYS 32k or HOSC. The SYS 32k can be either the internal or external low-frequency clock, and the external one has more accuracy.
  - Supports 8 prescale factors
  - Programmable 32-bit down timer
  - Supports two timing modes: periodic mode and single counting mode
  - Generates an interrupt when the count is decreased to 0
- Supports AVS
  - Single clock source: HOSC
  - Programmable 33-bit up timer
  - Supports updating the initial value anytime
  - 12-bit frequency divider factor
  - Supports Pause/Start function

3.9 Audio

3.9.1 Audio Codec

- One audio differential microphone input: MICINP/N
- One audio lineout output: LINEOUTP/N
- One audio analog-to-digital converter (ADC) channel
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 48 kHz ADC sample rate
  - 95 ± 3dB SNR@A-weight, -80 ± 3dB THD+N
- One audio digital-to-analog converter (DAC) channel
  - 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate

- SNR ⩾ 90 dB (A-weight), THD+N ⩽ -85 dB @Load=10K
- Supports Dynamic Range Controller adjusting the DAC playback and ADC Capture
- One 128x20-bits FIFO for ADC data receive and one 128 x 20-bits FIFO for DAC data transmit
- Programmable FIFO thresholds
- Supports interrupts and DMA

3.9.2 I2S/PCM

- One I2S/PCM interface
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and TDM format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and receive data FIFOs
  - Programmable FIFO thresholds
  - 128 x 32-bit TXFIFO, 64 x 32-bit RXFIFO
- Supports multiple function clocks
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and peripheral I2S/PCM satisfy timing parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode (Only if the IO PAD and peripheral I2S/PCM satisfy timing parameters)
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8 bits to 32 bits
  - Sample rate from 8 kHz to 384 kHz (sample rate * channel * slot width ⩽ 24.576 MHz)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

3.10 Peripheral Interfaces

3.10.1 USB2.0 DRD

- One USB2.0 DRD (USB0), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Static host and device mode
- USB host that supports the following:
  - Compatible with Enhanced Host Controller Interface (EHCI) specification, version 1.0
  - Compatible with Open Host Controller Interface (OHCI) specification, version 1.0a
  - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
  - Supports only 1 USB Root Port shared between EHCI and OHCI
- USB device that supports the following:

- High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)
- Up to 8KB+64Bytes FIFO for EPs (including EP0)

- Supports an internal DMA controller for data transfer with memory
- Device and Host controller share an 8KB SRAM and a physical PHY

3.10.2 Ethernet MAC

- Compatible with the IEEE 802.3-2002 standard
- Supports 10/100M bit/s data transfer rates
- Supports RMII PHY interface
  - Supports both full-duplex and half-duplex operation
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
  - Supports linked-list descriptor list structure
  - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 2 KBytes of data
  - Comprehensive status reporting for normal operation and transfers with errors
- Supports 1 KB TXFIFO for transmission packets and 2 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions
- Support MDIO Interface

3.10.3 UART

- Up to 4 UART controllers: UART0, UART1, UART2, UART3
- Compatible with industry-standard 16450/16550 UARTs
- 5-8 data bits, 1/1.5/2 stop bits, programmable parity (even, odd, or no parity)
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
  - Each of them is 64 bytes for UART0
  - Each of them is 128 bytes for UART1, UART2, UART3
- Supports 8-bit/RS-485 format
- Supports Software/hardware flow control
- Supports interrupts and DMA mode
- Supports auto-flow by using CTS & RTS (excluding UART0)
- Supports TX/RX DMA salve interface

3.10.4 PWM

- Up to 12 PWM channels
  - Supports PWM continuous mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range:

  - 0 to 40 MHz (when the clock source is DCXO)
  - 0 to 100 MHz (when the clock source is APB0 clock)
- Various duty-cycle: 0% -100%
- Minimum resolution: 1/65536

- Supports dead-zone generator, and the dead-zone time is configurable
- Maximum 4 group of PWM channel output
  - In group mode, the relative phase of the output waveform for each channel is configurable
- Supports capture input
- Supports PWM output and capture input to generate interrupts

3.10.5 SPI and SPI_DBI

Up to 3 SPI controllers: SPI0, SPI1, and SPI2

SPI0 and SPI1

SPI0 only supports SPI mode, and SPI1 supports both SPI mode and DBI mode

SPI Mode

- Multiple SPI modes:
  - Master mode and slave mode for standard SPI
  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Master mode for Quad-Output/Quad-Input SPI
  - Master mode for 3-wire SPI, with programmable serial data frame length of 1 bit to 32 bits
- TX/RX DMA Slave interface
- Transmit/Receive data FIFO with 8-bit wide and 64-entry
- Transmit/ Receive data buffer with 8-bit wide and 4-entry
- Supports mode0, mode1, mode2, and mode3 for master mode and slave mode
- Supports control signal configuration
  - One or two chip select(s) to support multiple peripherals
  - Polarity and phase of the Chip Select (SPI_CS) and SPI Clock (SPI_CLK) are configurable

DBI Mode

- DBI Type C 3 Line/4 Line Interface Mode
- 2 Data Lane Interface Mode
- RGB111/444/565/666/888 video format
- Maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Tearing effect
- Software flexible control video frame rate

SPI2

- Multiple SPI modes:
  - Master mode and slave mode for standard SPI
  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Master mode for Quad-Output/Quad-Input SPI
  - Master mode for 3-wire SPI, with programmable serial data frame length of 1 bit to 32 bits
  - Camera slave mode for Dual-Input SPI
  - Camera slave mode for Quad-Input SPI
- TX/RX DMA Slave interface
- Transmit/Receive data FIFO with 8-bit wide and 64-entry
- Transmit/ Receive data buffer with 8-bit wide and 128-entry
- Supports mode0, mode1, mode2, and mode3 for master mode and slave mode
- Supports control signal configuration for master mode and slave mode
  - One chip select
  - Polarity and phase of the Chip Select (SPI_CS) and SPI Clock (SPI_CLK) are configurable

3.10.6 Two Wire Interface (TWI)

- Up to 3 TWI controllers: TWI0, TWI1, and TWI2
- Compliant with I2C bus standard
- master mode and slave mode
- 7-bit and 10-bit device addressing modes
- Standard mode (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s)
- Supports multi-master devices

3.10.7 General Purpose ADC (GPADC)

- One GPADC with total 3 channels
- 12-bit sampling resolution and 8-bit effective precision
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode
- Analog input range: 0 to 1.8 V
- Maximum voltage for GPADC pins:
  - For GPADC0-0: 3.63 V
  - For GPADC0-2 and GPADC0-3: 2.376 V

3.11 Security

3.11.1 Crypto Engine (CE)

- Supports encryption and decryption algorithms: AES, DES, 3DES, SHA-1, MD5, PRNG, CRC32/16, and SHA256
- AES/DES/3DES symmetrical algorithm supports ECB/CBC/CTR mode
- AES symmetrical algorithm supports CTS mode and 128/192/256-bit key size
- 160-bit hardware PRNG with 192-bit seed
- 32 x 32 RXFIFO and 32 x 32 TXFIFO
- AHB interface, supporting CPU access
- DMA interface, supporting external DMA access

3.11.2 True Random Number Generator (TRNG)

- 128-bit hardware TRNG

3.11.3 Security ID (SID)

- 2048-bit eFuse
- One-time programming
- Supports error bit position correction and ECC checksum
- Read/write protection
- SSK backup and read/write protection backup

3.12 Wi-Fi Subsystem

3.12.1 Wi-Fi MAC

- 802.11d - Regulatory domain operation
- 802.11e - QoS including WMM
- 802.11i - Security including WPA/WPA2/WPA3 compliance
- 802.11w-Supports STA Mode with PMF, SA Query, SAE

3.12.2 Wi-Fi Baseband

- Compatible with IEEE 802.11 b/g/n standard on 2.4 GHz
- Up to 20 MHz bandwidth
- 802.11n MCS0-7 with data rate up to 72.2Mbps (BPSK, r=1/2 through 64QAM, r=5/6)
- 6M~54M data rate for 802.11g
- DSSS, CCK modulation with long and short preamble
- Short Guard Interval
- Long Guard Interval

- Supports RX STBC

3.12.3 Wi-Fi Radio

- Integrated 2.4GHz PA, LNA, and T/R switch
- Internal impedance matching network and harmonic filter allow chip to connect to antenna directly
- Supports XRADIOTECH’s MPD™ technology ensure linearity tracking automatically to always keep EVM and mask within specifications
- Special Architecture and Device design to keep the reliability of PA and also deliver high output power (>25dBm)

3.13 Package

QFN 88 Pins, 9 mm x 9 mm body size, 0.95 mm height (maximum)

4 Pin Description

NOTE

The V821 is configured with different sets of pin characteristic and GPIO multiplexing. The following takes V821L2-WXX as an example. For the pin description of other devices, see *V821L2-XXX_PINOUT.xlsx* and *V821M2-WXX&V821L2-WXX_PINOUT.xlsx*.

4.1 Pin Characteristics

This section lists the characteristics of the device pins from the following seven aspects.

[1] **Pin#**: Package pin numbers associated with each signal.

[2] **Pin Name**: The name of the package pin.

NC means these pins are not connected.

[3] **Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

N/A (Not Applicable)

[4] **Pin Reset State**: The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] **Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pullup

PD: Internal pulldown

PU/PD: Internal pullup and pulldown

N/A: Not Applicable

[6] **Default Buffer Strength**: Defines the default drive strength of the associated output buffer. There are total four levels for buffer strength: 2 mA for level0; 3 mA for level1; 4 mA for level2; 6 mA for level3.

N/A means Not Applicable.

[7] **I/O Power Supply**: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

4.1.1 SDRAM

Table 4-1 SDRAM Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
31	VCC-DRAM0	P	N/A	N/A	N/A	N/A
32	VCC-DRAM1	P	N/A	N/A	N/A	N/A

4.1.2 DCXO

Table 4-2 DCXO Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1	DXIN	AI	N/A	N/A	N/A	VCC-DCXO
2	DXOUT	AO	N/A	N/A	N/A	VCC-DCXO
88	VCC-DCXO	P	N/A	N/A	N/A	N/A

4.1.3 GPIO Groups

4.1.3.1 Port A

Table 4-3 Port A Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
35	GPADC0-2/PA0	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
36	PA1	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
37	PA2	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
38	GPADC0-3/PA3	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
39	PA4	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
40	PA5	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
41	PA6	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
42	PA7	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
43	PA8	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
44	PA9	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
45	PA10	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
46	PA11	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
47	PA12	I/O	Z	PU/PD	4 mA	VCC18-MCSI&VCC-PA
34	VCC18-MCSI&VCC-PA	P	N/A	N/A	N/A	N/A

4.1.3.2 Port C

Table 4-4 Port C Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
16	PC0	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
17	PC1	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
18	PC2	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
19	PC3	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
20	PC4	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
21	PC5	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
22	PC6	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
23	PC7	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
24	PC8	I/O	Z	PU	4 mA	VCC33-PMU&VCC33-PC
25	PC9	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
26	PC10	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
27	PC11	I/O	Z	PU	4 mA	VCC33-PMU&VCC33-PC
28	PC15	I/O	Z	PU/PD	4 mA	VCC33-PMU&VCC33-PC
29	FEL/PC16	I/O	Z	PU	4 mA	VCC33-PMU&VCC33-PC
14	VCC33-PMU&VCC33-PC	P	N/A	N/A	N/A	N/A

4.1.3.3 Port D

Table 4-5 Port D Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
61	PD1	I/O	Z	PU/PD	4 mA	VCC33-PD
62	PD2	I/O	Z	PU/PD	4 mA	VCC33-PD
63	PD3	I/O	Z	PU/PD	4 mA	VCC33-PD
64	PD4	I/O	Z	PU/PD	4 mA	VCC33-PD
65	PD5	I/O	Z	PU/PD	4 mA	VCC33-PD
66	PD6	I/O	Z	PU/PD	4 mA	VCC33-PD
67	PD7	I/O	Z	PU/PD	4 mA	VCC33-PD
68	PD8	I/O	Z	PU/PD	4 mA	VCC33-PD
69	PD9	I/O	Z	PU/PD	4 mA	VCC33-PD

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
70	PD10	I/O	Z	PU/PD	4 mA	VCC33-PD
72	PD11	I/O	Z	PU/PD	4 mA	VCC33-PD
73	PD12	I/O	Z	PU/PD	4 mA	VCC33-PD
74	PD13	I/O	Z	PU/PD	4 mA	VCC33-PD
75	PD14	I/O	Z	PU/PD	4 mA	VCC33-PD
76	PD15	I/O	Z	PU/PD	4 mA	VCC33-PD
77	PD16	I/O	Z	PU/PD	4 mA	VCC33-PD
78	PD17	I/O	Z	PU/PD	4 mA	VCC33-PD
79	PD18	I/O	Z	PU/PD	4 mA	VCC33-PD
80	PD19	I/O	Z	PU/PD	4 mA	VCC33-PD
82	PD22	I/O	Z	PU/PD	4 mA	VCC33-PD
83	PD23	I/O	Z	PU/PD	4 mA	VCC33-PD
71	VCC33-PD	P	N/A	N/A	N/A	N/A

4.1.3.4 Port L

Table 4-6 Port L Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
10	PMC-EN0/PL0	I/O	Z	PU/PD	4 mA	VCC18-RTC
9	PMC-EN1/PL1	I/O	Z	PU/PD	4 mA	VCC18-RTC
8	PMC-EN2/PL2	I/O	Z	PU/PD	4 mA	VCC18-RTC/VCC33-PMU&VCC33-PC
7	PL3	I/O	Z	PU/PD	4 mA	VCC18-RTC/VCC33-PMU&VCC33-PC
6	X32KIN/PL4	I/O	Z	PU/PD	4 mA	VCC18-RTC/VCC33-PMU&VCC33-PC
5	X32KOUT/PL5	I/O	Z	PU/PD	4 mA	VCC18-RTC/VCC33-PMU&VCC33-PC
4	TEST/PL6(1)	I/O	Z	PU/PD	4 mA	VCC18-RTC/VCC33-PMU&VCC33-PC

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
3	PL7	I/O	Z	PU/PD	4 mA	VCC18-RTC/VCC33-PMU&VCC33-PC

(1) TEST/PL6 pin should be held low during chip boot.

4.1.4 USB

Table 4-7 USB Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
58	USB0-DM	A I/O	N/A	N/A	N/A	VCC33-USB&VCC33-AUD
59	USB0-DP	A I/O	N/A	N/A	N/A	VCC33-USB&VCC33-AUD
57	VCC33-USB&VCC33-AUD	P	N/A	N/A	N/A	N/A

4.1.5 RF

Table 4-8 RF Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
86	ANT	A	N/A	N/A	N/A	N/A
84	VCC15-TX	P	N/A	N/A	N/A	N/A
87	VCC15-ANA	P	N/A	N/A	N/A	N/A
85	VCC33-RF	P	N/A	N/A	N/A	N/A

4.1.6 Audio Codec

Table 4-9 Audio Codec Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
50	MICINN	AI	N/A	N/A	N/A	AVCC
49	MICINP	AI	N/A	N/A	N/A	AVCC
54	LINEOUTN	AO	N/A	N/A	N/A	AVCC

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
53	LINEOUTP	AO	N/A	N/A	N/A	AVCC
52	VRA1	AO	N/A	N/A	N/A	AVCC
55	AVCC	P	N/A	N/A	N/A	N/A
51	AGND	G	N/A	N/A	N/A	N/A

4.1.7 GPADC

Table 4-10 GPADC Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
48	GPADC0-0	AI	N/A	N/A	N/A	AVCC

4.1.8 PMU

Table 4-11 PMU Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
13	VBAT-RTC	P	N/A	N/A	N/A	N/A
11	VCC18-RTC	P	N/A	N/A	N/A	N/A
12	VCC18-LDO	P	N/A	N/A	N/A	N/A
56	VCC28-LDO	P	N/A	N/A	N/A	N/A

4.1.9 System

Table 4-12 System Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
15	VDD-SYS0	P	N/A	N/A	N/A	N/A
30	VDD-SYS1	P	N/A	N/A	N/A	N/A
33	VDD-SYS2	P	N/A	N/A	N/A	N/A
60	VDD-SYS3	P	N/A	N/A	N/A	N/A
81	VDD-SYS4	P	N/A	N/A	N/A	N/A

4.2 GPIO Multiplex Function

The following tables provide a description of the GPIO multiplex function.

NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function11 to Function13 are reserved; Function15 is IO disable function.

4.2.1 Port A

Table 4-13 Port A Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
GPADC0-2/PA0	I/O	CSI-SM-VS	PWM0-5			CLK-FANOUT0					PA-EINT0
PA1	I/O	MIPI-CSI-MCLK0	TWI1-SCK	TWI0-SCK	UART1-CTS	PWM0-10					PA-EINT1
PA2	I/O	MIPI-CSI-MCLK1	TWI1-SDA	TWI0-SDA	UART1-RTS	PWM0-11					PA-EINT2
GPADC0-3/PA3	I/O	CSI-SM-VS	PWM0-6	TWI0-SCK	UART1-TX	CLK-FANOUT0					PA-EINT3
PA4	I/O	CSI-SM-HS	PWM0-7	TWI0-SDA	UART1-RX	CLK-FANOUT1					PA-EINT4
PA5	I/O	MIPIA-CSI-CK0N	UART2-CTS	PWM0-8	UART3-TX	TWI1-SCK	SPI2-CS0				PA-EINT5
PA6	I/O	MIPIA-CSI-CK0P	UART2-RTS	PWM0-9	UART3-RX	TWI1-SDA	SPI2-CLK				PA-EINT6
PA7	I/O	MIPIA-CSI-D0N	UART2-TX	UART1-TX	PWM0-0	TWI0-SCK	SPI2-MOSI				PA-EINT7
PA8	I/O	MIPIA-CSI-D0P	UART2-RX	UART1-RX	PWM0-1	TWI0-SDA	SPI2-MISO				PA-EINT8
PA9	I/O	MIPIA-CSI-D1N/MIPIB-CSI-D0N	TWI0-SCK	TWI1-SCK	PWM0-2	UART3-CTS	SPI2-HOLD				PA-EINT9
PA10	I/O	MIPIA-CSI-D1P/MIPIB-CSI-D0P	TWI0-SDA	TWI1-SDA	PWM0-3	UART3-RTS	SPI2-WP				PA-EINT10
PA11	I/O	MIPIB-CSI-CK0N	TWI1-SCK	TWI0-SCK	PWM0-4	UART3-TX					PA-EINT11
PA12	I/O	MIPIB-CSI-CK0P	TWI1-SDA	TWI0-SDA	PWM0-5	UART3-RX					PA-EINT12

4.2.2 Port C

Table 4-14 Port C Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PC0	I/O	SDC0-D1	R-JTAG0-TMS	UART3-CTS	PWM0-0	TWI2-SCK					PC-EINT0
PC1	I/O	SDC0-D0	R-JTAG1-TMS	UART3-RTS	PWM0-1	TWI2-SDA					PC-EINT1
PC2	I/O	SDC0-CLK	UART0-TX	UART3-TX	PWM0-2	TWI1-SCK					PC-EINT2
PC3	I/O	SDC0-CMD	R-JTAG1-TCK	UART3-RX	PWM0-3	TWI1-SDA					PC-EINT3
PC4	I/O	SDC0-D3	UART0-RX	UART2-TX	PWM0-4	TWI0-SCK					PC-EINT4
PC5	I/O	SDC0-D2	R-JTAG0-TCK	UART2-RX	PWM0-5	TWI0-SDA					PC-EINT5

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PC6	I/O	SPIF-WP	SPI0-WP	PWM0-6	TWI2-SCK	FEM-CTRL0	SDC0-CLK				PC-EINT6
PC7	I/O	SPIF-HOLD	SPI0-HOLD	PWM0-7	TWI2-SDA	FEM-CTRL1	SDC0-CMD	CSI-SM-VS			PC-EINT7
PC8	I/O	SPIF-MOSI	SPI0-MOSI	BOOT-SEL0	PWM0-8		SDC0-D0				PC-EINT8
PC9	I/O	SPIF-CLK	SPI0-CLK	TWI2-SCK	PWM0-9		SDC0-D1				PC-EINT9
PC10	I/O	SPIF-CS0	SPI0-CS0	TWI2-SDA	TWI0-SCK	PWM0-10	SDC0-D2				PC-EINT10
PC11	I/O	SPIF-MISO	SPI0-MISO	BOOT-SEL1	TWI0-SDA	PWM0-11	SDC0-D3				PC-EINT11
PC15	I/O		PWM0-11	PWM0-9							PC-EINT15
FEL/PC16	I/O			PWM0-10			CSI-SM-VS	SDC0-RST			PC-EINT16

4.2.3 Port D

Table 4-15 Port D Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PD1	I/O	LCD-D3	NCSI-PCLK	RMII-RXD1	PWM0-0	SDC1-D1	TWI0-SCK	SPI1-CS0/DBI-CSX	SPI2-CS0		PD-EINT1
PD2	I/O	LCD-D4	NCSI-MCLK	RMII-TXCK	PWM0-1	SDC1-D0	TWI0-SDA	SPI1-CLK/DBI-SCLK	SPI2-CLK		PD-EINT2
PD3	I/O	LCD-D5	NCSI-HSYNC	RMII-CRS-DV	PWM0-2	SDC1-CLK	TWI1-SCK	SPI1-MOSI/DBI-SDO	SPI2-MOSI		PD-EINT3
PD4	I/O	LCD-D6	NCSI-VSYNC	RMII-RXD0	PWM0-3	SDC1-CMD	TWI1-SDA	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	SPI2-MISO		PD-EINT4
PD5	I/O	LCD-D7	NCSI-D0	RMII-TXD0	PWM0-4	SDC1-D3	SPI1-CLK	SPI1-HOLD/DBI-DCX/DBI-WRX	SPI2-HOLD		PD-EINT5
PD6	I/O	LCD-D10	NCSI-D1	RMII-TXD1	PWM0-5	SDC1-D2	SPI1-MOSI	SPI1-WP/DBI-TE	SPI2-WP		PD-EINT6
PD7	I/O	LCD-D11	NCSI-D2	RMII-TXEN	PWM0-6	UART1-CTS	SPI1-MISO	R-JTAG1-TCK	I2S0-DOUT0	I2S0-DIN0	PD-EINT7
PD8	I/O	LCD-D12	NCSI-D3	RMII-RXER	PWM0-7	UART1-RTS	SPI1-CS0	R-JTAG1-TMS	I2S0-DOUT1	I2S0-DIN1	PD-EINT8
PD9	I/O		NCSI-D4	RMII-MDC	PWM0-8	UART1-TX	TWI2-SCK	LCD-CLK	I2S0-DOUT2	I2S0-DIN2	PD-EINT9
PD10	I/O		NCSI-D5	RMII-MDIO	PWM0-9	UART1-RX	TWI2-SDA	LCD-DE	I2S0-DOUT3	I2S0-DIN3	PD-EINT10
PD11	I/O		NCSI-D6	RMII-EPHY-25M	PWM0-10	I2S0-MCLK	PWM0-0	LCD-HSYNC			PD-EINT11
PD12	I/O		NCSI-D7	PWM0-2	SPI1-CLK	I2S0-BCLK	CLK-FANOUT0	LCD-VSYNC/TCON-TRIG			PD-EINT12
PD13	I/O		NCSI-D8	PWM0-3	SPI1-MOSI	I2S0-LRCK	TWI1-SCK	TCON-FSYNC			PD-EINT13
PD14	I/O		NCSI-D9	PWM0-4	SPI1-MISO	I2S0-DIN0	TWI1-SDA	SPI1-CS0/DBI-CSX	SPI2-CS0		PD-EINT14
PD15	I/O		NCSI-D10	PWM0-5	SPI1-CS0	I2S0-DOUT0	TWI2-SCK	SPI1-CLK/DBI-SCLK	SPI2-CLK		PD-EINT15
PD16	I/O		NCSI-D11	PWM0-6	SPI1-CS1	CSI-SM-VS	TWI2-SDA	SPI1-MOSI/DBI-SDO	SPI2-MOSI		PD-EINT16

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PD17	I/O			PWM0-7	PWM0-11	SDC1-CLK	FEM-CTRL0	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	SPI2-MISO		PD-EINT17
PD18	I/O			PWM0-8	TWI1-SCK	SDC1-CMD	FEM-CTRL1	SPI1-HOLD/DBI-DCX/DBI-WRX	SPI2-HOLD		PD-EINT18
PD19	I/O			PWM0-9	TWI1-SDA	SDC1-D0		SPI1-WP/DBI-TE	SPI2-WP		PD-EINT19
PD22	I/O		UART0-TX	R-JTAG0-TCK	PWM0-10	SDC1-D3	FEM-CTRL0	TWI2-SCK			PD-EINT22
PD23	I/O		UART0-RX	R-JTAG0-TMS	PWM0-11	SDC1-D2	FEM-CTRL1	TWI2-SDA			PD-EINT23

4.2.4 Port L

Table 4-16 Port L Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function10	Function14
PMC-EN0/PL0	I/O	TWI1-SCK									PL-EINT0
PMC-EN1/PL1	I/O	TWI1-SDA									PL-EINT1
PMC-EN2/PL2	I/O	TWI2-SCK	UART3-TX	UART2-CTS							PL-EINT2
PL3	I/O	TWI2-SDA	UART3-RX	UART2-RTS							PL-EINT3
X32KIN/PL4	I/O	TWI0-SCK	UART0-TX	UART2-TX							PL-EINT4
X32KOUT/PL5	I/O	TWI0-SDA	UART0-RX	UART2-RX							PL-EINT5
TEST/PL6	I/O	CSI-SM-VS									PL-EINT6
PL7	I/O										PL-EINT7

4.3 Detailed Signal Description

The following tables show the detailed function description of every signal based on the different interfaces.

[1] **Signal Name**: The name of every signal.

[2] **Description**: The detailed function description of every signal.

[3] **Type**: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

4.3.1 SDRAM

Table 4-17 SDRAM Signal Description

Signal Name[1]	Description[2]	Type[3]
VCC-DRAM	DRAM Power Supply	P

4.3.2 System Control

Table 4-18 System Control Signal Description

Signal Name[1]	Description[2]	Type[3]
Test	Test Signal	I
FEL	Boot Process Select Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process. For details, see *Allwinner_V821_Hardware_Design_Guide*.	I
BOOT-SEL0	Boot Media Select 0 For details, see *Allwinner_V821_Hardware_Design_Guide*.	I
BOOT-SEL1	Boot Media Select 1 For details, see *Allwinner_V821_Hardware_Design_Guide*.	I

4.3.3 RTC&PLL

Table 4-19 RTC&PLL Signal Description

Signal Name[1]	Description[2]	Type[3]
X32KIN	32.768 kHz Crystal Clock Input	AI
X32KOUT	32.768 kHz Crystal Clock Output	AO

4.3.4 DCXO

Table 4-20 DCXO Signal Description

Signal Name[1]	Description[2]	Type[3]
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
VCC-DCXO	Digital Compensated Crystal Oscillator Power Supply	P

4.3.5 Clock Fanout

Table 4-21 Clock Fanout Signal Description

Signal Name[1]	Description[2]	Type[3]
CLK-FANOUT0	Internal Clock Fanout Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz	O
CLK-FANOUT1	Internal Clock Fanout Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz	O

4.3.6 RF

Table 4-22 RF Signal Description

Signal Name[1]	Description[2]	Type[3]
ANT	Antenna of RF	A
FEM-CTRL0	Front End Module Control, TX-EN	I/O
FEM-CTRL1	Front End Module Control, RX-EN	I/O
VCC15-TX	RF TX Power Supply, Typical 1.5 V	P
VCC15-ANA	RF Analog Power Supply, Typical 1.5 V	P
VCC33-RF	RF PA 3.3 V Power Supply	P

4.3.7 PMU

Table 4-23 PMU Signal Description

Signal Name[1]	Description[2]	Type[3]
VBAT-RTC	RTC Power Input	P
VCC18-RTC	LDO RTC 1.8 V Power Output	P
VCC18-LDO	LDO 1.8 V Power Output	P
VCC28-LDO	LDO 2.8 V Power Output	P

4.3.8 PMC

Table 4-24 PMC Signal Description

Signal Name[1]	Description[2]	Type[3]
PMC-EN0	LDO/DCDC Enable	O
PMC-EN1	LDO/DCDC Enable	O
PMC-EN2	LDO/DCDC Enable	O

4.3.9 SD Card/SDIO/eMMC

Table 4-25 SD Card/SDIO/eMMC Signal Description

Signal Name[1]	Description[2]	Type[3]
SDC0-CMD	SD Card/eMMC Command Output/Response Input	I/O, OD
SDC0-CLK	SD Card/eMMC Clock Output	O
SDC0-RST	SD Card/eMMC Reset	O
SDC0-D0	SD Card/eMMC Data Input/ Output 0	I/O
SDC0-D1	SD Card/eMMC Data Input/ Output 1	I/O
SDC0-D2	SD Card/eMMC Data Input/ Output 2	I/O
SDC0-D3	SD Card/eMMC Data Input/ Output 3	I/O
SDC1-CMD	SDIO WIFI Command Output/Response Input	I/O, OD
SDC1-CLK	SDIO WIFI Clock Output	O
SDC1-D0	SDIO WIFI Data Input/ Output 0	I/O
SDC1-D1	SDIO WIFI Data Input/ Output 1	I/O
SDC1-D2	SDIO WIFI Data Input/ Output 2	I/O
SDC1-D3	SDIO WIFI Data Input/ Output 3	I/O

4.3.10 USB

Table 4-26 USB Signal Description

Signal Name[1]	Description[2]	Type[3]
USB0-DM	USB0 Differential Data (Negative)	A I/O
USB0-DP	USB0 Differential Data (Positive)	A I/O
VCC33-USB	USB2.0 DRD 3.3V Power Supply	P

4.3.11 I2S/PCM

Table 4-27 I2S/PCM Signal Description

Signal Name[1]	Description[2]	Type[3]
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O
I2S0-DIN0	I2S0/PCM0 Serial Data Input 0	I
I2S0-DIN1	I2S0/PCM0 Serial Data Input 1	I
I2S0-DIN2	I2S0/PCM0 Serial Data Input 2	I
I2S0-DIN3	I2S0/PCM0 Serial Data Input 3	I
I2S0-DOUT0	I2S0/PCM0 Serial Data Output 0	O
I2S0-DOUT1	I2S0/PCM0 Serial Data Output 1	O
I2S0-DOUT2	I2S0/PCM0 Serial Data Output 2	O
I2S0-DOUT3	I2S0/PCM0 Serial Data Output 3	O

4.3.12 Audio Codec

Table 4-28 Audio Codec Signal Description

Signal Name[1]	Description[2]	Type[3]
MICINN	Microphone Differential Negative Input	AI
MICINP	Microphone Differential Positive Input	AI
LINEOUTN	Lineout Differential Output (Negative)	AO
LINEOUTP	Lineout Differential Output (Positive)	AO
AVCC	Power Supply for Analog Part	P
VRA1	Internal Reference Voltage	AO
AGND	Analog Ground	G

Signal Name[1]	Description[2]	Type[3]
VCC33-AUD	Audio 3.3V Power Supply	P

4.3.13 GPADC

Table 4-29 GPADC Signal Description

Signal Name[1]	Description[2]	Type[3]
GPADC0-0	General Purpose ADC0 Input 0	AI
GPADC0-2	General Purpose ADC0 Input 2	AI
GPADC0-3	General Purpose ADC0 Input 3	AI

4.3.14 MIPI CSI

Table 4-30 MIPI CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
MIPI-CSI-MCLK0	MIPI CSI A Master Clock	O
MIPIA-CSI-CK0N	MIPI CSI A Differential Receive Clock Signal (Negative)	AI
MIPIA-CSI-CK0P	MIPI CSI A Differential Receive Clock Signal (Positive)	AI
MIPIA-CSI-D0N	MIPI CSI A Data Line 0 Input (Negative)	AI
MIPIA-CSI-D0P	MIPI CSI A Data Line 0 Input (Positive)	AI
MIPIA-CSI-D1N	MIPI CSI A Data Line 1 Input (Negative)	AI
MIPIA-CSI-D1P	MIPI CSI A Data Line 1 Input (Positive)	AI
MIPI-CSI-MCLK1	MIPI CSI B Master Clock	O
MIPIB-CSI-CK0N	MIPI CSI B Differential Receive Clock Signal (Negative)	AI
MIPIB-CSI-CK0P	MIPI CSI B Differential Receive Clock Signal (Positive)	AI
MIPIB-CSI-D0N	MIPI CSI B Data Line 0 Input (Negative)	AI
MIPIB-CSI-D0P	MIPI CSI B Data Line 0 Input (Positive)	AI
CSI-SM-HS	CSI Horizontal SYNC	O
CSI-SM-VS	CSI Vertical SYNC/Frame SYNC	O
VCC18-MCSI&VCC-PA	MIPI CSI/Port A Power Supply	P

4.3.15 Parallel CSI

Table 4-31 Parallel CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
NCSI-PCLK	Parallel CSI Pixel Clock Input	I
NCSI-MCLK	Parallel CSI Master Clock Output	O
NCSI-HSYNC	Parallel CSI Horizontal Synchronous Input	I
NCSI-VSYNC	Parallel CSI Vertical Synchronous Input	I
NCSI-D0	Parallel CSI Pixel Data 0	I
NCSI-D1	Parallel CSI Pixel Data 1	I
NCSI-D2	Parallel CSI Pixel Data 2	I
NCSI-D3	Parallel CSI Pixel Data 3	I
NCSI-D4	Parallel CSI Pixel Data 4	I
NCSI-D5	Parallel CSI Pixel Data 5	I
NCSI-D6	Parallel CSI Pixel Data 6	I
NCSI-D7	Parallel CSI Pixel Data 7	I
NCSI-D8	Parallel CSI Pixel Data 8	I
NCSI-D9	Parallel CSI Pixel Data 9	I
NCSI-D10	Parallel CSI Pixel Data 10	I
NCSI-D11	Parallel CSI Pixel Data 11	I

4.3.16 LCD

Table 4-32 LCD Signal Description

Signal Name[1]	Description[2]	Type[3]
LCD-CLK	LCD Clock	O
LCD-VSYNC	LCD Vertical Synchronization	O
LCD-HSYNC	LCD Horizontal Synchronization	O
LCD-DE	LCD Data Enable	O
TCON-FSYNC	Frame Synchronization Signal for TCON and Sensor	O
TCON-TRIG	Screen Trigger Signal	I
LCD-D3	LCD Data Input/Output 3	I/O
LCD-D4	LCD Data Input/Output 4	I/O

Signal Name[1]	Description[2]	Type[3]
LCD-D5	LCD Data Input/Output 5	I/O
LCD-D6	LCD Data Input/Output 6	I/O
LCD-D7	LCD Data Input/Output 7	I/O
LCD-D10	LCD Data Input/Output 10	I/O
LCD-D11	LCD Data Input/Output 11	I/O
LCD-D12	LCD Data Input/Output 12	I/O

4.3.17 Ethernet MAC

Table 4-33 Ethernet MAC Signal Description

Signal Name[1]	Description[2]	Type[3]
RMII-TXCK	RMII Transmit Clock	I
RMII-RXER	RMII Receive Error	I
RMII-CRS-DV	RMII Carrier Sense Receive Data Valid	I
RMII-TXEN	RMII Transmit Enable	O
RMII-EPHY-25M	EMAC PHY 25 MHz Clock Output	O
RMII-MDC	RMII Management Data Clock	O
RMII-MDIO	RMII Management Data Input/ Output	I/O
RMII-RXD0	RMII Receive Data 0	I
RMII-RXD1	RMII Receive Data 1	I
RMII-TXD0	RMII Transmit Data 0	O
RMII-TXD1	RMII Transmit Data 1	O

4.3.18 SPI&SPI DBI

Table 4-34 SPI&SPI DBI Signal Description

Signal Name[1]	Description[2]	Type[3]
SPI0-CS0	SPI0 Chip Select 0 (Active Low)	I/O
SPI0-CLK	SPI0 Clock	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O

Signal Name[1]	Description[2]	Type[3]
SPI0-HOLD	SPI0 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-CS0	SPI1 Chip Select 0 (Active Low)	I/O
SPI1-CS1	SPI1 Chip Select 1 (Active Low)	I/O
SPI1-CLK	SPI1 Clock	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-HOLD	SPI1 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI2-CS0	SPI2 Chip Select 0 (Active Low)	I/O
SPI2-CLK	SPI2 Clock	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O
SPI2-WP	SPI2 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI2-HOLD	SPI2 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
DBI-CSX	Chip Select Signal (Active Low)	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge.	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O

4.3.19 SPI Flash

Table 4-35 SPI Flash Signal Description

Signal Name[1]	Description[2]	Type[3]
SPIF-CS0	SPI Peripheral Chip Select Signal, Low Active	O
SPIF-CLK	SPI Master Mode Clock Output	O
SPIF-MOSI	SPI Master Data Out, Slave Data In	I/O
SPIF-MISO	SPI Master Data In, Slave Data Out	I/O
SPIF-WP	SPI Write Protection (Active Low)	I/O
SPIF-HOLD	SPI Hold Signal	I/O

4.3.20 UART

Table 4-36 UART Signal Description

Signal Name[1]	Description[2]	Type[3]
UART0-RX	UART0 Data Receiver	I
UART0-TX	UART0 Data Transmitter	O
UART1-CTS	UART1 Clear to Send	I
UART1-RTS	UART1 Request to Send	O
UART1-RX	UART1 Data Receiver	I
UART1-TX	UART1 Data Transmitter	O
UART2-CTS	UART2 Clear to Send	I
UART2-RTS	UART2 Request to Send	O
UART2-RX	UART2 Data Receiver	I
UART2-TX	UART2 Data Transmitter	O
UART3-CTS	UART3 Clear to Send	I
UART3-RTS	UART3 Request to Send	O
UART3-RX	UART3 Data Receiver	I
UART3-TX	UART3 Data Transmitter	O

4.3.21 PWM

Table 4-37 PWM Signal Description

Signal Name[1]	Description[2]	Type[3]
PWM0-0	PWM0 Wave Output /Capture Wave Input 0	I/O

Signal Name[1]	Description[2]	Type[3]
PWM0-1	PWM0 Wave Output /Capture Wave Input 1	I/O
PWM0-2	PWM0 Wave Output /Capture Wave Input 2	I/O
PWM0-3	PWM0 Wave Output /Capture Wave Input 3	I/O
PWM0-4	PWM0 Wave Output /Capture Wave Input 4	I/O
PWM0-5	PWM0 Wave Output /Capture Wave Input 5	I/O
PWM0-6	PWM0 Wave Output /Capture Wave Input 6	I/O
PWM0-7	PWM0 Wave Output /Capture Wave Input 7	I/O
PWM0-8	PWM0 Wave Output /Capture Wave Input 8	I/O
PWM0-9	PWM0 Wave Output /Capture Wave Input 9	I/O
PWM0-10	PWM0 Wave Output /Capture Wave Input 10	I/O
PWM0-11	PWM0 Wave Output /Capture Wave Input 11	I/O

4.3.22 TWI

Table 4-38 TWI Signal Description

Signal Name[1]	Description[2]	Type[3]
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O

4.3.23 JTAG

Table 4-39 JTAG Signal Description

Signal Name[1]	Description[2]	Type[3]
R-JTAG0-TMS	CPU0 JTAG Mode Select	I/O
R-JTAG0-TCK	CPU0 JTAG Clock Signal	I
R-JTAG1-TMS	CPU1 JTAG Mode Select	I/O
R-JTAG1-TCK	CPU1 JTAG Clock Signal	I

4.3.24 Interrupt

Table 4-40 Interrupt Signal Description

Signal Name[1]	Description[2]	Type[3]
PA-EINT0	Port A Interrupt	I
PA-EINT1	Port A Interrupt	I
PA-EINT2	Port A Interrupt	I
PA-EINT3	Port A Interrupt	I
PA-EINT4	Port A Interrupt	I
PA-EINT5	Port A Interrupt	I
PA-EINT6	Port A Interrupt	I
PA-EINT7	Port A Interrupt	I
PA-EINT8	Port A Interrupt	I
PA-EINT9	Port A Interrupt	I
PA-EINT10	Port A Interrupt	I
PA-EINT11	Port A Interrupt	I
PA-EINT12	Port A Interrupt	I
PC-EINT0	Port C Interrupt	I
PC-EINT1	Port C Interrupt	I
PC-EINT2	Port C Interrupt	I
PC-EINT3	Port C Interrupt	I
PC-EINT4	Port C Interrupt	I
PC-EINT5	Port C Interrupt	I
PC-EINT6	Port C Interrupt	I
PC-EINT7	Port C Interrupt	I
PC-EINT8	Port C Interrupt	I
PC-EINT9	Port C Interrupt	I
PC-EINT10	Port C Interrupt	I
PC-EINT11	Port C Interrupt	I
PC-EINT15	Port C Interrupt	I
PC-EINT16	Port C Interrupt	I
PD-EINT1	Port D Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PD-EINT2	Port D Interrupt	I
PD-EINT3	Port D Interrupt	I
PD-EINT4	Port D Interrupt	I
PD-EINT5	Port D Interrupt	I
PD-EINT6	Port D Interrupt	I
PD-EINT7	Port D Interrupt	I
PD-EINT8	Port D Interrupt	I
PD-EINT9	Port D Interrupt	I
PD-EINT10	Port D Interrupt	I
PD-EINT11	Port D Interrupt	I
PD-EINT12	Port D Interrupt	I
PD-EINT13	Port D Interrupt	I
PD-EINT14	Port D Interrupt	I
PD-EINT15	Port D Interrupt	I
PD-EINT16	Port D Interrupt	I
PD-EINT17	Port D Interrupt	I
PD-EINT18	Port D Interrupt	I
PD-EINT19	Port D Interrupt	I
PD-EINT22	Port D Interrupt	I
PD-EINT23	Port D Interrupt	I
PL-EINT0	Port L Interrupt	I
PL-EINT1	Port L Interrupt	I
PL-EINT2	Port L Interrupt	I
PL-EINT3	Port L Interrupt	I
PL-EINT4	Port L Interrupt	I
PL-EINT5	Port L Interrupt	I
PL-EINT6	Port L Interrupt	I
PL-EINT7	Port L Interrupt	I

5 Electrical characteristics

5.1 Parameter Conditions

5.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at Ta = 25 °C and Ta = Ta max.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical Values

Unless otherwise specified, the typical data are based on Ta = 25 °C. They are given only as design guidelines.

5.1.3 Temperature Definitions

- Ambient Temperature— the temperature of the surrounding environment.
- Junction Temperature— the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature— the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature— the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

5.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. The following table specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under section 5.3 Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Supply Name	Description	Min(1)	Max(1)	Unit
AVCC	Power Supply for Analog Part	-0.3	2.16	V
VBAT-RTC	Power Supply for Analog	-0.3	6.5	V
VCC15-ANA	Power Supply for RF	-0.3	2.16	V
VCC15-TX	Power Supply for RF	-0.3	2.16	V
VCC18-MCSI& VCC-PA	MIPI CSI Power Supply Digital Port A Power	-0.3	2.16	V
VCC33-USB&VCC33-AUD	Power Supply for USB Power Supply for Audio	-0.3	3.96	V
VCC33-PMU&VCC33-PC	Digital Port C Power	-0.3	3.96	V
VCC33-PD	Digital Port D Power	-0.3	3.96	V
VCC33-RF	Power Supply for RF	-0.3	3.96	V
VCC-DCXO	Power Supply for DCXO	-0.3	2.16	V
VCC-DRAM	Power Supply for DRAM IO and DDR2	-0.3	2.1	V
VDD-SYS	Power Supply for System	-0.3	1.05	V
V_{ESD}(2)	Human Body Model (HBM)(3)	-2000	+2000	V
	Charged Device Model (CDM)(4)	-600	+600	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(5)	PASS		
	Latch-up over-voltage performance voltage injection on each IO pin(6)	PASS		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2023.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2022.

(5) Based on JESD78F; each device is tested with IO pin injection of ±200 mA at room temperature.

(6) Based on JESD78F; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.3 Recommended Operating Conditions

The following table describes operating conditions of the device.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2 Recommended Operating Conditions

Supply Name	Description	Min	Typ	Max	Unit
AVCC	Power Supply for Analog Part	1.764	1.8	1.836	V
VBAT-RTC	Power Supply for Analog	2.1	3.3	6.0	V
VCC15-ANA	Power Supply for RF	1.4	1.5	1.98	V
VCC15-TX	Power Supply for RF	1.4	1.5	1.98	V
VCC18-MCSI&VCC-PA	MIPI CSI Power Supply Digital Port A Power	1.71	1.8	1.98	V
VCC33-USB&VCC33-AUD	Power Supply for USB Power Supply for Audio	3.07	3.3	3.63	V
VCC33-PMU&VCC33-PC	Digital Port C Power	2.97	3.3	3.63	V
VCC33-PD	Digital Port D Power	2.97	3.3	3.63	V
VCC33-RF	Power Supply for RF	2.97	3.3	3.63	V
VCC-DCXO	Power Supply for DCXO	1.71	1.8	1.89	V
VCC-DRAM	Power Supply for DRAM IO and DDR2	1.7	1.8	1.95	V
		1.425	1.5	1.575	V
VDD-SYS	Power Supply for System	0.9(1)	-	1.05	V

(1) In system hibernation scenarios, V821L2-WXX supports a minimum recommended operating voltage of 0.8V.

5.4 GPIO DC Electrical Characteristics

The following table summarizes the GPIO DC electrical characteristics of the device.

Table 5-3 DC Electrical Characteristics

(VCC: VCC-PA/VCC33-PC/VCC33-PD)

Symbol	Parameter		Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage		0.7*VCC	-	1.1*VCC	V
VIL	Low-Level Input Voltage		-0.3	-	0.3*VCC	V
R_{PU}	Output Pull-up Resistance	PC0-PC16	9	15	21	kΩ
		PD1, PD2, PD4 , PD5, PD6	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
R_{PD}	Output Pull-down Resistance	PC0-PC16	9	15	21	kΩ
		PD1, PD2, PD4 , PD5, PD6	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
I_{IH}	High-Level Input Current		-	-	10	uA
I_{IL}	Low-Level Input Current		-	-	10	uA
V_{OH}	High-Level Output Voltage		VCC – 0.3	-	VCC	V
V_{OL}	Low-Level Output Voltage		0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current		-10	-	10	uA
C_{IN}	Input Capacitance		-	-	5	pF
C_{OUT}	Output Capacitance		-	-	5	pF

PD22 pin and PD23 pin support IR-CUT driver. The following table shows the driving capacity of PD22 pin and PD23 pin when IC-CUT function is enabled.

Table 5-4 The Driving Capacity of PD22 And PD23 When IR-CUT Function Enabled

VCC: VCC33-PD =3.3 V

Driving Strength	Parameter	Min	Max	Unit
Level0	High-Level Output Voltage	VCC-1.7	-	V
	Low-Level Output Voltage	-	0.97	V
	Maximum Output Current	30	40	mA
Level1	High-Level Output Voltage	VCC-1.2	-	V
	Low-Level Output Voltage	-	0.75	V

Driving Strength	Parameter	Min	Max	Unit
	Maximum Output Current	60	70	mA
Level2	High-Level Output Voltage	VCC-0.9	-	V
	Low-Level Output Voltage	-	0.61	V
	Maximum Output Current	85	95	mA
Level3	High-Level Output Voltage	VCC-0.8	-	V
	Low-Level Output Voltage	-	0.5	V
	Maximum Output Current	-	100	mA

5.5 SMHC Electrical Characteristics

The SMHC electrical parameters are related to different supply voltage.

Figure 5-1 SMHC Voltage Waveform

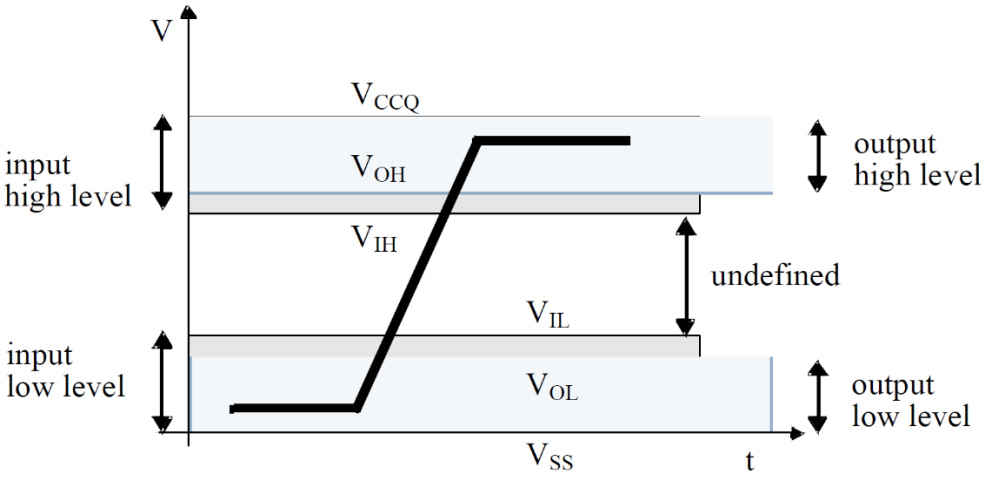


Table 5-5 shows 3.3 V SMHC electrical parameters.

Table 5-5 3.3 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125 * V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

5.6 GPADC Electrical Characteristics

Table 5-6 lists the GPADC electrical characteristics.

Table 5-6 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Effective Precision	-	8	-	bits
Sampling Rate	-	-	1	MHz
Conversion Time	-	13	-	ADC Clock Cycles

5.7 Audio Codec Electrical Characteristics

Test Conditions

VDD-SYS = 0.9 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, ADC fs = 16 kHz, input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 5-7 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	DAC to LINEOUTLP(R=100K)					
	Full-scale	0dBFS 1kHz	-	0.54	-	Vrms
	SNR(A-weighted)	0data	-	95	-	dB
	THD+N	0dBFS 1kHz	-	-85	-	dB
ADC Path	MICIN via ADC					
	Output Level	MICP=3.2Vpp/2,MICN=3.2Vpp/2, 1kHz，0dB Gain	-	907	-	mFFS
	SNR(A-weighted)		-	96	-	dB
	THD+N		-	-85	-	dB
	Output Level	MICP=1.6450Vpp/2,MICN=1.650Vpp/2, 1kHz, 6dB Gain	-	907	-	mFFS
	SNR(A-weighted)		-	95	-	dB
	THD+N		-	-85	-	dB
	Output Level	MICP=1.165Vpp/2,MICN=1.165Vpp/2, 1kHz, 9dB Gain	-	907	-	mFFS
	SNR(A-weighted)		-	95	-	dB
	THD+N		-	-85	-	dB

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Output Level	MICP=0.823Vpp/2,MICN=0.823Vpp/2, 1kHz, 12dB Gain	-	907	-	mFFS
	SNR(A-weighted)		-	95	-	dB
	THD+N		-	-85	-	dB
	Output Level	MICP=0.586Vpp/2,MICN=0.586Vpp/2, 1kHz, 15dB Gain	-	907	-	mFFS
	SNR(A-weighted)		-	94	-	dB
	THD+N		-	-84	-	dB
	Output Level	MICP=0.415Vpp/2,MICN=0.415Vpp/2, 1kHz, 18dB Gain	-	907	-	mFFS
	SNR(A-weighted)		-	92	-	dB
	THD+N		-	-84	-	dB
	Output Level	MICP=0.294Vpp/2,MICN=0.294Vpp/2, 1kHz, 21dB Gain	-	906	-	mFFS
	SNR(A-weighted)		-	90	-	dB
	THD+N		-	-83	-	dB
	Output Level	MICP=0.209Vpp/2,MICN=0.209Vpp/2, 1kHz, 24dB Gain	-	906	-	mFFS
	SNR(A-weighted)		-	88	-	dB
	THD+N		-	-81	-	dB
	Output Level	MICP=0.1504Vpp/2,MICN=0.1504Vpp/2, 1kHz, 27dB Gain	-	906	-	mFFS
	SNR(A-weighted)		-	86	-	dB
	THD+N		-	-80	-	dB
	Output Level	MICP=0.1040Vpp/2,MICN=0.1040Vpp/2, 1kHz, 30dB Gain	-	906	-	mFFS
	SNR(A-weighted)		-	83	-	dB
	THD+N		-	-77	-	dB
	Output Level	MICP=0.0745Vpp/2,MICN=0.0745Vpp/2, 1kHz, 33dB Gain	-	906	-	mFFS
	SNR(A-weighted)		-	80	-	dB
	THD+N		-	-75	-	dB
	Output Level	MICP=0.0528pp/2,MICN=0.0528Vpp/2, 1kHz, 36dB Gain	-	906	-	mFFS
	SNR(A-weighted)		-	78	-	dB
	THD+N		-	-73	-	dB

5.8 Clock Electrical Characteristics

5.8.1 High Frequency Reference Clock

Table 5-8 External Reference Clock Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{IN}	Clock input frequency list using an external clock source	-	40/24	-	MHz
	Clock input frequency list using a XTAL and the built-in oscillator	-	40/24	-	MHz
F_{INTOL}	Tolerance on input frequency without trimming	-20	-	+20	ppm
T_{stable}	Clock stabilization time	-	-	10	ms
I_{LEAK}	Input leakage current, both for analog and digital	-	-	1	uA

5.8.1.1 Clock Source Detection

An integrated automatic detection mechanism detects the clock source from the connections of the DXIN and DXOUT pins:

- When an external reference clock source is used, the clock input pin is DXIN. This device supports both an analog and digital source. An analog source shall be AC coupled to DXIN while a digital source shall be DC coupled to DXIN. In both cases, DXOUT shall be floating.
- When a XTAL and the built-in oscillator are used, the XTAL shall be DC coupled to DXIN and DXOUT.

5.8.1.2 External Clock Source

Table 5-9 External Clock Requirements

Symbol	Parameter	Min.	Typ.	Max.	Unit
AC coupled signal					
F_{IN}	Frequency	-	40/24	-	MHz
V_{PP}	Peak-to-peak voltage range of the AC coupled analog input	0.6	1.0	1.5	V
N_H	Total harmonic content of the input signal	-	-	-25	dBc

Symbol	Parameter	Min.	Typ.	Max.	Unit
DC coupled signal					
V_{IL}	input low voltage on DXIN	0	-	0.3*1.5	V
V_{IH}	input high voltage on DXIN	0.7*1.5	-	1.5	V
Tr/T_f	10%-90% rise and fall time	-	-	5	ns
Duty Cycle	Cycle-to-cycle	40	50	60	%
Both analog and digital signals					
Phase Noise	Ref clock @ 24/40 MHz, 2.4 GHz 802.11b/g/n operation @1 kHz @10 kHz @100 kHz @1 MHz	-	-	 -125 -135 -145 -145	dBc/Hz

5.8.1.3 External XTAL and Built-in Oscillator

Table 5-10 External High Frequency Crystal Characteristics Requirements

Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		-	40/24	-	MHz
ESR		-	-	60	Ω
Cin_xtal[1]	Single-ended	0	-	25.4	pF
Load Capacitance[1]		-	16	27	pF
Oscillator Tuning Range[2]		+/-20	+/-50	+/-70	ppm
Crystal Frequency Accuracy at Nominal Temp.	25 °C	-10	-	+10	ppm
Crystal Drift Due to Temperature	-20 to +85 °C	-10	-	+10	ppm
Crystal Pull Ability		10	-	150	ppm/pF

NOTE

1. The load capacitance value (C_{load}) and shunt capacitance value(C_{shunt}) depends on XTAL model. DXOUT and DXIN pin have inside capacitance (C_{in_xtal}), so external added load capacitance value (PCB Welding Capacitance) C_{load_ext} = C_{load} * 2 - C_{in_xtal} - C_{pcb} - C_{shunt} * 2, C_{pcb} is PCB parasitic capacitance (single-ended). C_{in_xtal} has tuning range about 25.4pF, which is controlled by software.

2. Tuning range depends on XTAL load capacitance requirement, typical case is based on 24/40MHz XTAL, 16pF Cload.

5.8.2 Low Frequency Reference Clock

This device uses low frequency reference clock for option. It can use an external low frequency crystal, or a built-in oscillator, or internal RCOSC. The external crystal and a built-in oscillator is used during power save modes.

5.8.2.1 External XTAL and Built-in Oscillator

Table 5-11 External Low Frequency Crystal Characteristics Requirements

Symbol	Conditions	Min.	Typ.	Max.	Unit
Nominal Frequency	-	-	32.768	-	KHz
Load Capacitance[1]	-	-	-	-	pF
C_{shunt}1	-	-	2	-	pF

NOTE

The load capacitance value (C_{load}) and shunt capacitance value (C_{shunt}) depends on LXTAL model, external added load capacitance value (PCB Welding Capacitance) C_{load_ext} = C_{load} * 2 - C_{pcb} - C_{shunt} * 2, C_{pcb} is PCB parasitic capacitance (single-ended).

5.8.2.2 Internal RCOSC Reference Clock Source

This device has an integrated RC oscillator low frequency reference clock source inside. This clock is calibrated by CPU clock source from high frequency reference. RCOSC takes effect automatically when there is no external crystal.

5.9 Wi-Fi 2.4G RF Receiver Specification

Test Condition: VBAT= 5 V, VCC15-ANA= 1.5 V, Temperature= 25 °C

Table 5-12 Wi-Fi 2.4G RF Receiver Specifications

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412	2442	2484	MHz
RX Sensitivity (802.11b)	1Mbps DSSS	-	-97	-95	dBm
	2Mbps DSSS	-	-95.2	-93.2	dBm
	5.5Mbps CCK	-	-93.1	-91.1	dBm
	11Mbps CCK	-	-90	-88	dBm
RX Sensitivity (802.11g)	6Mbps OFDM	-	-93.1	-91.1	dBm
	9Mbps OFDM	-	-92	-90	dBm
	12Mbps OFDM	-	-91	-89	dBm
	18Mbps OFDM	-	-88	-86	dBm
	24Mbps OFDM	-	-85.5	-83.5	dBm
	36Mbps OFDM	-	-82.1	-80.1	dBm
	48Mbps OFDM	-	-78.0	-76.0	dBm
	54Mbps OFDM	-	-76.7	-74.7	dBm
RX Sensitivity (802.11n, 20MHz)	MCS 0	-	-92.7	-90.7	dBm
	MCS 1	-	-89.5	-87.5	dBm
	MCS 2	-	-87.1	-85.1	dBm
	MCS 3	-	-84.4	-82.4	dBm
	MCS 4	-	-81.2	-79.2	dBm
	MCS 5	-	-77.1	-75.1	dBm
	MCS 6	-	-75.3	-73.3	dBm
	MCS 7	-	-74	-72	dBm
Maximum Receive Level	6 Mbps OFDM	-	0.0	-	dBm
	54 Mbps OFDM	-	-1.0	-	dBm
	MCS0	-	-3.0	-	dBm
	MCS7	-	-1.0	-	dBm
	1 Mbps CCK	41	43	-	dBc

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Receive Adjacent Channel Rejection	11 Mbps CCK	36	38	-	dBc
	BPSK rate 1/2, 6 Mbps OFDM	29	31	-	dBc
	64QAM rate 3/4, 54 Mbps OFDM	15	17	-	dBc
	HT20, MCS 0, BPSK rate 1/2	28	30	-	dBc
	HT20, MCS 7, 64QAM rate 5/6	9	11	-	dBc

NOTE

The minimum limit considers the variation of process, voltage and temperature.

5.10 Wi-Fi 2.4G RF Transmitter Specification

Test Condition: VBAT= 5 V, VCC15-ANA= 1.5 V, Temperature= 25 °C

Table 5-13 Wi-Fi 2.4G RF Transmitter Specifications

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412	2442	2484	MHz
TX output Power with mask and EVM compliance[1]	1Mbps DSSS	20.7	21.2	-	dBm
	11Mbps CCK	20.9	21.4	-	dBm
	6Mbps OFDM	17.7	18.2	-	dBm
	54Mbps OFDM	16	16.5	-	dBm
	HT20, MCS 0	17.7	18.2	-	dBm
	HT20, MCS 7	15.5	16	-	dBm
TX EVM	1Mbps DSSS	-	-22.2	-20.2	dB
	11Mbps CCK	-	-21.8	-19.8	dB
	6Mbps OFDM	-	-26.3	-24.3	dB
	54Mbps OFDM	-	-27.7	-25.7	dB

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
	HT20, MCS 0	-	-26.8	-24.8	dB
	HT20, MCS 7	-	-31.7	-29.7	dB
Carrier Suppression		-	-	-40	dBc
Accuracy of Power Control	Closed-loop control across all temperature ranges and channels	-1.5	-	+1.5	dB
Harmonic Output Power	2nd Harmonic	-	-41	-	dBm/MHz
	3rd Harmonic	-	-31	-	dBm/MHz

NOTE

1. Refer to IEEE 802.11 specification for Tx spectrum limits:

   802.11b mask (18.4.7.3)

   802.11g mask (19.5.4)

   802.11g EVM (17.3.9.6.3)

   802.11n HT20 mask (20.3.21.1)

   802.11n HT20 EVM (20.3.21.7.3)

2. The minimum limit considers the variation of process, voltage and temperature.

5.11 Wi-Fi Power Consumption

Table 5-14 Wi-Fi Power Consumption

Test Condition: Temperature= 25 °C, VBAT= 4.2V, VCC15-ANA= 1.5V

Symbol	MCU State	Wi-Fi State	TX/RX	Test Condition		Performance			
				(Signaling Mode)		Min	Typ(1)	Max	Unit
ACTIVE	ACTIVE	ACTIVE	TX	1M DSSS	17dBm	-	492	-	mA
				11M CCK	17dBm	-	504	-	mA
				6M OFDM	16dBm	-	347	-	mA
				54M OFDM	16dBm	-	349	-	mA

Symbol	MCU State	Wi-Fi State	TX/RX	Test Condition (Signaling Mode)		Performance Min	Typ(1)	Max	Unit
				HT20, MCS0	16dBm	-	349	-	mA
				HT20, MCS7	15dBm	-	346	-	mA
STAND BY	SLEEP	ACTIVE	TX	1M DSSS, null frame	17dBm	-	403	-	mA
			RX	RX listen	-	-	27.2	-	mA
				1M DSSS	-	-	27	-	mA
		PS Mode	RX	DTIM1	-	-	630	-	μA
				DTIM3	-	-	282	-	μA
				DTIM8	-	-	180	-	μA
				DTIM10	-	-	166	-	μA
		OFF	-	-	-	-	107	-	μA
HIBERN ATION	OFF	OFF	-	-	-	-	11.8	-	μA

(1) Actual Wi-Fi power consumption will be affected by PVT.

5.12 Interface Timing Characteristics

5.12.1 SMHC Interface Timing

5.12.1.1 HS-SDR Mode

NOTE

IO voltage is 3.3V.

Figure 5-2 SMHC HS-SDR Mode Output Timing Diagram

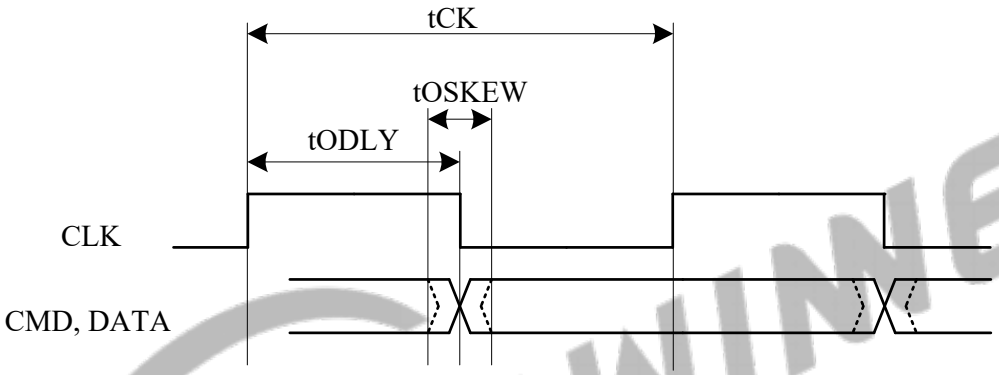


Table 5-15 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 5-3 SMHC HS-SDR Mode Input Timing Diagram

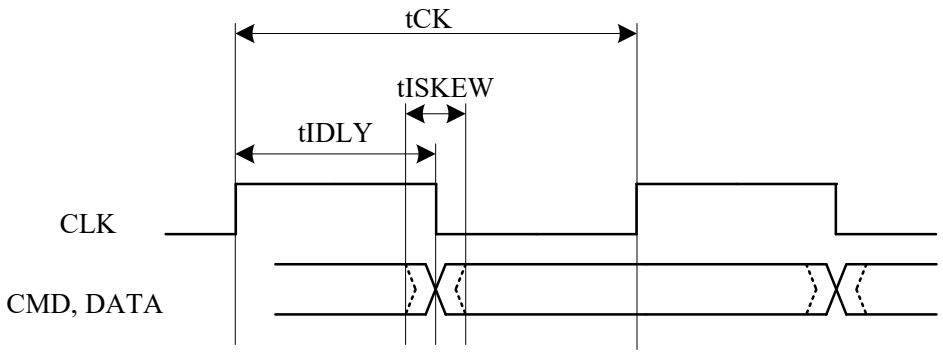


Table 5-16 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

5.12.1.2 HS-DDR Mode

Figure 5-4 SMHC HS-DDR Mode Output Timing Diagram

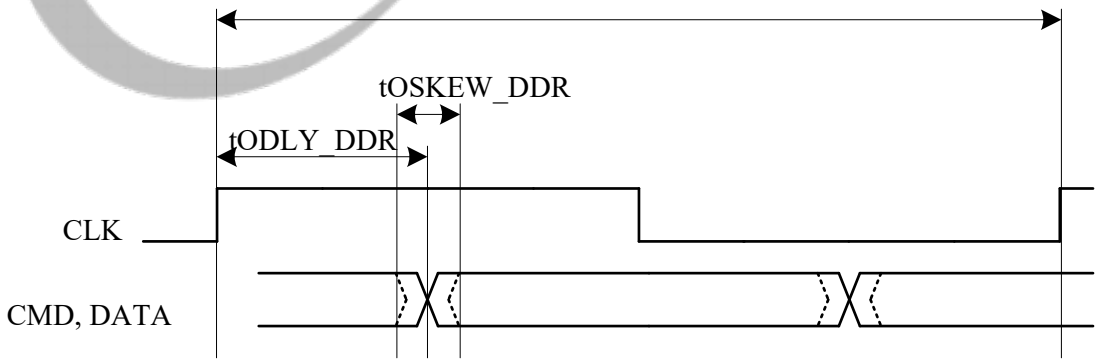


Table 5-17 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY-DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 5-5 SMHC HS-DDR Mode Input Timing Diagram

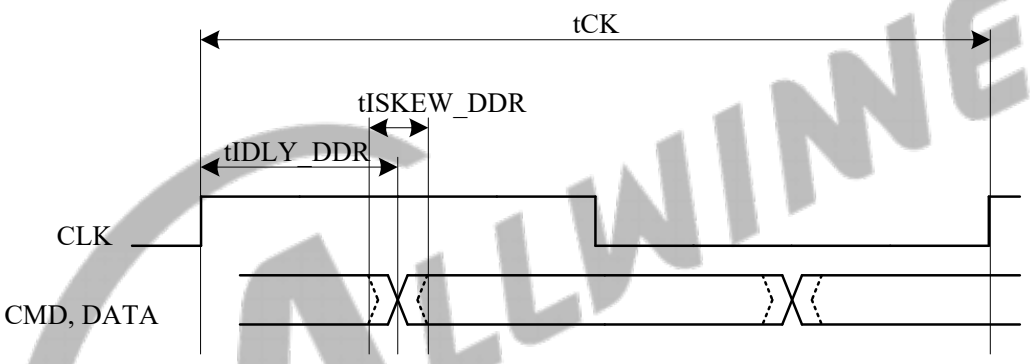


Table 5-18 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY-DDR	-	-	8.3	ns
Data input skew time in DDR mode	tISKEW-DDR	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

5.12.2 LCD Interface Timing

Figure 5-6 HV_IF Vertical Timing

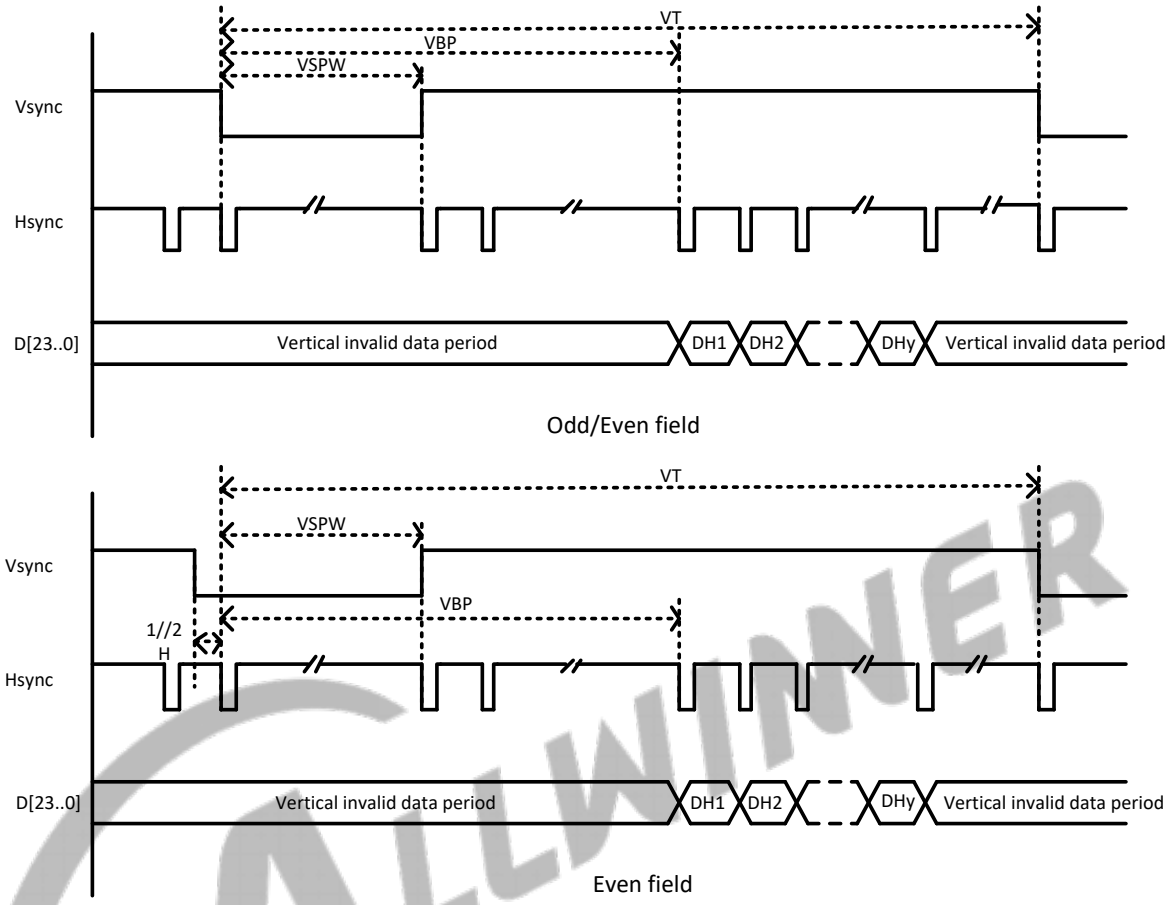
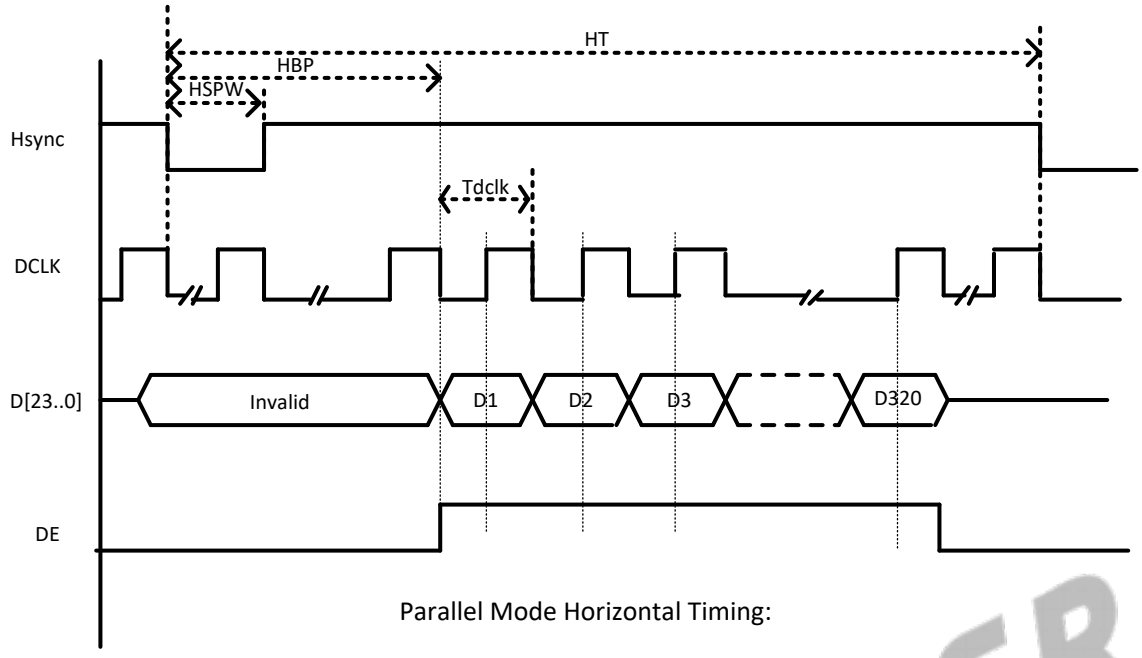
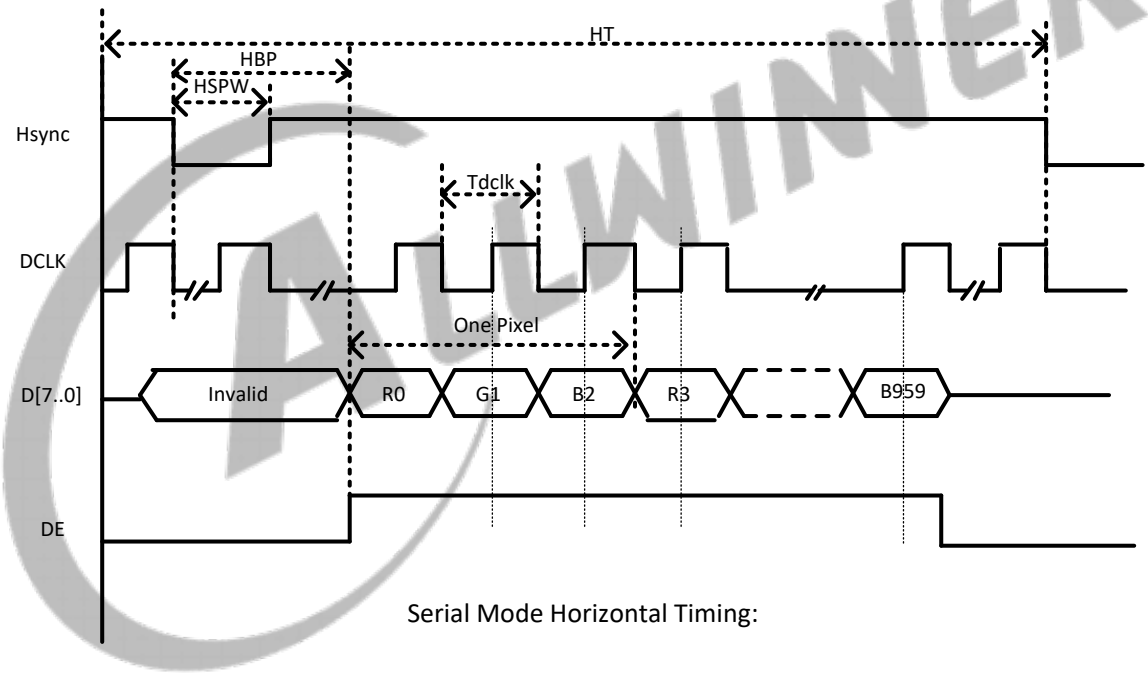


Figure 5-7 HV_IF Horizontal Timing



Parallel Mode Horizontal Timing:



Serial Mode Horizontal Timing:

Table 5-19 LCD HV_IF Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK Cycle Time	tDCLK	11.4	-	-	ns
Hsync Period Time	tHT	-	HT+1	-	tDCLK
Hsync Width	tHSPW	-	HSPW+1	-	tDCLK
Hsync Back Porch	tHBP	-	HBP+1	-	tDCLK
Vsync Period Time	tVT	-	VT/2	-	tHT
Vsync Width	tVSPW	-	VSPW+1	-	tHT

Parameter	Symbol	Min	Typ	Max	Unit
Vsync Back Porch	tVBP	-	VBP+1	-	tHT
(1) Vsync: Vertical sync, indicates one new frame. (2) Hsync: Horizontal sync, indicate one new scan line. (3) DCLK: Dot clock, pixel data are sync by this clock. (4) LDE: LCD data enable. (5) LCD[7..3], LCD [12..10]: 8 Bit RGB/YUV output from input FIFO for panel.					

5.12.3 MIPI CSI Interface Timing

Figure 5-8 MIPI CSI Interface Timing

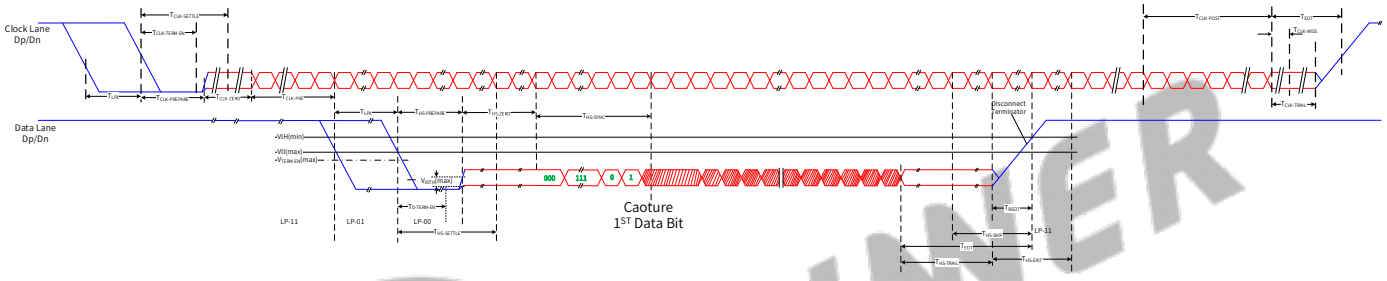


Table 5-20 MIPI CSI Interface Timing Constants

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	(1),(6)
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns	(5)
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	(5)
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	(5)
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane	95		300	ns	(6),(7)

Parameter	Description	Min	Typ	Max	Unit	Notes
	HS transitions, starting from the beginning of TCLK-PREPARE.					
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns	(6)
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns	(5)
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns	(5)
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35ns + 4*UI		(6)
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.			105ns + n*12*UI		(3),(5)
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns	(5)
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85ns + 6*UI	ns	(5)
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns	(5)
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns + 6*UI		145ns + 10*UI	ns	(6)

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40			ns	(6)
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60ns + n*4*UI)			ns	(2), (3), (5)
T_{INIT}		100			ns	(5)
T_{LPX}	Transmitted length of any Low-Power state period	50			ns	(4), (5)
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2	ns	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX}$			ns	(5)
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX}$			ns	(5)
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		$2*T_{LPX}$	ns	(5)
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	(5)

NOTE

(1) The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

(2) If a > b then max (a, b) = a otherwise max (a, b) = b.

(3) Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode.

(4) TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

(5) Transmitter-specific parameter.

(6) Receiver-specific parameter.

(7) The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.

5.12.4 Parallel CSI Interface Timing

Figure 5-9 Parallel CSI Data Sample Timing

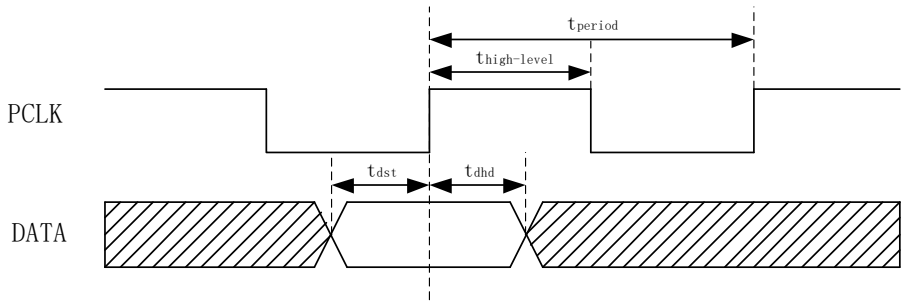


Table 5-21 Parallel CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.73	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

5.12.5 Ethernet MAC Interface Timing

Figure 5-10 RMII Receive Timing

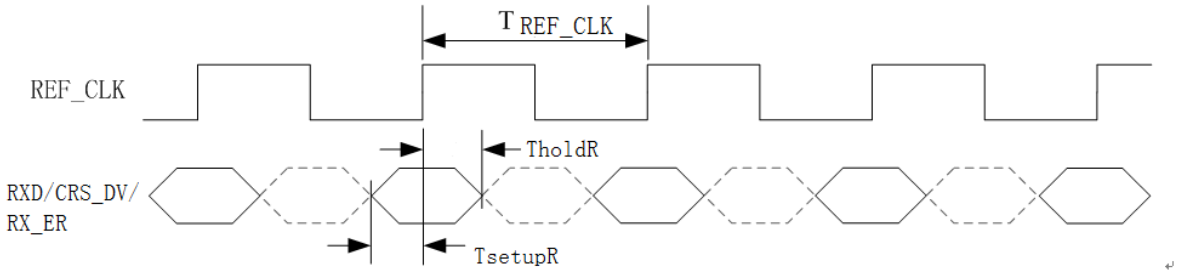


Figure 5-11 RMII Transmit Timing

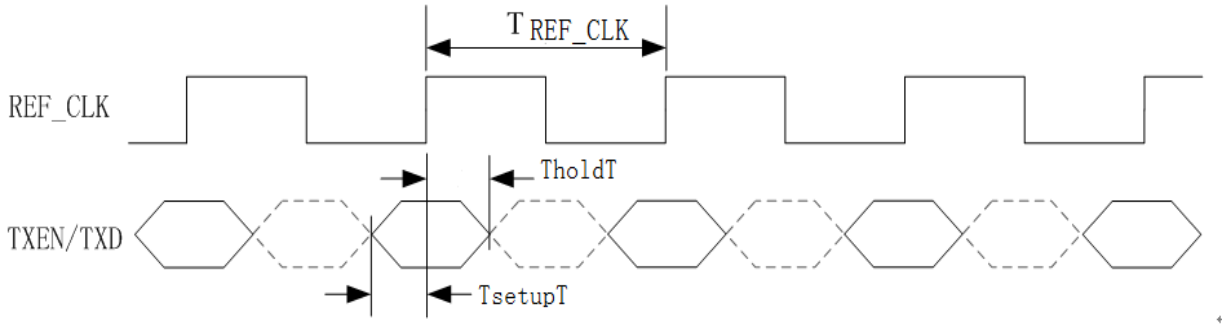


Table 5-22 RMII Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
T_{REF_CLK}	Reference Clock Period	-	20	-	ns
Tduty	REF_CLK duty cycle	35		65	%
TsetupT	TXD/TXEN to REF_CLK setup time	4			ns
TholdT	TXD/TXEN to REF_CLK hold time	2			ns
TsetupR	RXD/CRS_DV/RX_ER to REF_CLK setup time	4			ns
TholdR	RXD/CRS_DV/RX_ER to REF_CLK hold time	2			ns

5.12.6 SPI Interface Timing

Figure 5-12 SPI Writing Timing

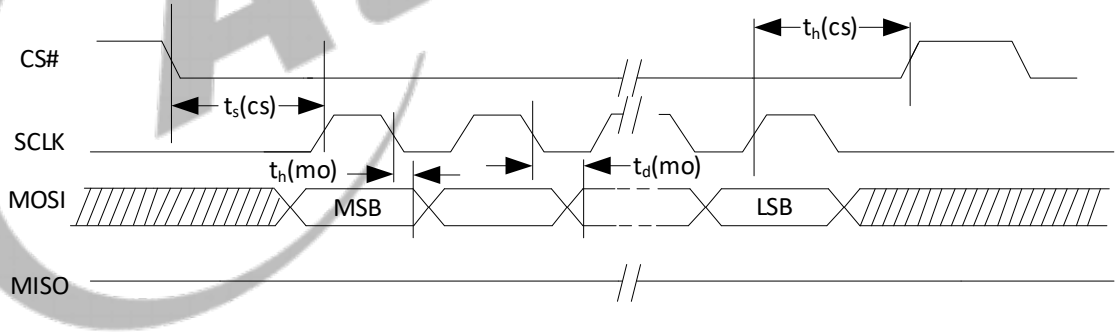


Figure 5-13 SPI Reading Timing

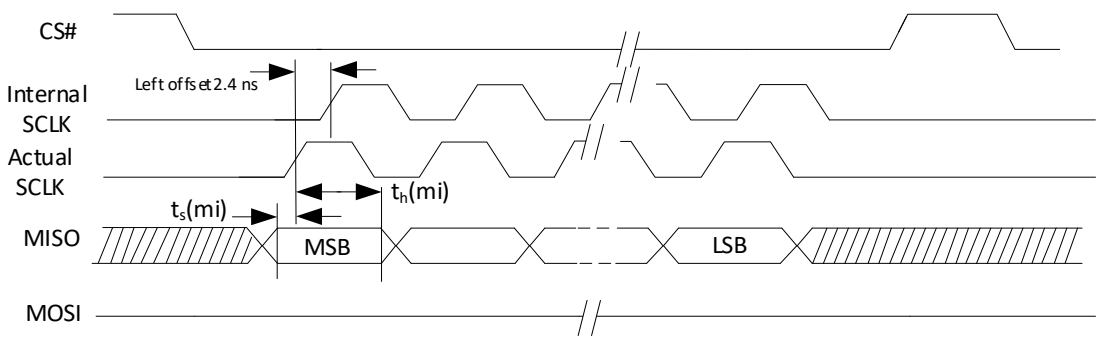


Table 5-23 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	t_s(cs)	-	2T(1)	-	ns
CS# Active Hold Time	t_h(cs)	-	2T(1)	-	ns
Data output Delay Time	t_v(mo)	-	T(1)/2-3	-	ns
Data output Hold Time	t_h(mo)	-	T(1)/2-3	-	ns
Data In Setup Time	t_s(mi)	0.2	-	-	ns
Data In Hold Time	t_h(mi)	0.2	-	-	ns
(1) T is the cycle of clock.					

5.12.7 SPI-DBI Interface Timing

Figure 5-14 DBI 3-line Serial Interface Timing

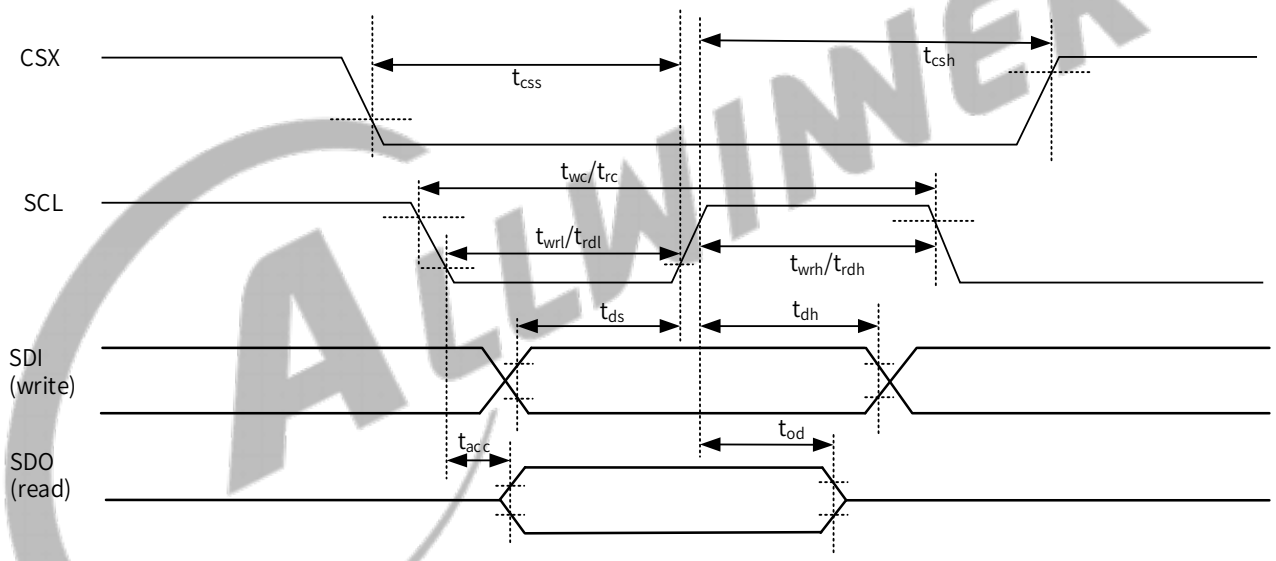


Table 5-24 DBI 3-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns

Signal	Parameter	Symbol	Min	Max	Unit
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-25 DBI 3-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	10(1)	50	ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-6.67 MHz.					

Figure 5-15 DBI 4-line Serial Interface Timing

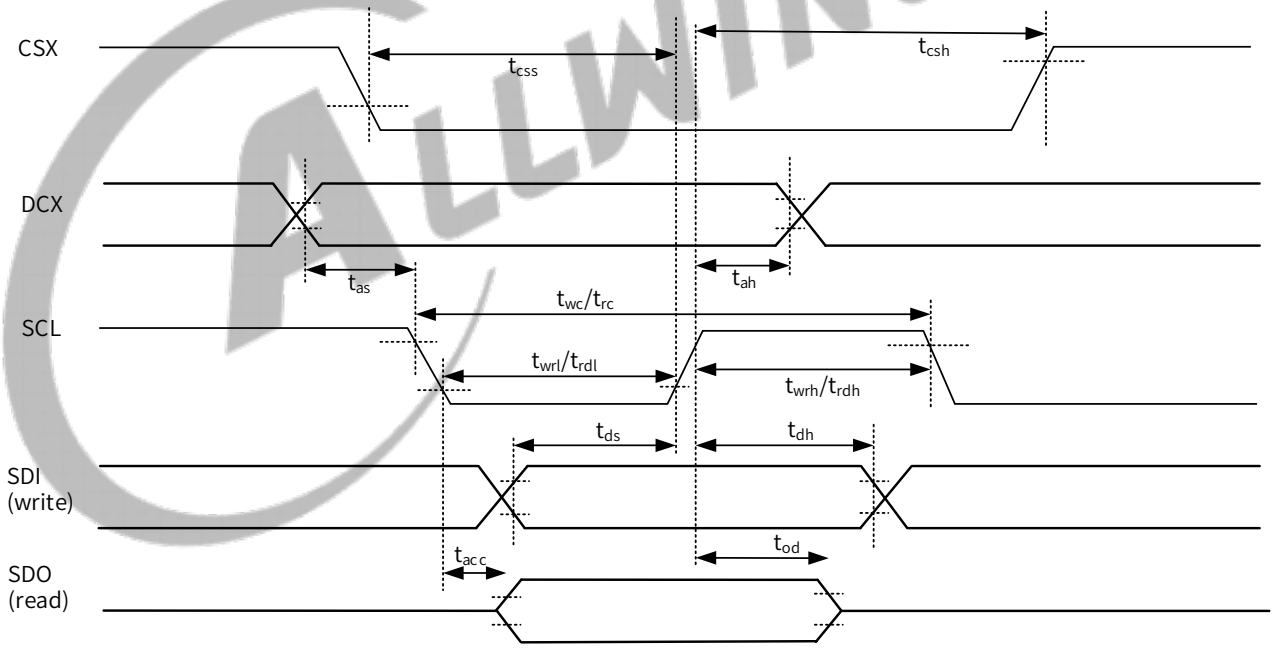


Table 5-26 DBI 4-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Write cycle	t_{wc}	16		ns

Signal	Parameter	Symbol	Min	Max	Unit
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-27 DBI 4-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-6.67 MHz.					

5.12.8 UART Interface Timing

Figure 5-16 UART RX Timing

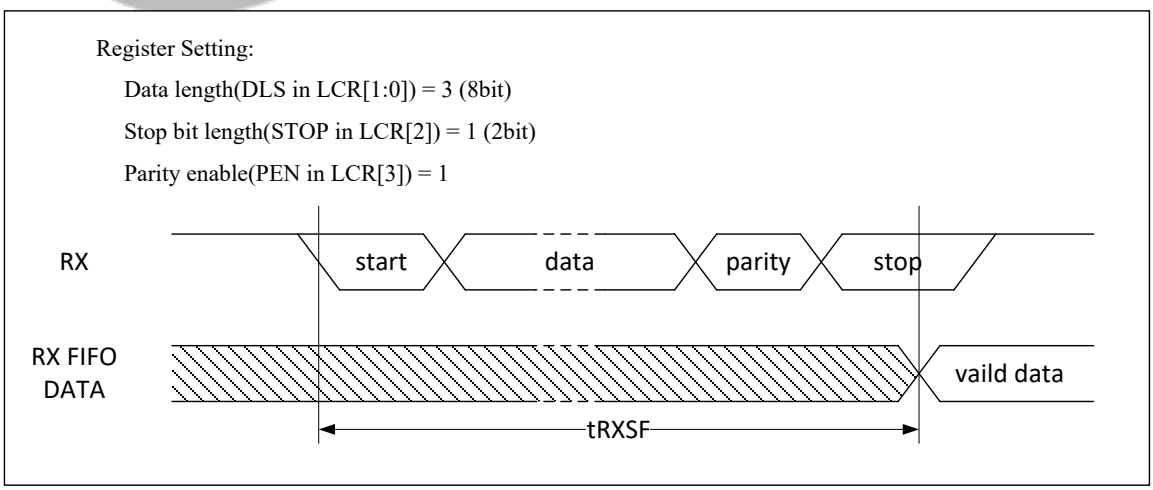


Figure 5-17 UART nCTS Timing

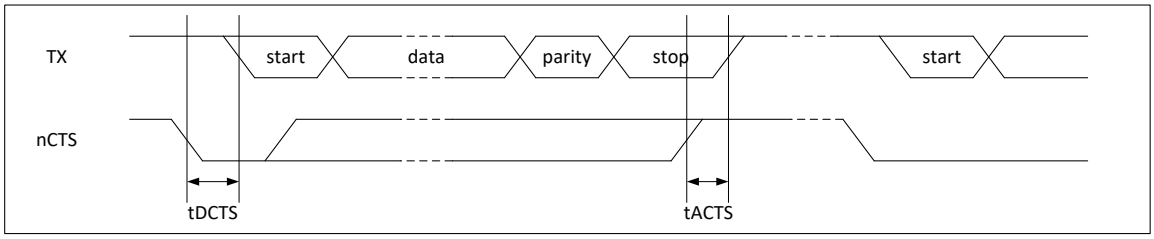


Figure 5-18 UART nRTS Timing

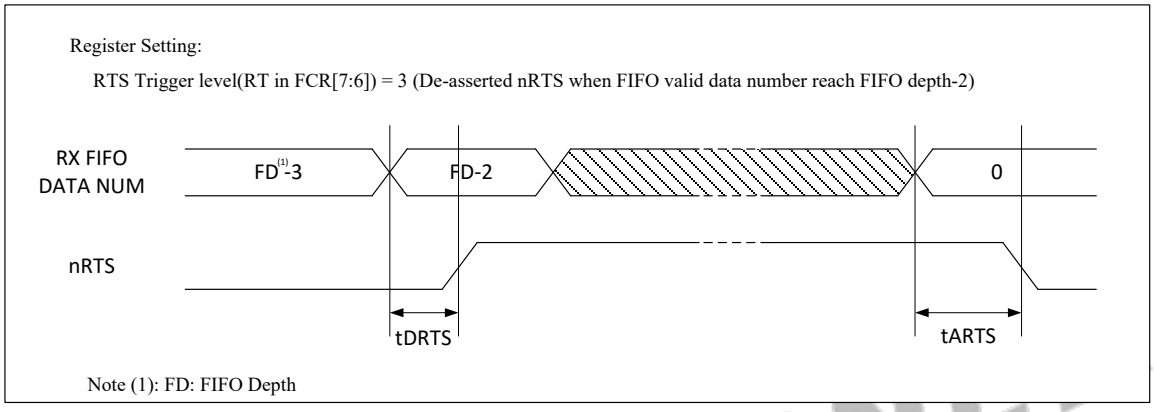


Table 5-28 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5*BRP(1)	-	11*BRP(1)	ns
Delay time of de-asserted nCTS to TX strat	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
(1) BRP: Baud-Rate Period.					

5.12.9 TWI Interface Timing

Figure 5-19 TWI Timing

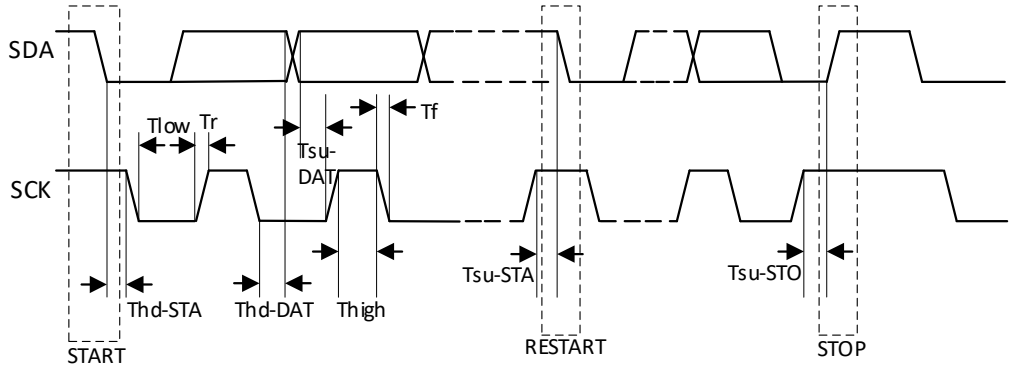


Table 5-29 TWI Timing Parameters

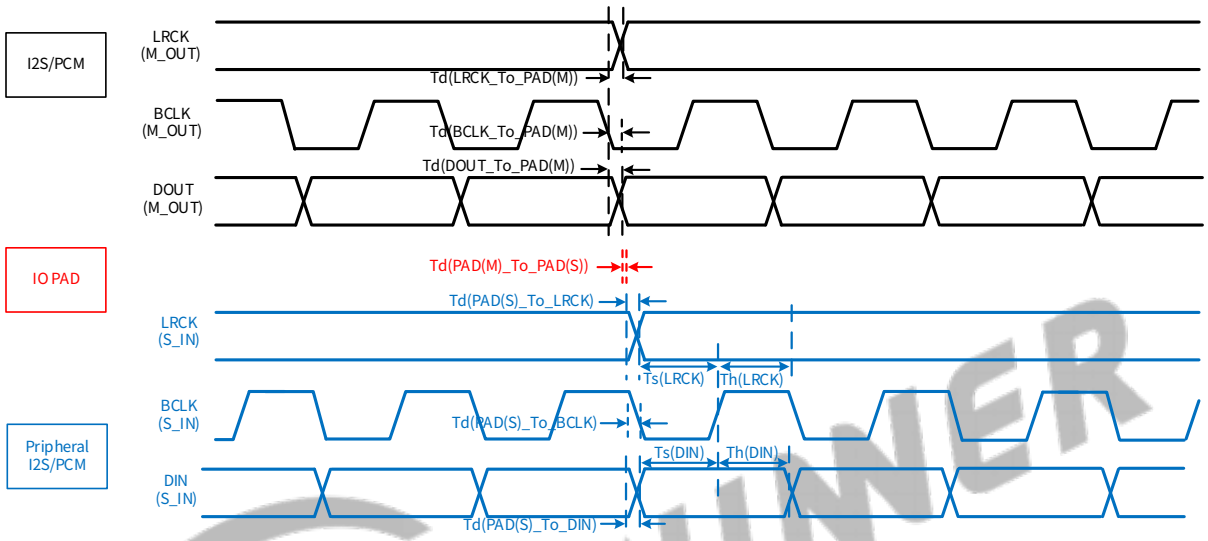
Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data	Thd-DAT	5.0	-	-	-	us
Setup Time In Stop	Tsu-STO	4.0	-	0.6	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us
SCK High level Time	Thigh	4.0	-	0.6	-	us
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

5.12.10 I2S/PCM Interface Timing

5.12.10.1 Data Output timing of I2S/PCM in Master mode

The Data Output timing of I2S/PCM in Master mode and the Data Input timing of Peripheral I2S/PCM in Slave mode show in Figure 5-20.

Figure 5-20 Data Output Timing of I2S/PCM in Master Mode



The Data Output timing parameters of I2S/PCM in Master mode and The Data Input timing parameters of Peripheral I2S/PCM in Slave mode show in Table 5-30.

Table 5-30 Data Output Timing Parameters of I2S/PCM in Master Mode

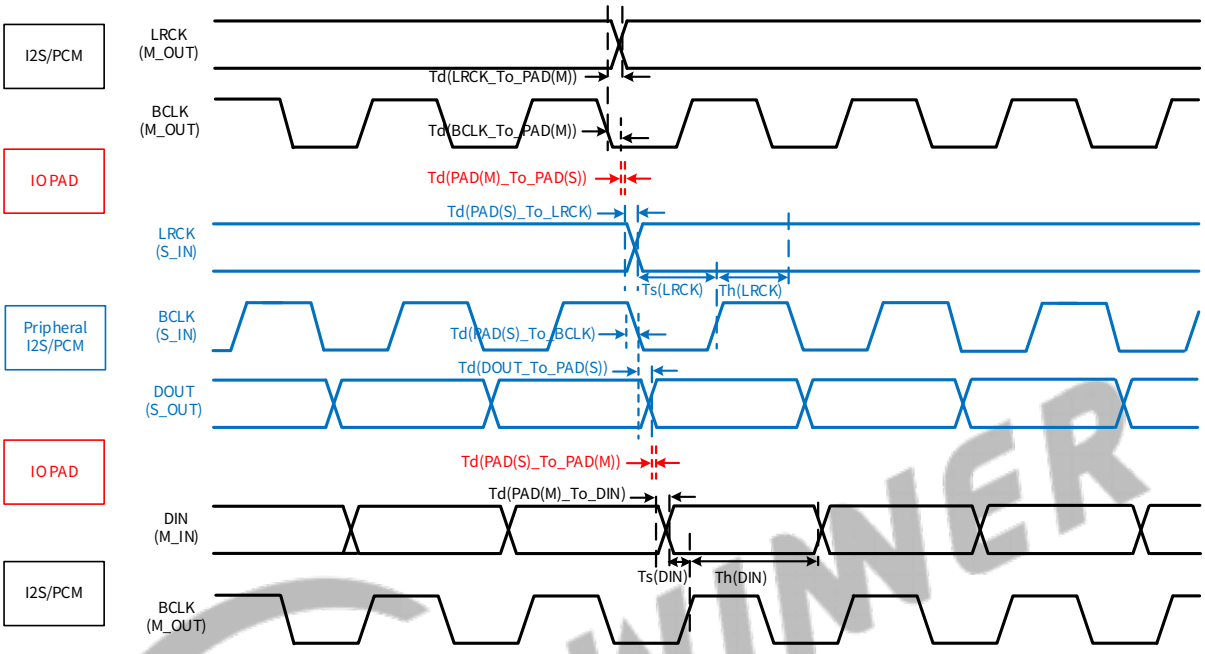
Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
T_d(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5 (restriction)	T_w1<2.5(requirement)	ns
T_d(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(restriction)		
T_d(DOUT_To_PAD(M))	DOUT to PAD(M) Delay	/	T3<6.5(restriction)		
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
T_d(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T4*<7.0(estimation)	T_w2*<1.0(requirement)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay	/	T5*<7.0(estimation)		

Parameter		Min	Max	Skew	Units
	DOUT PAD(M) to DIN PAD(S) Delay	/	T6*<7.0(estimation)		
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
T_d(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T7*<6.5(assumption)	T_w3*<2.5(requirement)	ns
T_d(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T8*<6.5(assumption)		
T_d(PAD(S)_To_DIN)	PAD(S) to DIN Delay	/	T9*<6.5(assumption)	/	/
T_s(LRCK)	LRCK Setup Slack	T10*(analysis)	/	/	ns
T_h(LRCK)	LRCK Hold Slack	T11*(analysis)	/	/	ns
T_s(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
T_h(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

5.12.10.2 Data Input timing of I2S/PCM in Master mode

The Data Input timing of I2S/PCM in Master mode and the Data Output timing of Peripheral I2S/PCM in Slave mode show in Figure 5-21.

Figure 5-21 Data Input Timing of I2S/PCM in Master Mode



The Data Input timing parameters of I2S/PCM in Master mode and The Data Output timing parameters of Peripheral I2S/PCM in Slave mode are shown in Table 5-31.

Table 5-31 Data Input Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5(requirement)	Tw1<2.5 (estimation)	ns
Td(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(requirement)		ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T3*<7.0(requirement)	Tw2*<1.0 (estimation)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay		T4*<7.0(requirement)		

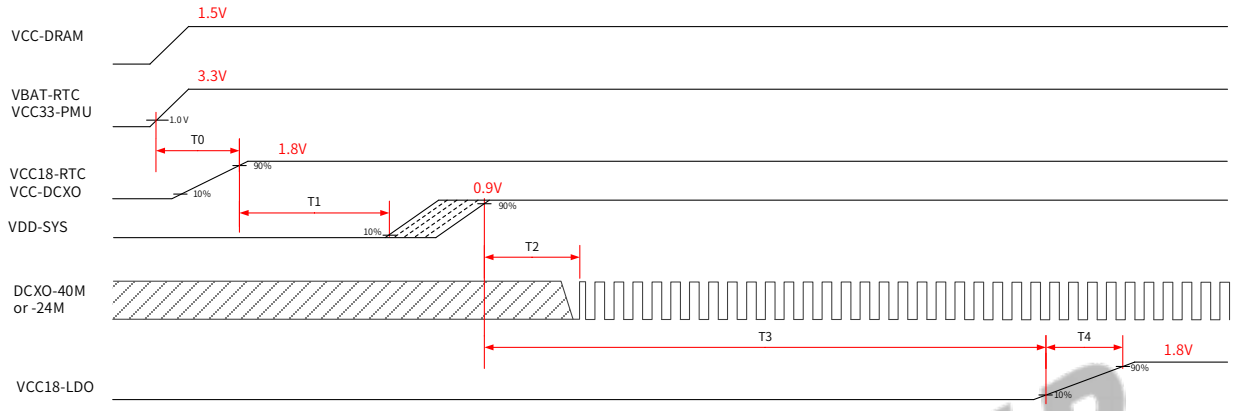
Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T5*<6.5(requirement)	Tw3*<2.5 (estimation)	ns
Td(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T6*<6.5(requirement)		ns
Td(DOUT_To_PAD(S))	DOUT to PAD(S) Delay	/	T7*<6.5(requirement)	/	ns
Ts(LRCK)	LRCK Setup Slack	T8*(analysis)	/	/	ns
Th(LRCK)	LRCK Hold Slack	T9*(analysis)	/	/	ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_PAD(M))	DOUT PAD(S) to DIN PAD(M) Delay	/	T10*<7.0(requirement)	/	ns
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(PAD(M)_To_DIN)	PAD(M) to DIN Delay	/	T11<6.5(requirement)	/	ns
Ts(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
Th(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

5.13 Power-Up and Power-Down Sequence

5.13.1 Power-Up Sequence

The following figure shows an example of the power on sequence for this device.

Figure 5-22 Power-Up Sequence



NOTE

- There is no power-up step requirement between VCC-DRAM and other power supplies.
- VDD-SYS is powered by external DC-DC devices. The actual settle time of VDD-SYS is determined by the specific device used.
- The start-oscillation time of the DCXO is determined by the specific device used.

The following table represents the timing parameters of the power-up sequence.

Table 5-32 Timing Parameters of Power-Up Sequence

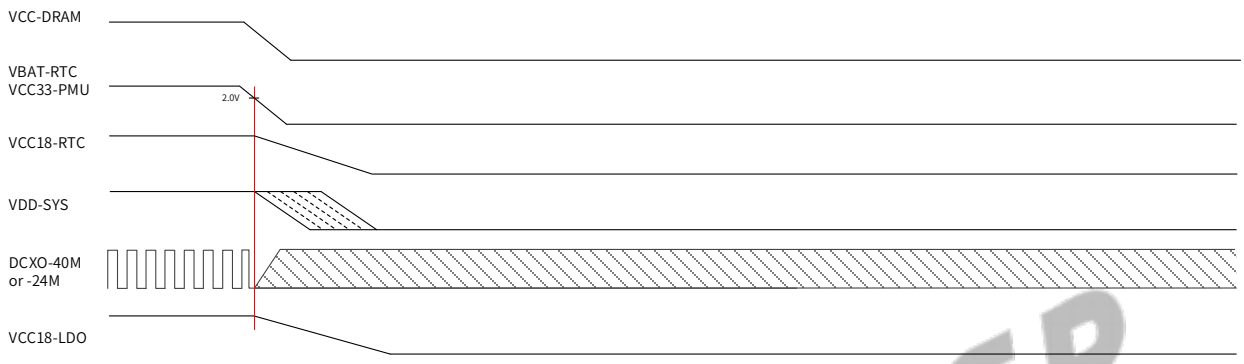
Parameters	Description	Min	Typ	Max	Unit
T0	Delay from VBAT-RTC/VCC33-PMU start ramp-up to VCC18-RTC/VCC-DCXO stable	80	-	-	us
T1	Delay from VCC18-RTC/VCC-DCXO stable to VDD-SYS start ramp-up.	1.1	-	3.5	ms
T2	Delay from VDD-SYS stable to DCXO stable	0	-	-	ms
T3	Delay from VDD-SYS stable to VCC18-LDO start ramp-up	25.0	-	35.0	ms
T4	VCC18-LDO settle time	50	-	150	us

5.13.2 Power-Down Sequence

The following figure shows an example of the power down sequence for this device.

- After the VBAT-RTC and VCC33-PMU become lower than 2.0 V, the DCXO starts to stop oscillating; VCC18-RTC, VDD-SYS, and VCC18-LDO start to ramp down.
- No special restriction for VCC-DRAM.

Figure 5-23 Power-Down Sequence



6 Temperature and Thermal Characteristics

6.1.1 Temperature

The following tables describe the temperature of the device

Table 6-1 Operating and Storage Temperature

Symbol	Parameter		Min	Max	Unit
T_a	Ambient Operating Temperature	V821M2-WXX V821L2-WXX	-30	70	°C
		V821L2-XXX	-30	80	°C
T_{STG}	Storage Temperature		-55	125	°C

Table 6-2 Junction Temperature

Chip	Recommended Operating Temperature (T_j)		Absolute Maximum Junction Temperature	Unit
	Min	Max		
V821	-30	115	125	°C

6.1.2 Package Thermal Characteristics

The maximum chip junction temperature ($T_{J\,max}$) must never exceed the values given in Table 6-2 Junction Temperature.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the device. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 6-3 Package Thermal Characteristics

Symbol	Parameter	Min	Typ(1)(2)	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	30.38	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	14	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	3.66	-	°C/W

(1) Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

(2) The testing PCB is 4 layers, 114.5 mm x 76.2 mm body, and 1.6 mm thickness. Ambient temperature is 25 °C.

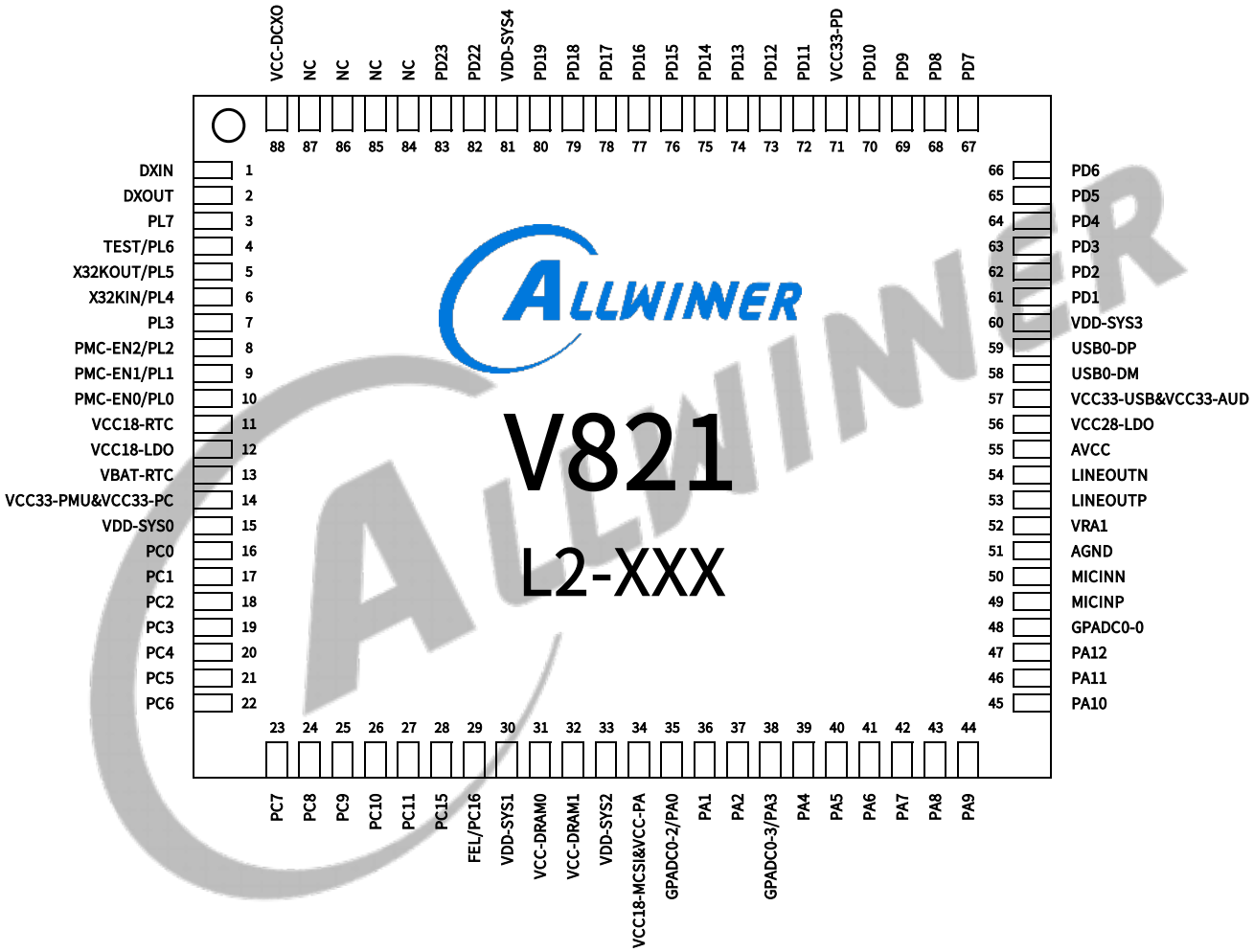
7 Pin Assignment

7.1.1 Pin Map

The following figures show the QFN 88 Pins, 9 mm x 9 mm, 0.35 mm pin pitch pin map.

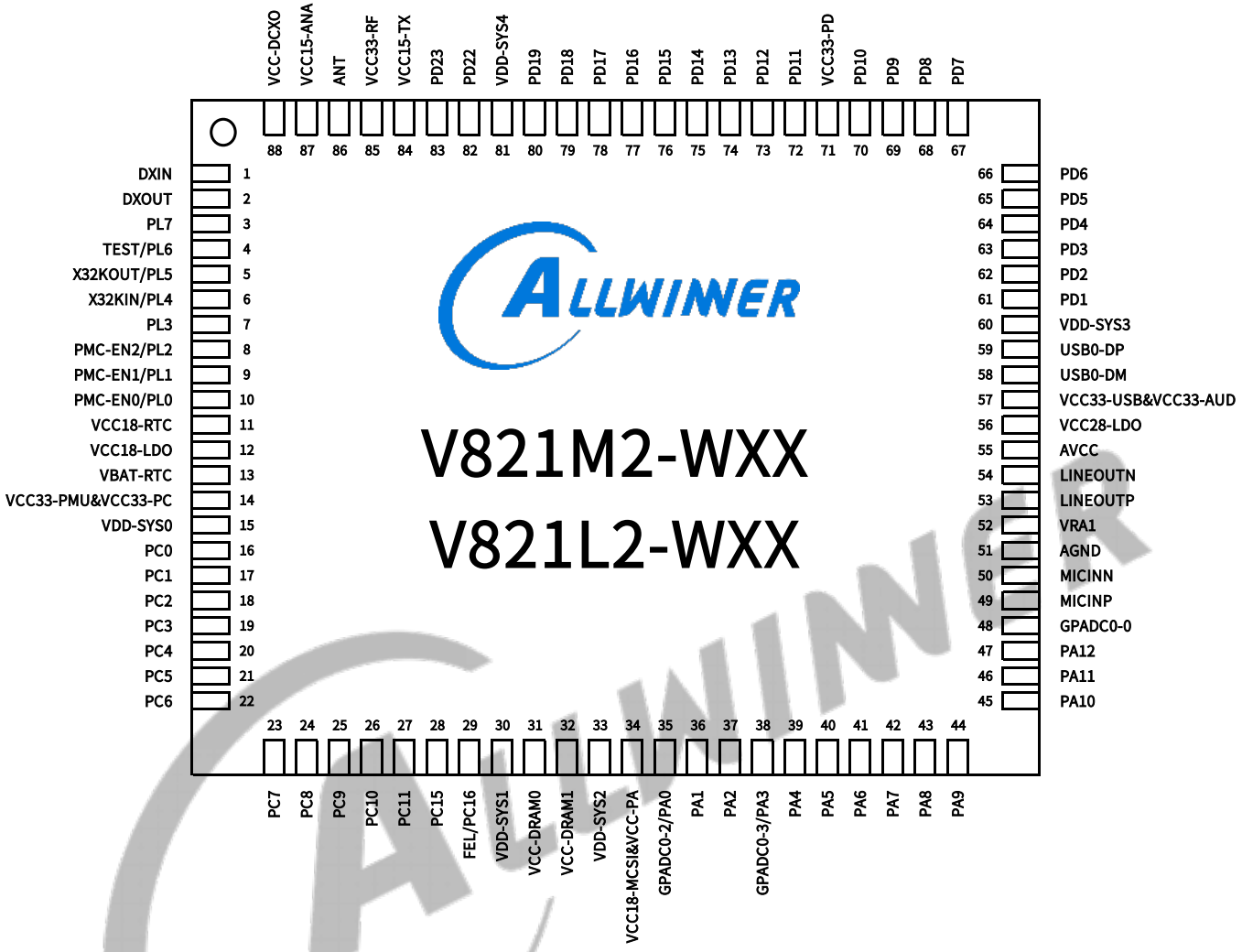
7.1.1.1 V821L2-XXX

Figure 7-1 V821L2-XXX Pin Map



7.1.1.2 V821M2-WXX/V821L2-WXX

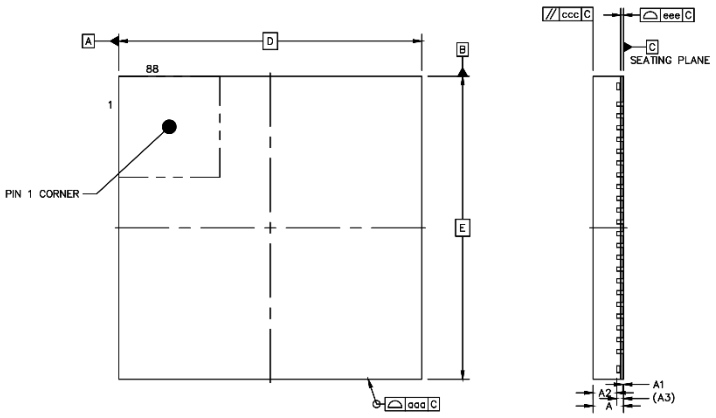
Figure 7-2 V821M2-WXX/V821L2-WXX Pin Map



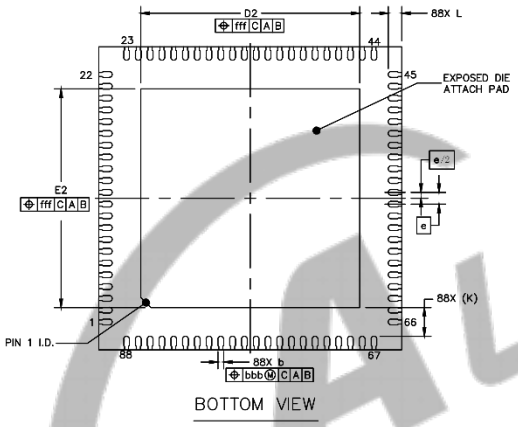
7.1.2 Package Dimension

The following figure shows the top, bottom, and side views of the QFN 88 package.

Figure 7-3 Package Dimension



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.85	0.9	0.95
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.12	0.17	0.22
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	6.4	6.5	6.6
	Y	E2	6.4	6.5	6.6
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.85 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	



NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP · Sn8~20s

8 Carrier, Storage and Backing Information

8.1 Carrier

The following table shows matrix tray carrier information.

Table 8-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	322.6 mm x 135.9 mm x 7.62 mm	260 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

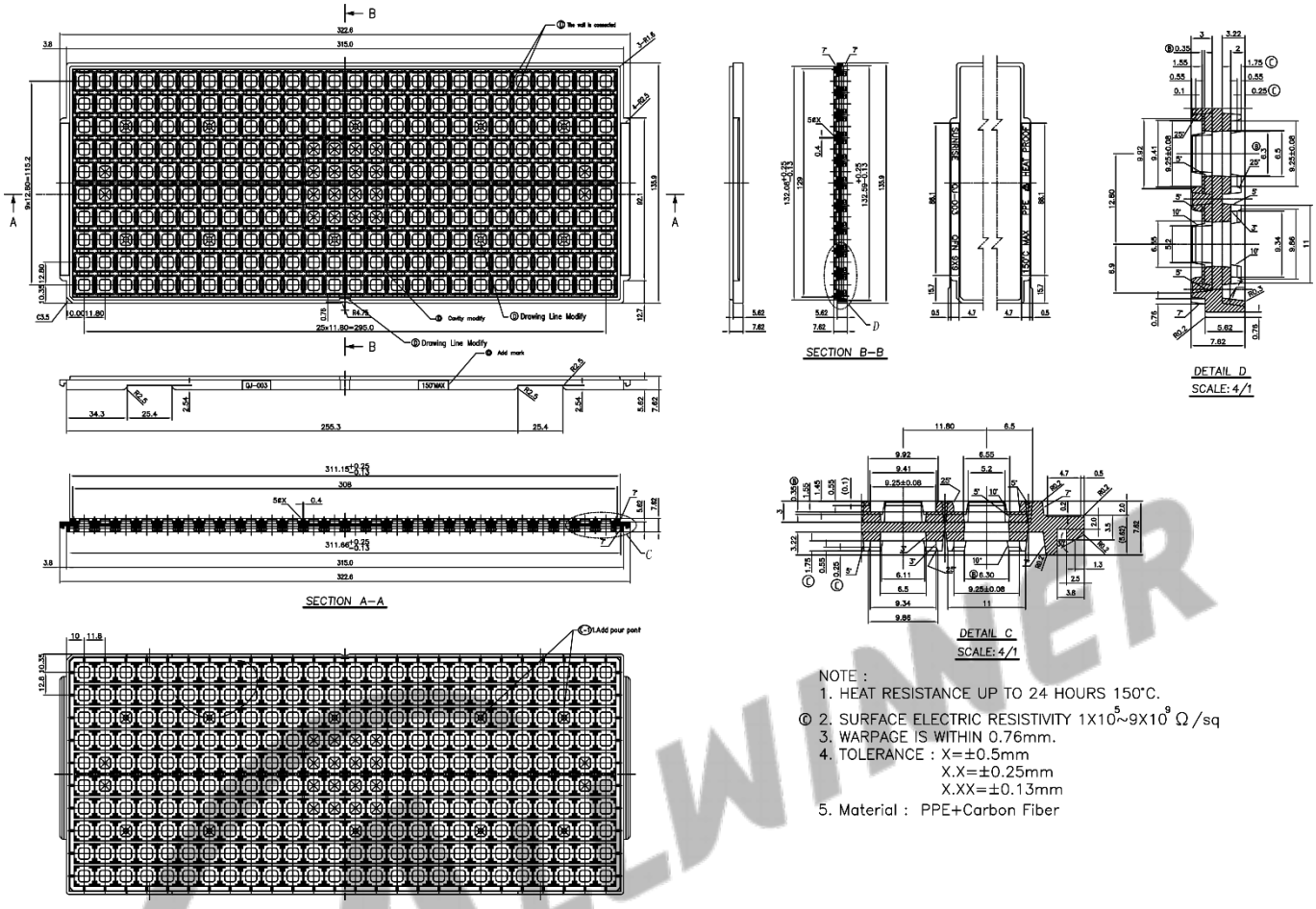
The following table shows packing quantity.

Table 8-2 Packing Quantity Information

Sample	Size	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
V821	9 mm x 9 mm	260	10	2600	6	15600

The following figure shows tray dimension drawing.

Figure 8-1 Tray Dimension Drawing



8.2 Storage

Reliability is affected if any condition specified in section 8.2.2 and section 8.2.3 has been exceeded.

8.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8-3 defines all MSL.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	⩽30°C / 85%RH
2	1 year	⩽30°C / 60%RH
2a	4 weeks	⩽30°C / 60%RH
3	168 hours	⩽30°C / 60%RH
4	72 hours	⩽30°C / 60%RH

MSL	Out-of-bag floor life	Comments
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label (TOL)	≤30°C / 60%RH

NOTE

The device samples are classified as MSL3.

8.2.2 Bagged Storage Conditions

The following table defines the shelf life.

Table 8-4 Bagged Storage Conditions

Packing Mode	Vacuum packing
Storage Temperature	20 26°C
Storage Humidity	40% 60%RH
Shelf Life	12 months

8.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration is as follows.

Table 8-5 Out-of-bag Duration

Storage Temperature	20 26°C
Storage Humidity	40% 60%RH
Moisture Sensitive Level (MSL)	3
Floor Life	168 hours

For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

8.3 Baking

It is not necessary to bake chips if the conditions specified in section 8.2.2 and section 8.2.3 have not been exceeded. It is necessary to bake chips if any condition specified in section 8.2.2 and section 8.2.3 has been exceeded.

It is necessary to bake chips if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.

9 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

The following figure shows the appropriate reflow profile.

Figure 9-1 Lead-free Reflow Profile

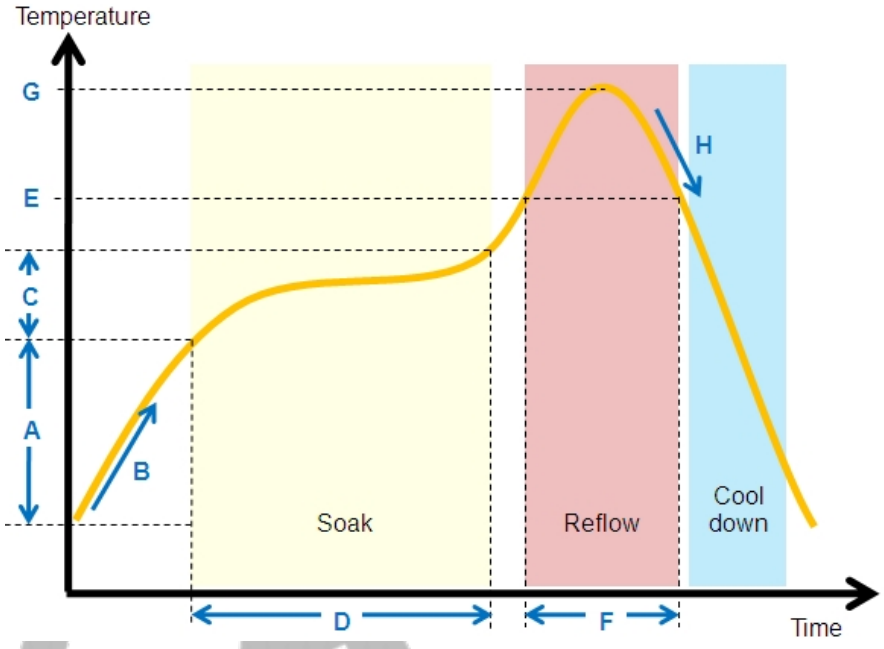


Table 9-1 Lead-free Reflow Profile Conditions

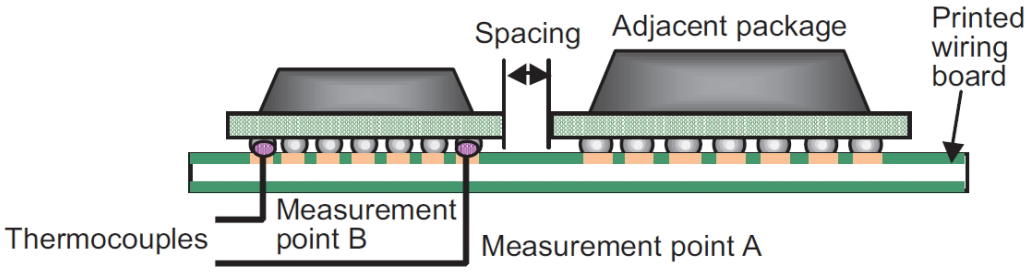
	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C -> 150 °C
B	Preheat ramp up rate	1.5–2.5 °C/s
C	Soak temperature range	150 °C -> 190 °C
D	Soak time	80–110 s
E	Liquidus temperature	217°C
F	Time above liquidus	60–90 s
G	Peak temperature	240–250 °C

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
H	Cool down temperature rate	⩽4°C/s

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe.

Figure 9-2 Measuring the Reflow Soldering Process



NOTE

To measure the temperature of the QFP-packaged chip, place the temperature probe directly at the pin.

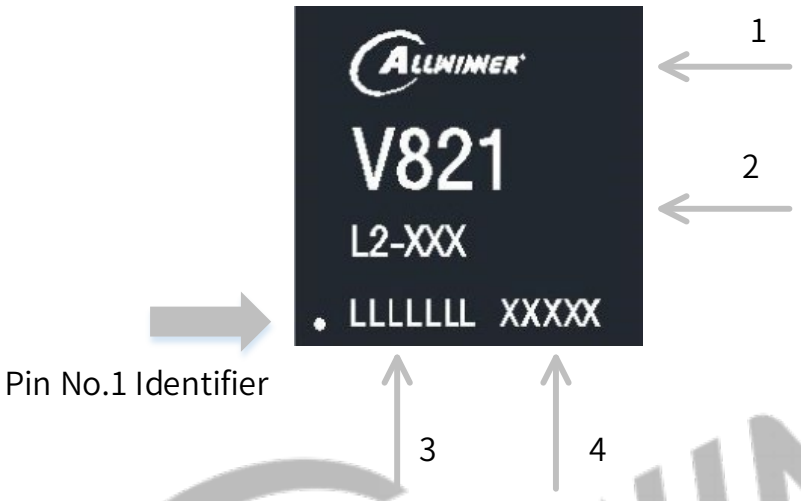
If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10 Part Marking

10.1 V821L2-XXX

The following figure shows the V821L2-XXX marking.

Figure 10-1 V821L2-XXX Marking



The following table describes the V821L2-XXX marking definitions.

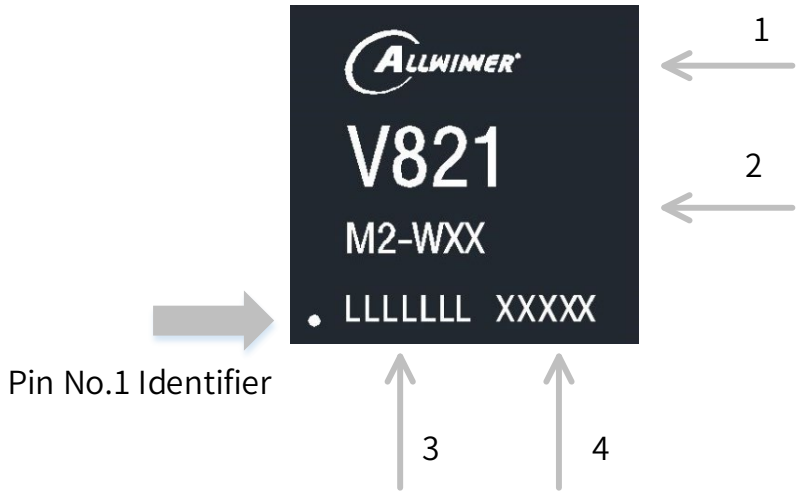
Table 10-1 V821L2-XXX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V821L2-XXX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.2 V821M2-WXX

The following figure shows the V821M2-WXX marking.

Figure 10-2 V821M2-WXX Marking



The following table describes the V821M2-WXX marking definitions.

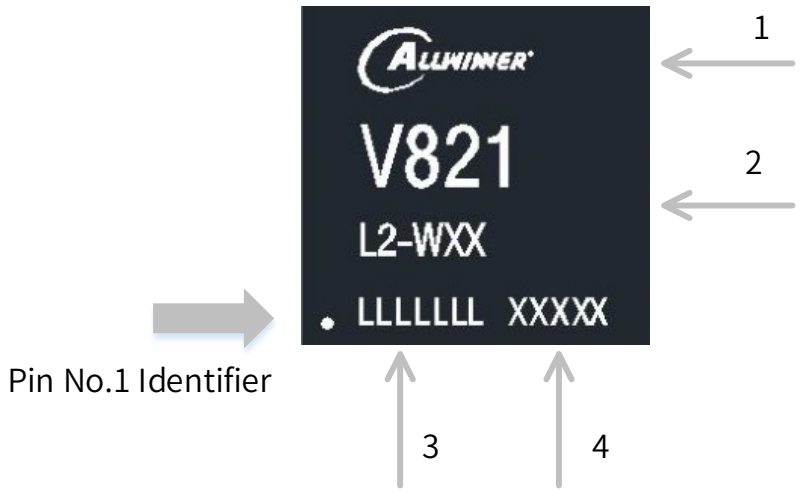
Table 10-2 V821M2-WXX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V821M2-WXX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.3 V821L2-WXX

The following figure shows the V821L2-WXX marking.

Figure 10-3 V821L2-WXX Marking



The following table describes the V821L2-WXX marking definitions.

Table 10-3 V821L2-WXX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V821L2-WXX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

Allwinner Technology Co., Ltd.
No.9 Technology Road 2, High-Tech Zone,
Zhuhai, Guangdong Province, China

Contact US:
Service@allwinnertech.com
www.allwinnertech.com