XTSD01G/XTSD02G/XTSD04/XTSD08G

DATASHEET

Rev V2.6

Mar 23, 2017

1. Introduction

XTX SD NAND is an embedded storage solution designed in a LGA8 package form. The operation of SD NAND is similar to an SD card which is an industry standard.

SD NAND consists of NAND flash and a high performance controller. 3.3V supply voltage is required for the NAND area (VCC). SD NAND is fully compliant with SD2.0 interface, which allows most of general CPU to utilize.
SD NAND has high performance at a competitive cost, high quality and low power consumption.

2. Product List

Part number	Capacity	Package	Size
XTSD01GLGEAG	1Gb	LGA8 (Land Grid Array)	8*6mm
XTSD02GLGEAG	2Gb	LGA8 (Land Grid Array)	8*6mm
XTSD04GLGEAG	4Gb	LGA8 (Land Grid Array)	8*6mm
XTSD08GLGEAG	8Gb	LGA8 (Land Grid Array)	8*6mm

3. Features

- Support up to 50Mhz clock frequency
- Support 1/4 bit mode
- Built-in HW ECC Engine and highly reliable NAND management mechanism
- Write speed up to class 8
- Smaller package LGA8 (Land Grid Array)

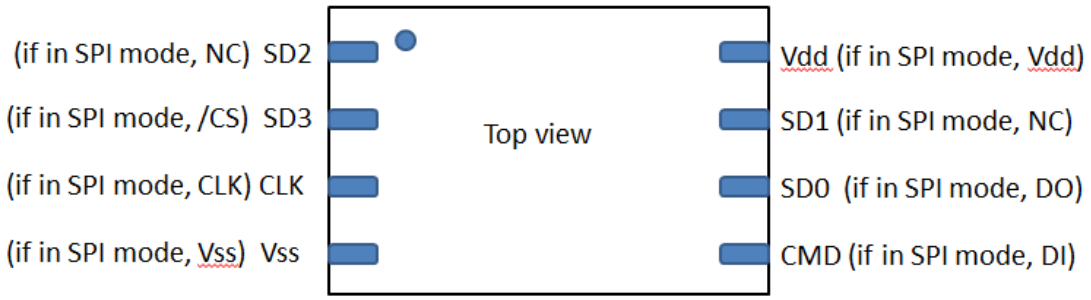
4. Physical Characteristics

4.1. Temperature

1) Operation Conditions
   Temperature Range: Ta = -30 to +85 degrees centigrade

2) Storage Conditions
   Temperature Range: Tstg = -40 to +85 degrees centigrade

5. Pin Assignments



Pin name (SD mode)

1	SD2, I/O pin
2	SD3, I/O pin
3	CLK, SD NAND clock signal
4	Vss, Ground
5	CMD, SD NAND command signal
6	SD0, I/O pin
7	SD1, I/O pin
8	Vdd, Power supply

Pin name (SPI mode)

1	NC, no connection
2	/CS, chip select
3	CLK, SD NAND clock signal
4	Vss, Ground
5	DI, data in
6	DO, data out
7	NC, no connecction
8	Vdd, Power supply

6. Usage

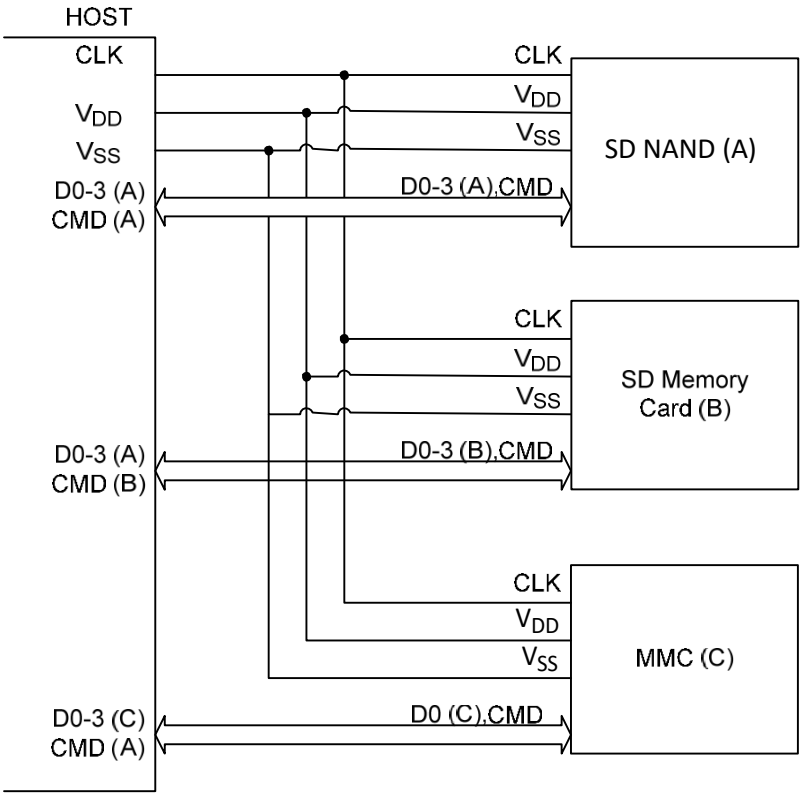
6.1 SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the SD card will use only DAT0. After initialization, host can change the bus width. Multiplied SD cards connections are available to the host. Common VDD, VSS and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each device from host.
This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:
Commands are transferred serially on the CMD line. A command is a token to start an operation from host to the device. Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:
Responses are transferred serially on the CMD line.
A response is a token to answer to a previous received command. Responses are sent from an addressed single card or from all connected cards.

Data:
Data can be transfer from the card to the host or vice versa. Data is transferred via the data lines .



CLK: Host card Clock signal

CMD: Bi-directional Command/ Response Signal

DAT0 - DAT3: 4 Bi-directional data signal

VDD: Power supply

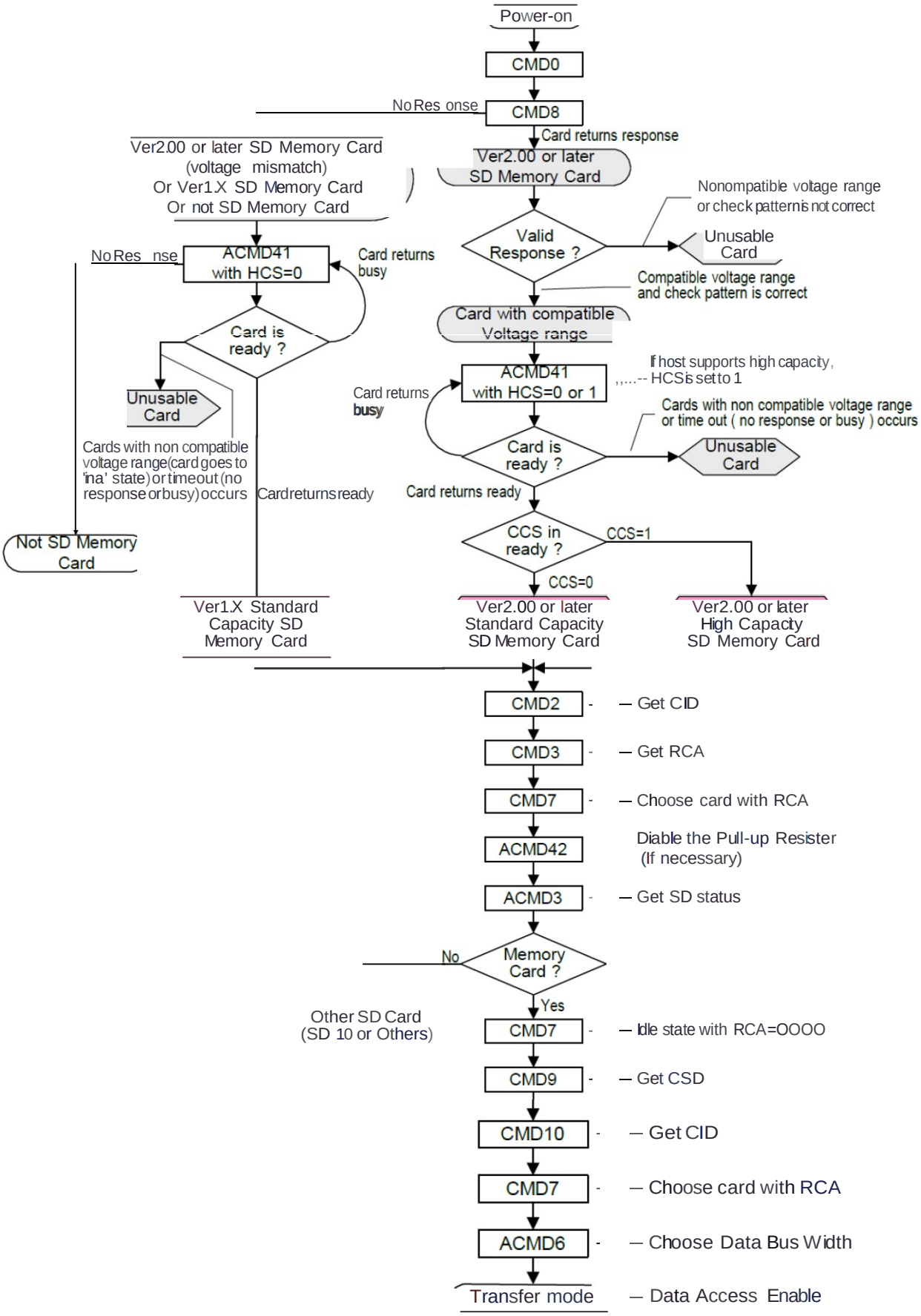
VSS: GND

6.2. Card Initialize

To initialize the SD NAND, follow the following procedure is recommended example.

1) Supply Voltage for initialization.
   Host System can apply the Operating Voltage from initialization to the card. Apply more than 74 cycles of Dummy-clock to the SD card.
2) Select operation mode (SD mode or SPI mode)
   In case of SPI mode operation, host should drive 1 pin (CD/DAT3) of SD Card I/F to "Low" level. Then, issue CMD0. In case of SD mode operation, host should drive or detect 1 pin of SD Card I/F (Pull up register of 1 pin is pull up to "High" normally). Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.
3) Send the ACMD41 with Arg = 0 and identify the operating voltage range of the Card.
4) Apply the indicated operating voltage to the card.
   Reissue ACMD41 with apply voltage storing and repeat ACMD41 until the busy bit is cleared. (Bit 31 Busy = 1) If response time out occurred, host can recognize not SD Card.
5) Issue the CMD2 and get the Card ID (CID).
   Issue the CMD3 and get the RCA. (RCA value is randomly changed by access, not equal zero)
6) Issue the CMD7 and move to the transfer state.
   If necessary, Host may issue the ACMD42 and disabled the pull up resistor for Card detect.
7) Issue the ACMD13 and poll the Card status as SD Memory Card.
   Check SD_CARD_TYPE value. If significant 8 bits are "all zero", that means SD Card. If it is not, stop initialization.
8) Issue CMD7 and move to standby state. Issue CMD9 and get CSD. Issue CMD10 and get CID.
9) Back to the Transfer state with CMD7.
   Issue ACMD6 and choose the appropriate bus-width.

Then the Host can access the Data between the SD card as a storage device.



SD card Initialize Procedure

6.3 DC Characteristics

Item		Symbo	MIN	MAX.	Unit	Note
Supply Voltage		V_{DD}	2.7	3.6	V	
Input Voltage	High Level	V_{IH}	$V_{DD} \times 0.625$	$V_{DD}+0.3$	V	
	Low Level	V_{IL}	$V_{SS}-0.3$	$V_{DD} \times 0.25$	V	
Output Voltage	High Level	V_{OH}	$V_{DD} \times 0.75$	—	V	I_{OH} = -2mA, $V_{DD}=V_{DD}$ min
	Low Level	V_{OL}	—	$V_{DD} \times 0.125$	V	I_{OL} = 2mA, $V_{DD}=V_{DD}$ min
Stanby Current		I_{CC1}	—	20*	mA	V_{DD} = 3.6V , Clock 25MHz
			—	0.2		V_{DD} = 3.0V, Clock STOP, Ta=25℃
Operation Current (*)	Write	I	—	30	mA	3.6V / 25MHz, 50MHz
	Read		—	30		
Input Voltage Setup Time		Vrs	—	250	ms	

Note: Standby current max 20mA with CLOCK 25Mhz only based on 100 pcs samples

Peak Voltage and Leak Current

Item	Symbol	Min.	Max.	Unit	Note
Peak voltage on all lines		-0.3	$V_{DD}+0.3$	V	
Input Leakage Current for all pins		-10	10	mA	
Output Leakage Current for all outputs		-10	10	mA	

Signal Capacitance

Item	Symbol	Min.	Max.	Unit	Note
Pull up Resistance	R_{CMD} R_{DAT}	10	100	k	
Total bus capacitance for each signal line	C_L	—	40	pF	1 card $C_{HOST}+C_{BUS} \leqq 30pF$
Card capacitance for signal pin	C_{CARD}	—	10	pF	
Pull up Resistance inside card (pin1)	R_{DAT3}	10	90	k	
Capacity Conneted to Power line	C_C	—	5	pF	

Note: WP pull-up (Rwp) Value is depend on the Host Interface drive circuit.

7. Internal Information

7.1.1. Registers

The SD NAND has six registers and SD Status information: OCR, CID, CSD, RCA, DSR, SCR and SD Status.
DSR IS NOT SUPPORTED in this card.
There are two types of register groups.
MMC compatible registers: OCR, CID, CSD, RCA, DSR, and SCR SD card Specific: SD Status SD card Registers

Resister Name	Bit Width	Description
OCR	32	Operation Conditions (VDU Voltage Profile and Busy Status Information)
CID	128	Card Identification information
CSD	128	Card specific information
RCA	16	Relative Card Address
DSR	16	Not Implemented (Programmable Card Driver): Driver Stage Register
SCR	64	SD Memory Card"s special features
SD Status	512	Status bits and Card features

7.1.2. OCR Register

This 32-bit register describes operating voltage range and status bit in the power supply. OCR register definition.

OCR bit position	VDD voltage window	Initial Value			
		1Gb	2Gb	4Gb	--
31	Card power up status bit(busy)	"0" = busy "1" = ready			
30	Card Capacity Status	"0"= SD Memory Card "1"= SDHC Memory Card			
29-25	reserved	All„0"			
24	Switching to 1.8V Accepted(S18A)	0			
23	3.6 - 3.5	1			
22	3.5 - 3.4	1			
21	3.4 - 3.3	1			
20	3.3 - 3.2	1			
19	3.2 - 3.1	1			
18	3.1 - 3.0	1			
17	3.0 - 2.9	1			
16	2.9 - 2.8	1			
15	2.8 - 2.7	1			
14	Reserved	0			
13	Reserved	0			
12	Reserved	0			
11	Reserved	0			
10	Reserved	0			
9	Reserved	0			
8	Reserved	0			
7	Reserved for Low Voltage Range	0			
6	Reserved	0			
5	Reserved	0			
4	Reserved	0			
3-0	reserved	All„0"			

bit 23-4: Describes the SD Card Voltage; bit 31 indicates the card power up status. Value "1" is set after power up and initialization procedure has been completed.

7.1.3. CID Register

The CID (Card Identification) register is 128-bit width. It contains the card identification information. (Refer Appendix 3. for the detail) The Value of CID Register is vender specific.

Table 11: CID Register

Field	Width	CID-slice	Initial Value			
			1Gb	2GB	4GB	–
MID	8	[127:120]	TBD			
OID	16	[119:104]	TBD			
PNM	40	[103:64]	TBD	TBD	TBD	–
PRV	8	[63:56]	TBD			
PSN	32	[55:24]	(a) (Product serial number)			
-	4	[23:20]	All "0b"			
MDT	12	[19:8]	(a) (Manufacture date)			
CRC	7	[7:1]	(b) (CRC)			
-	1	[0:0]	1b			

(a): Depends on the SD Card. Controlled by Production Lot.
(b) Depends on the CID Register

7.14. CSD Register

CSD is Card-Specific Data register provides information on 128bit width. Some field of this register can writable by PROGRAM_CSD (CMD27).

CSD Register

Field	Width	Cell Type	CSD Slice	Initial Value			
				1Gb	2Gb	4Gb	–
CSD_STRUCTURE	2	R	[127:126]	01b			
-	6	R	[125:120]	All "0b"			
TAAC	8	R	[119:112]	0_0001_110b (1ms)			
NSAC	8	R	[111:104]	00000000b			
TRAN_SPEED	8	R	[103:96]	0_0110_010b			
CCC	12	R	[95:84]	0101_1011_0101b			
READ_BL_LEN	4	R	[83:80]	1001b			
READ_BL_PARTIAL	1	R	[79:79]	0b			
WRITE_BLK_MISALIGN	1	R	[78:78]	0b			
READ_BLK_MISALIGN	1	R	[77:77]	0b			
DSR_IMP	1	R	[76:76]	0b			
-	6	R	[75:70]	All "0b"			
C_SIZE	22	R	[69:48]	TBD	TBD	TBD	–
-	1	R	[47:47]	0b			
ERASE_BLK_EN	1	R	[46:46]	1b			
SECTOR_SIZE	7	R	[45:39]	11_1111_1b			
WP_GRP_SIZE	7	R	[38:32]	000_0000b			
WP_GRP_ENABLE	1	R	[31:31]	0b			
-	2	R	[30:29]	00b			
R2W_FACTOR	3	R	[28:26]	010b			
WRITE_BL_LEN	4	R	[25:22]	1001b			
WRITE_BL_PARTIAL	1	R	[21:21]	0b			
-	2	R	[20:16]	All "0b"			
FILE_FORMAT_GRP	1	R	[15:15]	0b			
COPY	1	R/W(1)	[14:14]	0b			
PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	0b			
TMP_WRITE_PROTECT	1	R/W	[12:12]	0b			
FILE_FORMAT	2	R	[11:10]	00b			
-	2	R	[9:8]	All "0b"			
CRC	7	R/W	[7:1]	(CRC)			
-	1	-	[0:0]	1b			

Cell Type:R: Read Only, R/W: Writable and Readable, R/W(1): One-time Writable / Readable
Note: Erase of one data block is not allowed in this card. This information is indicated by "ERASE_BLK_EN". Host System should refer this value before one data block size erase.

7.15. RCA Register

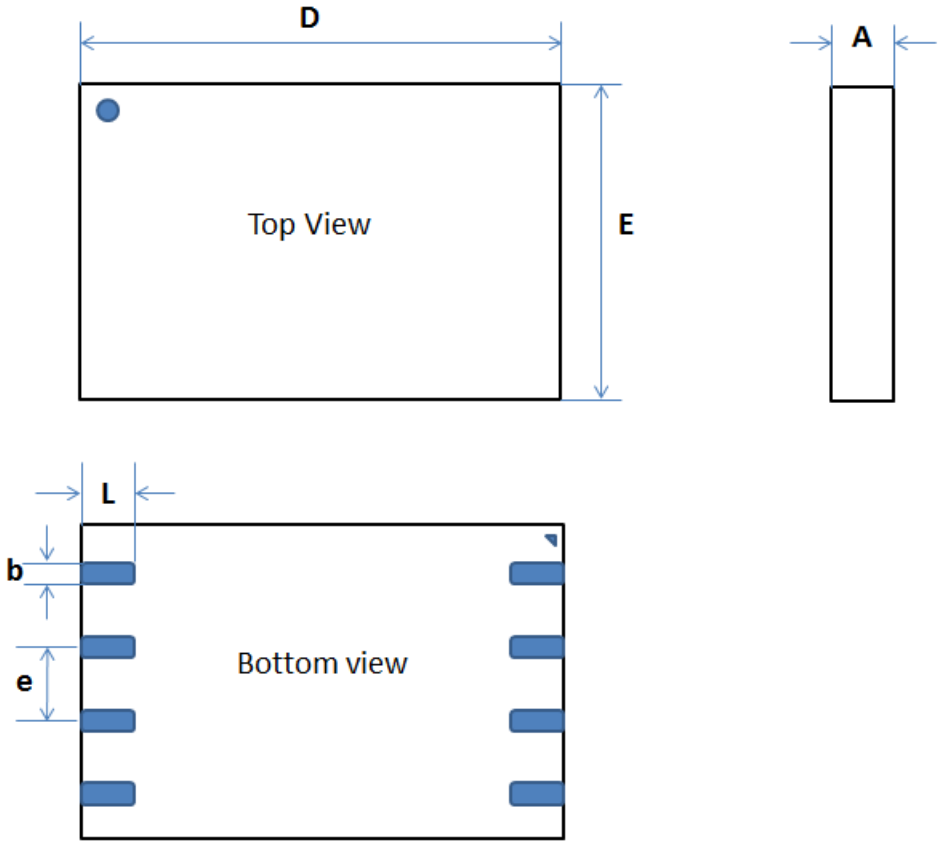
The writable 16bit relative card address register carries the card address in SD Card mode.

7.16 DSR Register

This register is not implemented on this card.

8. Package Dimensions

LGA8 (8*6mm) (Land Grid Array)

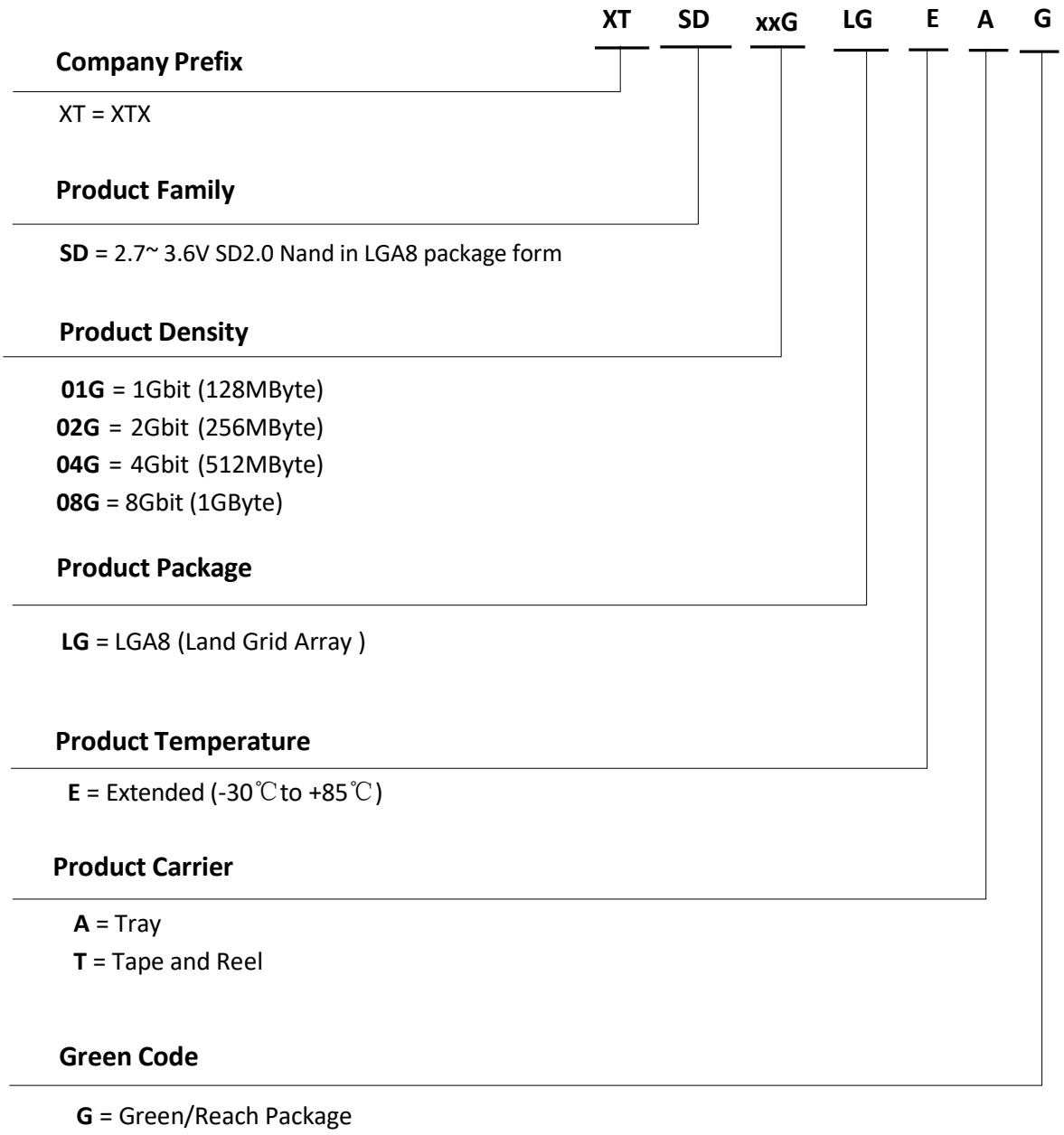


Dimensions

Symbol / Unit		A			b	D		E		e		L
mm	Min	0.85			0.55	7.95		5.95				0.75
	Nom	0.90			0.60	8.00		6.00		1.27		0.80
	Max	0.95			0.65	8.05		6.05				0.85

9. Ordering Informations

The ordering part number is formed by a valid combination of the following:



REVISION LIST

Version No.	Description	Date
V1.0	Initial release, part number is based on extended temperature, WSON 8*6mm package, tape & reel packing , 1Gb/2Gb/4Gb density were included .	2017/1/10
V1.1	Add 8Gb density , and correct some typos ;	2017/1/10
V2.1	Part number change from PNSDxxGWS to PNSDxxGLG; Package change from WSON8 to LGA8 ; Package dimension b change from 0.7mm to 0.6mm ; Package dimention picture updated without the dissipating pad ; Add a page for part number description ;	2017/1/22
V2.2	Modify part number descrition; Page head re-layout ;	2017/1/23
V2.3	Add SPI mode pin description	2017/2/1
V2.4	Set default Part number ans PNSDxxGLGEAG (tray packing)	2017/2/14
V2.5	Part number update from PNSDxxxx to XTSDxxxx	2017/3/3
V 2.6	Update ICC1 @ clock stop state to 0.2mA	2017/3/23