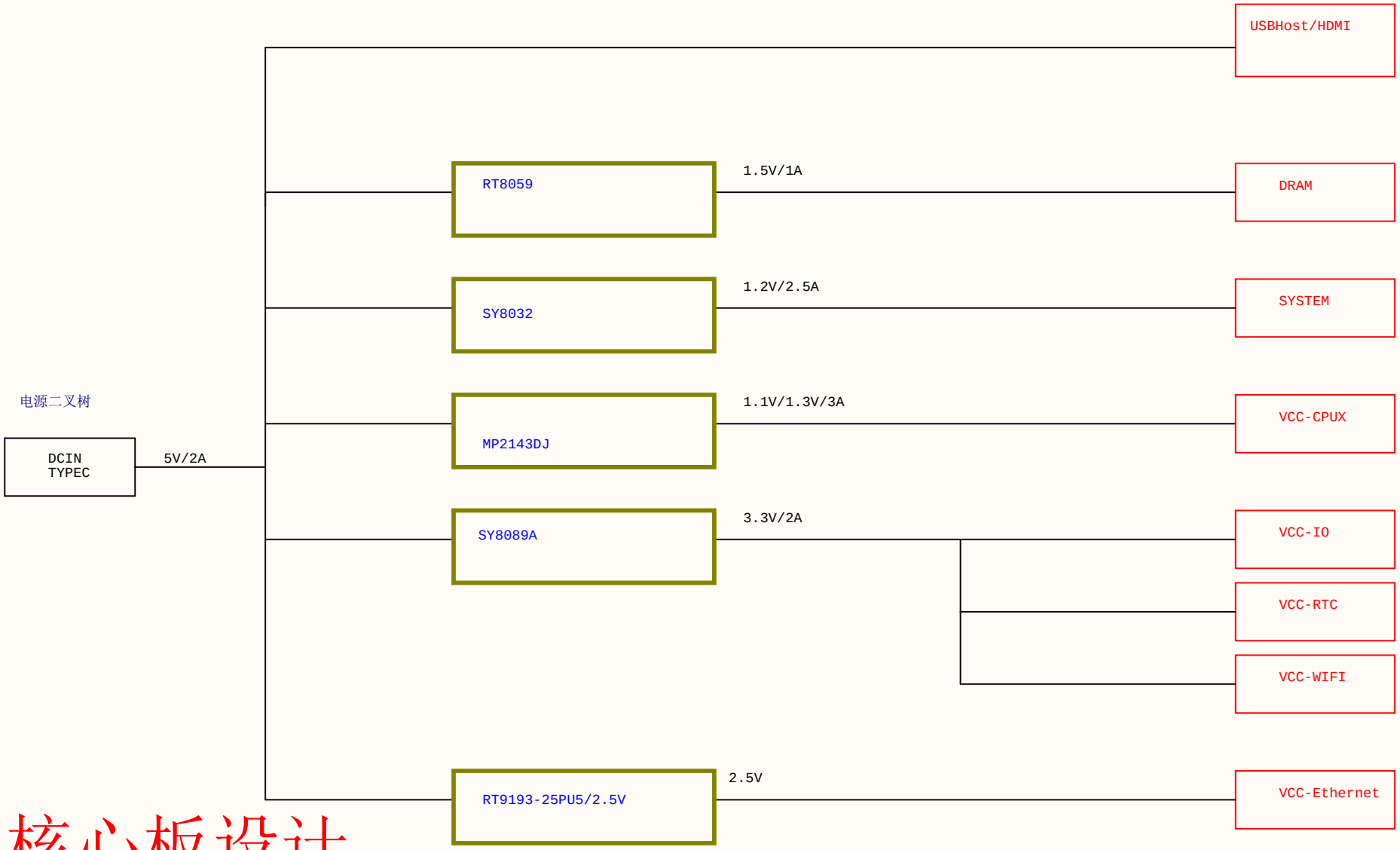
POWER TREE



核心板设计

CPU DRAM POWER GPIO

测试引出 TF CARD UART0 GND 5V

Title		
Size A4	Number	Revision
Date: 5/17/2020		Sheet of
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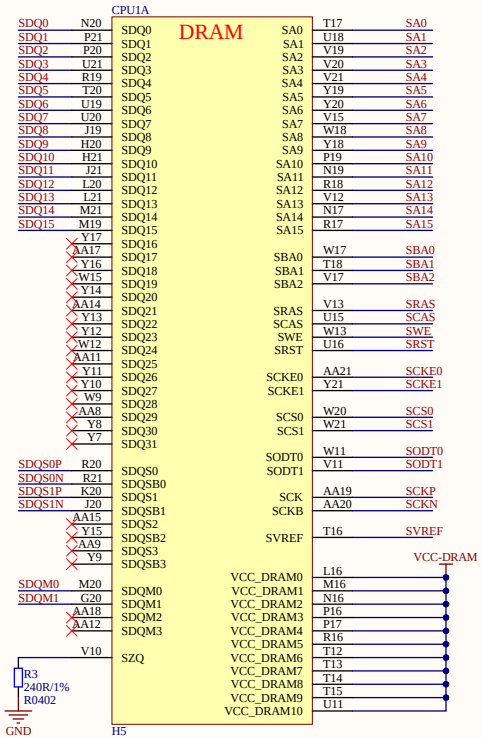
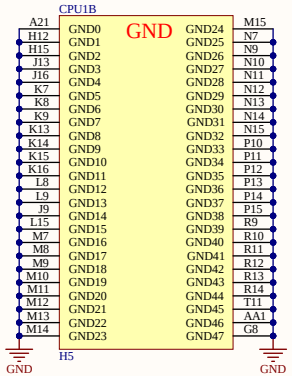
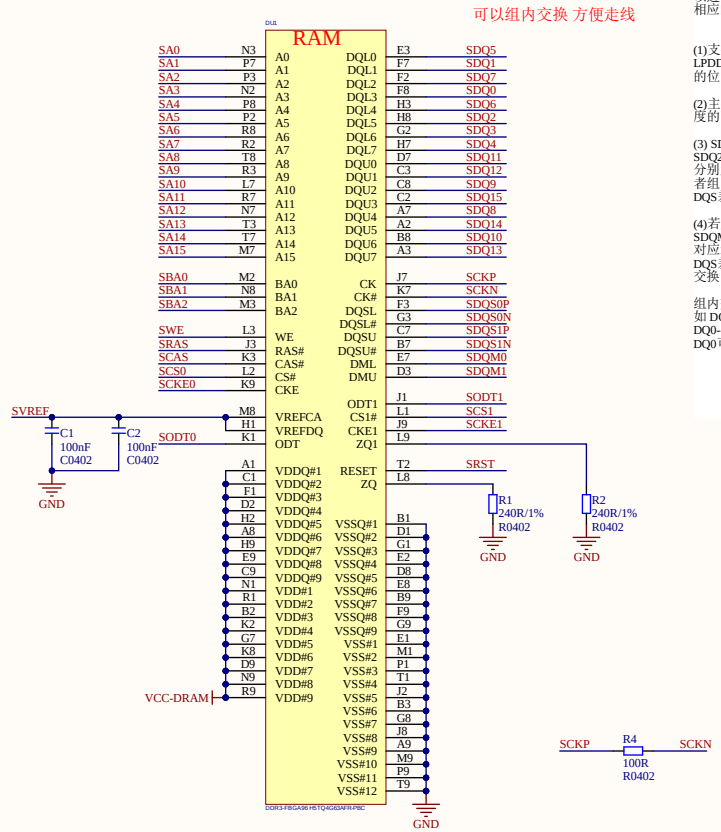




可以组内交换 方便走线



参考设计中有提到，如果使用DDR3，数据线可以进行组内或者组间交换，若进行组间交换，则相应的SDQM和SDMS差分对也必须进行相应交换

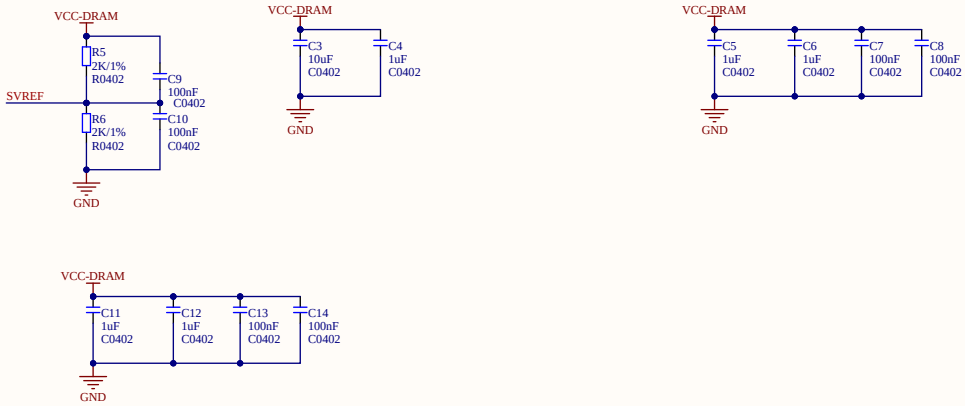
(1)支持DDR3, LPDDR2, LPDDR3,使用时需先确定DRAM的类型，以及单片的位宽，参考我司提供的DRAM参考layout.

(2)主控和DRAM端每--个ZQPIN都必须接240R-1%精度的下拉到地电阻。

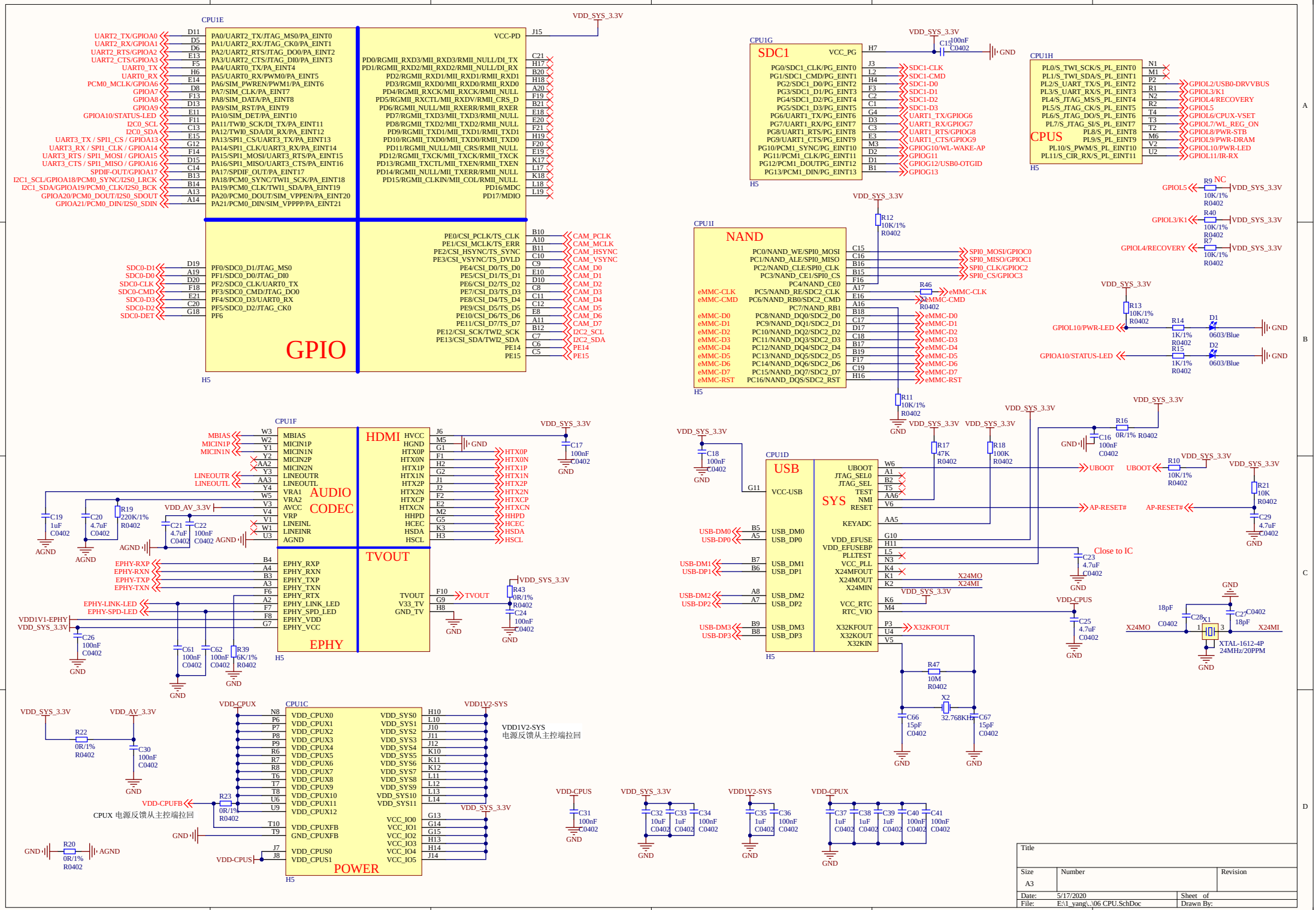
(3) SDQ0-SDQ7, SDQ8-SDQ15，SDQ16-SDQ23, SDQ24-SDQ31
分别为4组数据线，若用DDR3，则可以进行组内或者组间交换，若进行组间交换，则相应的SDQM和SDQS差分对也必须对应交换。

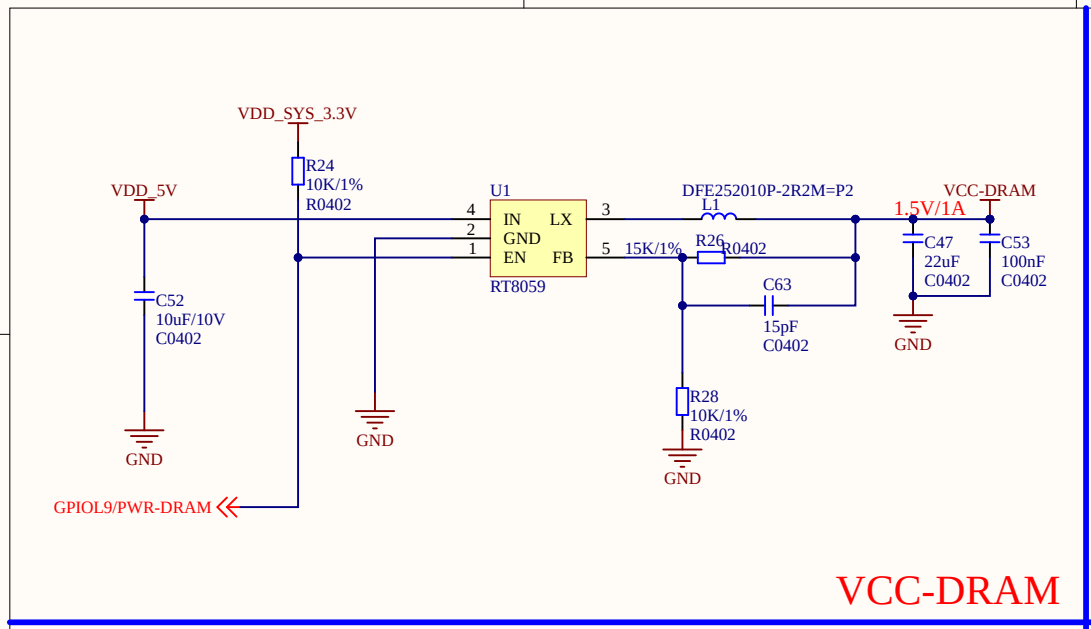
(4)若用LPDDR2或者LPDDR3，则SDQ0-SDQ7, SDQMO， SDQ0， SDQSOB 必须与主控.--对应连接，而其他高位的3组DQ以及高位的DQM和DQS差分对，则与DDR3类似，可以进行组内组间交换。

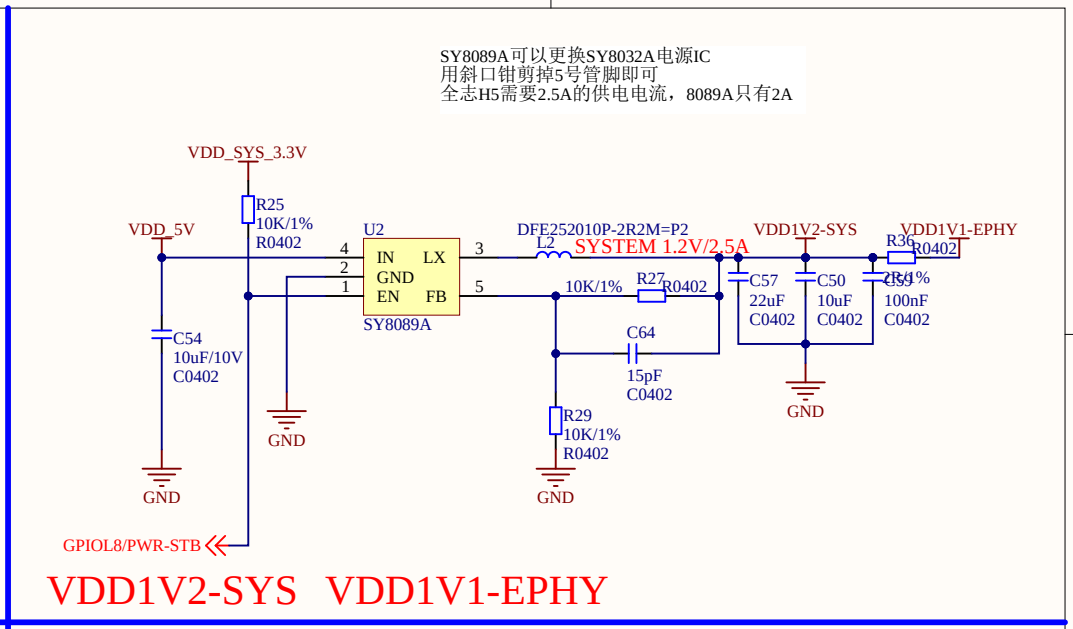
组内交换
如 DQ0-----DQ7是一组，一般情况下是CPU DQ0---------DDR DQ0这样一一对应，现在交换CPU DQ0可以对应DDR中的DQ1--------7中的任何一个。

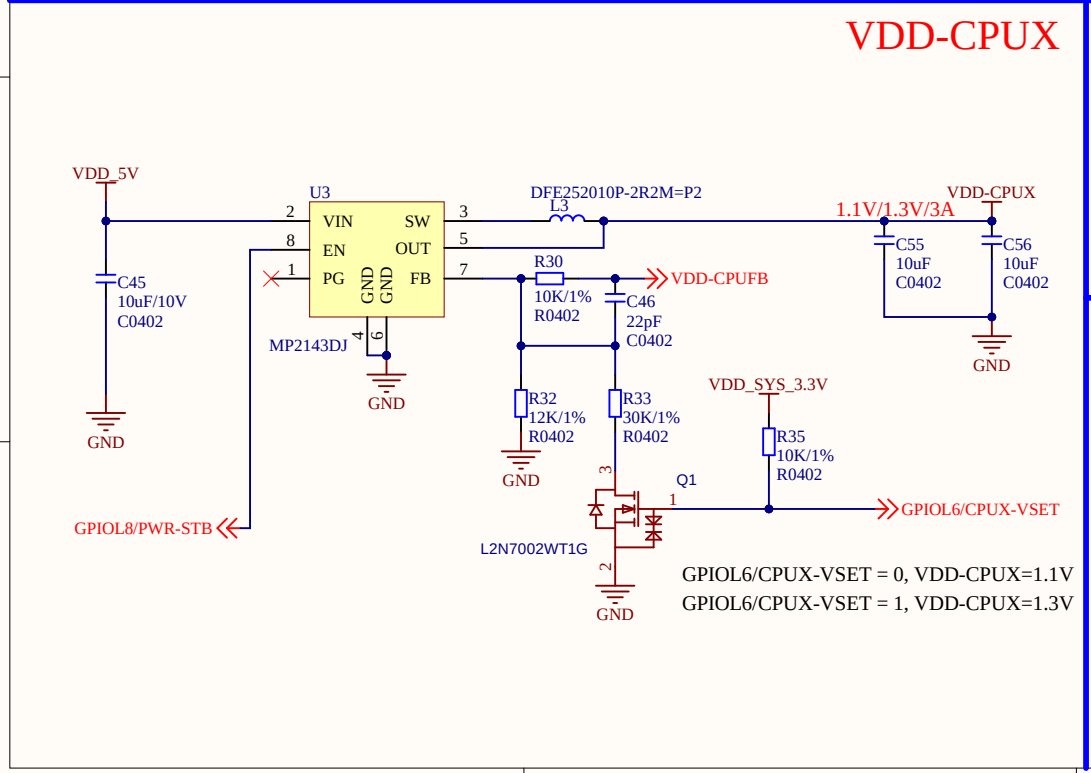


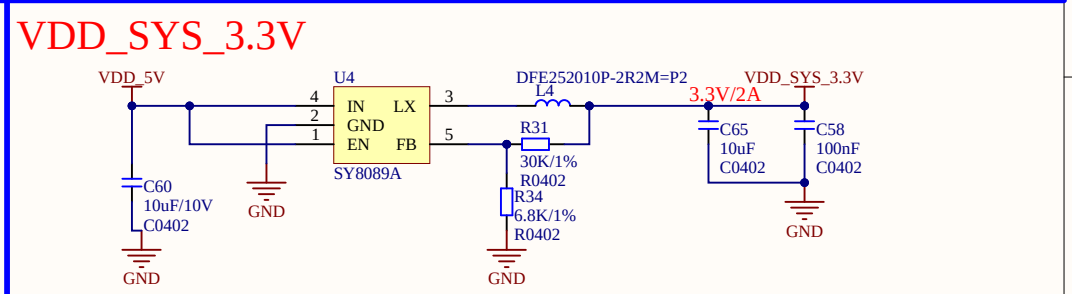
Title		
Size A4	Number	Revision
Date: 5/17/2020		Sheet of
File: E:\1_yang\..\05 DDR3 16X1.SchDoc		Drawn By:

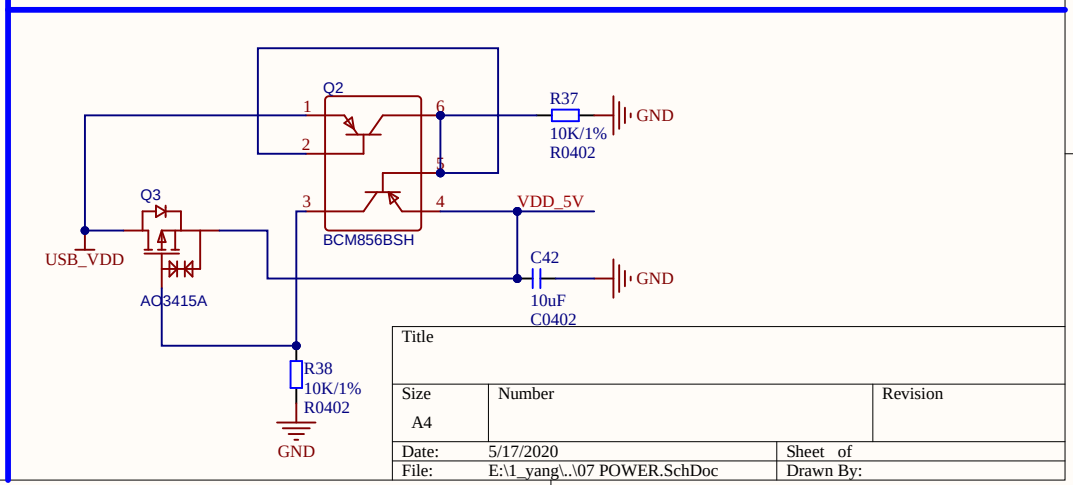

CPU1E
GPIO
H5
PA0/UART2_TX/JTAG_MS0/PA_EINT0
PA1/UART2_RX/JTAG_CK0/PA_EINT1
PA2/UART2_RTS/JTAG_DO0/PA_EINT2
PA3/UART2_CTS/JTAG_DI0/PA_EINT3
PA4/UART0_TX/PA_EINT4
PA5/UART0_RX/PWM0/PA_EINT5
PA6/SIM_PWREN/PWM1/PA_EINT6
PA7/SIM_CLK/PA_EINT7
PA8/SIM_DATA/PA_EINT8
PA9/SIM_RST/PA_EINT9
PA10/SIM_DET/PA_EINT10
PA11/TWI0_SCK/DI_TX/PA_EINT11
PA12/TWI0_SDA/DI_RX/PA_EINT12
PA13/SPI1_CS/UART3_TX/PA_EINT13
PA14/SPI1_CLK/UART3_RX/PA_EINT14
PA15/SPI1_MOSI/UART3_RTS/PA_EINT15
PA16/SPI1_MISO/UART3_CTS/PA_EINT16
PA17/SPDIF_OUT/PA_EINT17
PA18/PCM0_SYNC/TWI1_SCK/PA_EINT18
PA19/PCM0_CLK/TWI1_SDA/PA_EINT19
PA20/PCM0_DOUT/SIM_VPPEN/PA_EINT20
PA21/PCM0_DIN/SIM_VPPPP/PA_EINT21
VCC-PD
PD0/RGMII_RXD3/MII_RXD3/RMII_NULL/DI_TX
PD1/RGMII_RXD2/MII_RXD2/RMII_NULL/DI_RX
PD2/RGMII_RXD1/MII_RXD1/RMII_RXD1
PD3/RGMII_RXD0/MII_RXD0/RMII_RXD0
PD4/RGMII_RXCK/MII_RXCK/RMII_NULL
PD5/RGMII_RXCTL/MII_RXDV/RMII_CRS_D
PD6/RGMII_NULL/MII_RXERR/RMII_RXER
PD7/RGMII_TXD3/MII_TXD3/RMII_NULL
PD8/RGMII_TXD2/MII_TXD2/RMII_NULL
PD9/RGMII_TXD1/MII_TXD1/RMII_TXD1
PD10/RGMII_TXD0/MII_TXD0/RMII_TXD0
PD11/RGMII_NULL/MII_CRS/RMII_NULL
PD12/RGMII_TXCK/MII_TXCK/RMII_TXCK
PD13/RGMII_TXCTL/MII_TXEN/RMII_TXEN
PD14/RGMII_NULL/MII_TXERR/RMII_NULL
PD15/RGMII_CLKIN/MII_COL/RMII_NULL
PD16/MDC
PD17/MDIO
PF0/SDC0_D1/JTAG_MS0
PF1/SDC0_D0/JTAG_DI0
PF2/SDC0_CLK/UART0_TX
PF3/SDC0_CMD/JTAG_DO0
PF4/SDC0_D3/UART0_RX
PF5/SDC0_D2/JTAG_CK0
PF6
PE0/CSI_PCLK/TS_CLK
PE1/CSI_MCLK/TS_ERR
PE2/CSI_HSYNC/TS_SYNC
PE3/CSI_VSYNC/TS_DVLD
PE4/CSI_D0/TS_D0
PE5/CSI_D1/TS_D1
PE6/CSI_D2/TS_D2
PE7/CSI_D3/TS_D3
PE8/CSI_D4/TS_D4
PE9/CSI_D5/TS_D5
PE10/CSI_D6/TS_D6
PE11/CSI_D7/TS_D7
PE12/CSI_SCK/TWI2_SCK
PE13/CSI_SDA/TWI2_SDA
PE14
PE15
UART2_TX/GPIOA0
UART2_RX/GPIOA1
UART2_RTS/GPIOA2
UART2_CTS/GPIOA3
UART0_TX
UART0_RX
PCM0_MCLK/GPIOA6
GPIOA7
GPIOA8
GPIOA9
GPIOA10/STATUS-LED
I2C0_SCL
I2C0_SDA
UART3_TX / SPI1_CS / GPIOA13
UART3_RX / SPI1_CLK / GPIOA14
UART3_RTS / SPI1_MOSI / GPIOA15
UART3_CTS / SPI1_MISO / GPIOA16
SPDIF-OUT/GPIOA17
I2C1_SCL/GPIOA18/PCM0_SYNC/I2S0_LRCK
I2C1_SDA/GPIOA19/PCM0_CLK/I2S0_BCK
GPIOA20/PCM0_DOUT/I2S0_SDOUT
GPIOA21/PCM0_DIN/I2S0_SDIN
SDC0-D1
SDC0-D0
SDC0-CLK
SDC0-CMD
SDC0-D3
SDC0-D2
SDC0-DET
CAM_PCLK
CAM_MCLK
CAM_HSYNC
CAM_VSYNC
CAM_D0
CAM_D1
CAM_D2
CAM_D3
CAM_D4
CAM_D5
CAM_D6
CAM_D7
I2C2_SCL
I2C2_SDA
PE14
PE15
VDD_SYS_3.3V
CPU1G
SDC1
VCC_PG
PG0/SDC1_CLK/PG_EINT0
PG1/SDC1_CMD/PG_EINT1
PG2/SDC1_D0/PG_EINT2
PG3/SDC1_D1/PG_EINT3
PG4/SDC1_D2/PG_EINT4
PG5/SDC1_D3/PG_EINT5
PG6/UART1_TX/PG_EINT6
PG7/UART1_RX/PG_EINT7
PG8/UART1_RTS/PG_EINT8
PG9/UART1_CTS/PG_EINT9
PG10/PCM1_SYNC/PG_EINT10
PG11/PCM1_CLK/PG_EINT11
PG12/PCM1_DOUTPG_EINT12
PG13/PCM1_DIN/PG_EINT13
SDC1-CLK
SDC1-CMD
SDC1-D0
SDC1-D1
SDC1-D2
SDC1-D3
UART1_TX/GPIOG6
UART1_RX/GPIOG7
UART1_RTS/GPIOG8
UART1_CTS/GPIOG9
GPIOG10/WL-WAKE-AP
GPIOG11
GPIOG12/USB0-OTGID
GPIOG13
C15 100nF C0402
GND
CPU1H
CPUS
PL0/S_TWI_SCK/S_PL_EINT0
PL1/S_TWI_SDA/S_PL_EINT1
PL2/S_UART_TX/S_PL_EINT2
PL3/S_UART_RX/S_PL_EINT3
PL4/S_JTAG_MS/S_PL_EINT4
PL5/S_JTAG_CK/S_PL_EINT5
PL6/S_JTAG_DO/S_PL_EINT6
PL7/S_JTAG_SI/S_PL_EINT7
PL8/S_PL_EINT8
PL9/S_PL_EINT9
PL10/S_PWM/S_PL_EINT10
PL11/S_CIR_RX/S_PL_EINT11
GPIOL2/USB0-DRVVBUS
GPIOL3/K1
GPIOL4/RECOVERY
GPIOL5
GPIOL6/CPUX-VSET
GPIOL7/WL_REG_ON
GPIOL8/PWR-STB
GPIOL9/PWR-DRAM
GPIOL10/PWR-LED
GPIOL11/IR-RX
R9 NC 10K/1% R0402
R40 10K/1% R0402
R7 10K/1% R0402
CPU1I
NAND
PC0/NAND_WE/SPI0_MOSI
PC1/NAND_ALE/SPI0_MISO
PC2/NAND_CLE/SPI0_CLK
PC3/NAND_CE1/SPI0_CS
PC4/NAND_CE0
PC5/NAND_RE/SDC2_CLK
PC6/NAND_RB0/SDC2_CMD
PC7/NAND_RB1
PC8/NAND_DQ0/SDC2_D0
PC9/NAND_DQ1/SDC2_D1
PC10/NAND_DQ2/SDC2_D2
PC11/NAND_DQ3/SDC2_D3
PC12/NAND_DQ4/SDC2_D4
PC13/NAND_DQ5/SDC2_D5
PC14/NAND_DQ6/SDC2_D6
PC15/NAND_DQ7/SDC2_D7
PC16/NAND_DQS/SDC2_RST
SPI0_MOSI/GPIOC0
SPI0_MISO/GPIOC1
SPI0_CLK/GPIOC2
SPI0_CS/GPIOC3
eMMC-CLK
eMMC-CMD
eMMC-D0
eMMC-D1
eMMC-D2
eMMC-D3
eMMC-D4
eMMC-D5
eMMC-D6
eMMC-D7
eMMC-RST
R12 10K/1% R0402
R46 eMMC-CLK
eMMC-CMD R0402
R11 10K/1% R0402
R13 10K/1% R0402
R14 1K/1% R0402
R15 1K/1% R0402
D1 0603/Blue
D2 0603/Blue
GPIOL10/PWR-LED
GPIOA10/STATUS-LED
CPU1F
AUDIO CODEC
MBIAS
MICIN1P
MICIN1N
MICIN2P
MICIN2N
LINEOUTR
LINEOUTL
VRA1
VRA2
AVCC
VRP
LINEINL
LINEINR
AGND
HDMI
HVCC
HGND
HTX0P
HTX0N
HTX1P
HTX1N
HTX2P
HTX2N
HTXCP
HTXCN
HHPD
HCEC
HSDA
HSCL
TVOUT
V33_TV
GND_TV
EPHY
EPHY_RXP
EPHY_RXN
EPHY_TXP
EPHY_TXN
EPHY_RTX
EPHY_LINK_LED
EPHY_SPD_LED
EPHY_VDD
EPHY_VCC
VDD_AV_3.3V
C17 100nF C0402
C19 1uF C0402
C20 4.7uF C0402
R19 220K/1% R0402
C21 4.7uF C0402
C22 100nF C0402
R43 0R/1% R0402
C24 100nF C0402
C26 100nF C0402
C61 100nF C0402
C62 100nF C0402
R39 6K/1% R0402
VDD1V1-EPHY
CPU1D
USB
SYS
UBOOT
JTAG_SEL0
JTAG_SEL
TEST
NMI
RESET
KEYADC
VDD_EFUSE
VDD_EFUSEBP
PLLTEST
VCC_PLL
X24MFOUT
X24MOUT
X24MIN
VCC_RTC
RTC_VIO
X32KFOUT
X32KOUT
X32KIN
VCC-USB
USB_DM0
USB_DP0
USB_DM1
USB_DP1
USB_DM2
USB_DP2
USB_DM3
USB_DP3
R17 47K R0402
R18 100K R0402
R16 0R/1% R0402
C16 100nF C0402
R10 10K/1% R0402
R21 10K R0402
C29 4.7uF C0402
C23 4.7uF C0402
Close to IC
C25 4.7uF C0402
VDD-CPUS
X24MO
X24MI
X32KFOUT
R47 10M R0402
X2 32.768KHz
C66 15pF C0402
C67 15pF C0402
C27 18pF C0402
C28 18pF C0402
X1 XTAL-1612-4P 24MHz/20PPM
CPU1C
POWER
VDD_CPUX0
VDD_CPUX1
VDD_CPUX2
VDD_CPUX3
VDD_CPUX4
VDD_CPUX5
VDD_CPUX6
VDD_CPUX7
VDD_CPUX8
VDD_CPUX9
VDD_CPUX10
VDD_CPUX11
VDD_CPUX12
VDD_CPUXFB
GND_CPUXFB
VDD_CPUS0
VDD_CPUS1
VDD_SYS0
VDD_SYS1
VDD_SYS2
VDD_SYS3
VDD_SYS4
VDD_SYS5
VDD_SYS6
VDD_SYS7
VDD_SYS8
VDD_SYS9
VDD_SYS10
VDD_SYS11
VCC_IO0
VCC_IO1
VCC_IO2
VCC_IO3
VCC_IO4
VCC_IO5
VDD1V2-SYS
VDD1V2-SYS 电源反馈从主控端拉回
VDD-CPUX
VDD-CPUFB
CPUX 电源反馈从主控端拉回
R22 0R/1% R0402
C30 100nF C0402
R23 0R/1% R0402
R20 0R/1% R0402
C31 100nF C0402
C32 10uF C0402
C33 1uF C0402
C34 100nF C0402
C35 1uF C0402
C36 100nF C0402
C37 1uF C0402
C38 1uF C0402
C39 1uF C0402
C40 100nF C0402
C41 100nF C0402
Title
Size A3
Number
Revision
Date: 5/17/2020
File: E:\1_yang\..\06 CPU.SchDoc
Sheet of
Drawn By:





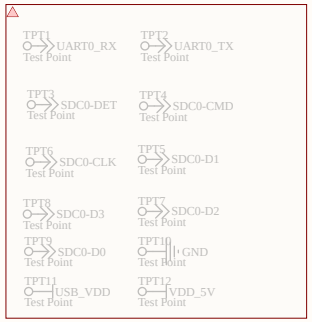






Title		
Size A4	Number	Revision
Date: 5/17/2020	Sheet of	
File: E:\1_yang\..\07 POWER.SchDoc	Drawn By:	

下(1-29)



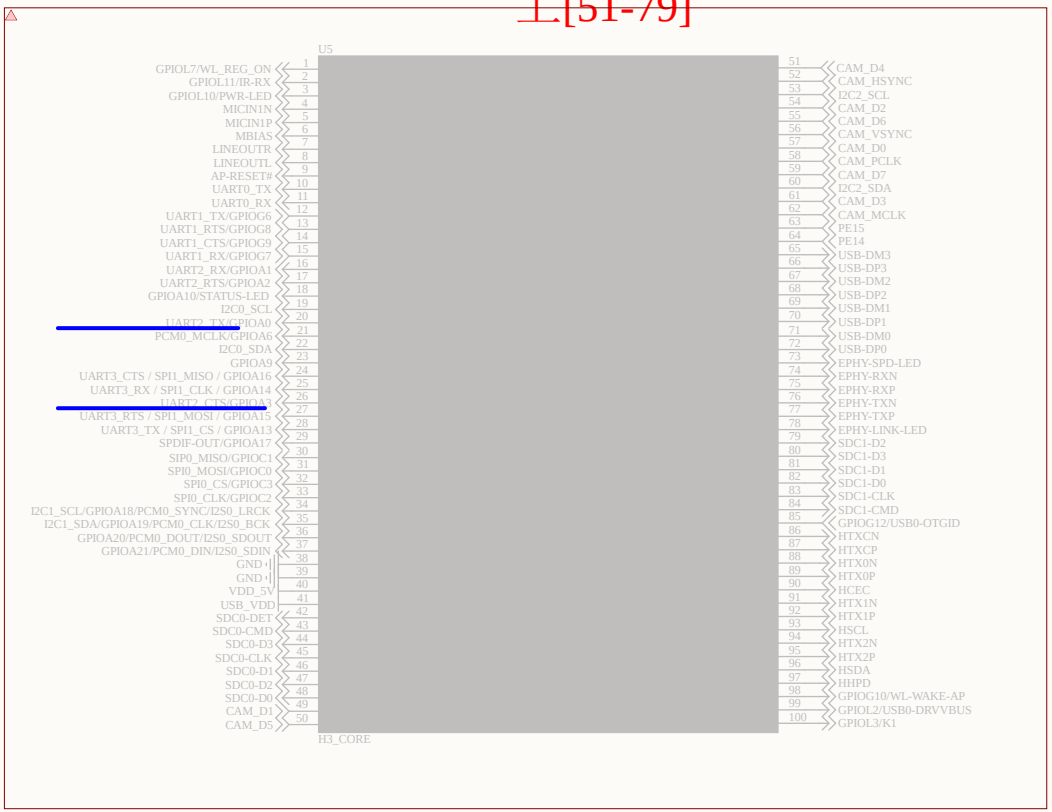
TPT13 VCC-DRAM Test Point

TPT14 VDD_SYS_3.3V Test Point

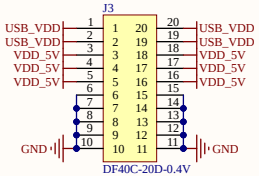
TPT15 VDD1V2-SYS Test Point

TPT16 VDD1V1-EPHY Test Point

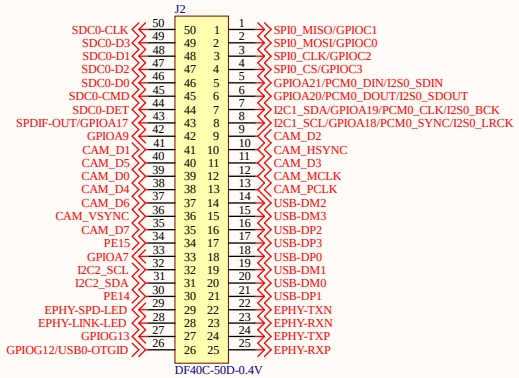
上[51-79]

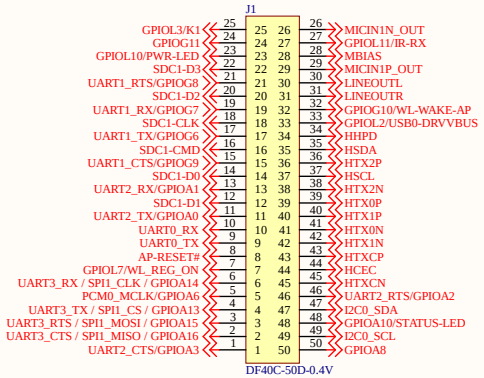


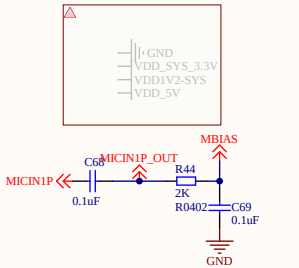
右[30-50]

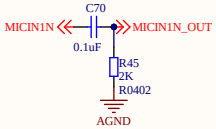


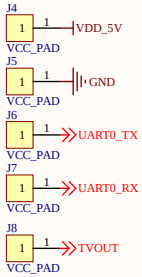
上[51-79]

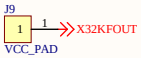




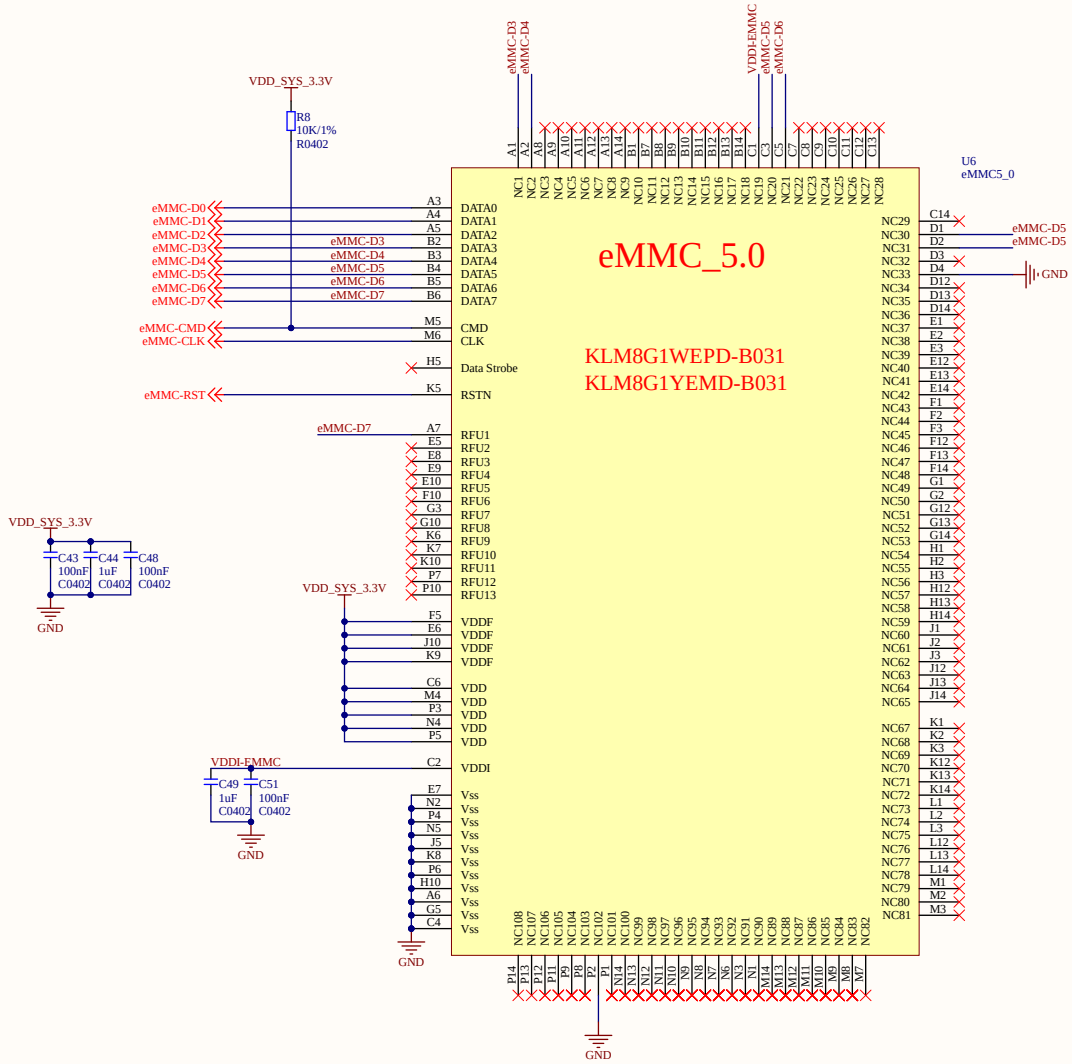








Title		
Size A1	Number	Revision
Date: 5/17/2020	Sheet of	
File: E:\1_yang\...\08 Core.SchDoc	Drawn By:	



Title		
Size A4	Number	Revision
Date: 5/17/2020	Sheet of	
File: E:\1_yang\..\09 eMMC.SchDoc	Drawn By:	