JZ4760B

Mobile Application Processor

Data Sheet

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1 Overview

JZ4760B is a mobile application processor targeting for multimedia rich and mobile devices like smartphone, tablet computer, mobile digital TV, and GPS. This SOC introduces innovative dual-core architecture to fulfill both high performance mobile computing and high quality video decoding requirements addressed by mobile multimedia devices.

The CPU (Central Processing Unit) core, equipped with 16K instruction cache and 16K data cache operating at 528~600MHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst processor engine. XBurst is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included.

The VPU (Video Processing Unit) core is powered with another XBurst processor engine. The SIMD instruction set implemented by XBurst engine, in together with the on chip video accelerating engine and post processing unit, delivers doubled video performance comparing with the single core implementation.

The memory interface supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory or 4-bit/8-bit/12-bit/16-bit/24-bit ECC MLC/TLC NAND flash memory for cost sensitive applications.

On-chip modules such as audio CODEC, multi-channel SAR-ADC, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. TV encoder unit 10-bits DAC provide composite TV signal output in PAL or NTSC format. The LCD controller support up to 1280x720 output, as well as external HDMI transmitter. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. The TS (Transport stream) interface provides enough bandwidth to connect to an external mobile digital TV demodulator. Other peripherals such as USB OTG and USB 1.1 host, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

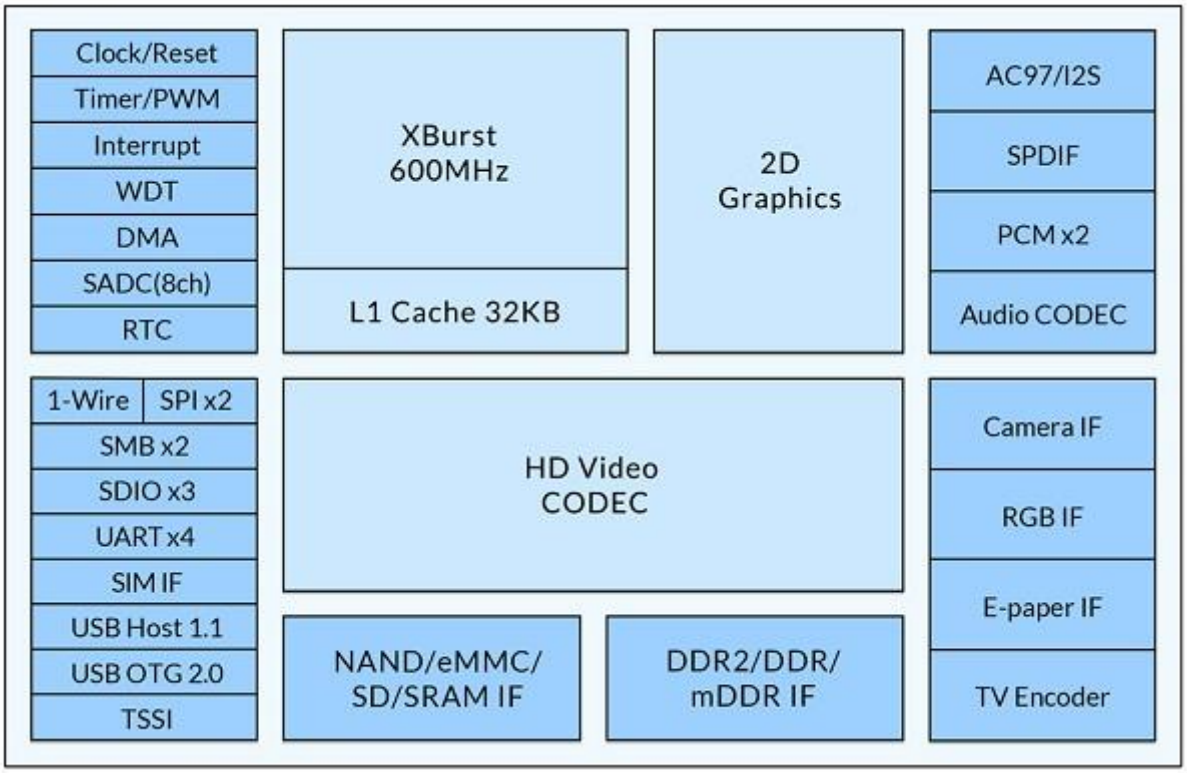


Figure 1-1 JZ4760B Diagram

1.2 Features

1.2.1 CPU

- XBurst CPU
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 8-stage pipeline micro-architecture up to 600MHz
- MMU
  - 32-entry joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- L1 Cache
  - 16K instruction cache
  - 16K data cache
- Hardware debug support

- 16kB tight coupled memory

1.2.2 VPU

- XBurst CPU for video processing
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® 8-stage pipeline micro-architecture up to 600MHz
- Video acceleration engine
  - Motion compensation
  - Motion estimation
  - De-block
  - DCT/IDCT for 4x4 block
  - Parser
- 48kB tight coupled memory
- 32kB scratch RAM

1.2.3 GPU

- 2D graphic
  - Up to 100M pix/s
  - Up to 1080P
  - Line/Rectangle
  - ROP4/Alpha blending/Filter
  - Rotation (90/180/270 degree)/Mirror
  - 1 Rectangle Clip

1.2.4 Display/Camera/Audio

- LCD controller
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode
  - 2, 4, 16 grayscales and up to 4096 colors in STN mode
  - 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
  - 24-bit data bus
  - Support 1,2,4,8 pins STN panel, 16bit, 18bit and 24bit TFT and 8bit I/F TFT
  - Display size up to 1280×720 pixels
  - 256×16 bits internal palette RAM
  - Support ITU601/656 data format
  - Support smart LCD (SRAM-like interface LCD module)
  - Support delta RGB
  - One single color background and two foreground OSD
  - Compressed frame supported
- TV encoder
  - Support NTSC or PAL

  - Support CVBS signal
  - 10 bits DAC
- EPD controller
  - Supports Electro-Phoretic Display and compatible devices
  - Supports different size of display panel
  - Supports different width of pixel data
  - Supports internal DMA operation and register operation
- Image post processor
  - Video frame resize
  - Color space conversion: 420/444/422 YUV to RGB convert
  - Bi-cubic algorithm supported
  - Video enhancement
- Alpha_osd
  - Support ARGB8888, RGB565, RGB555
  - Each layer has an alpha value for all pixels
  - Up to 800*480
  - Software can change overlay orders
  - The level of overlay can be set by software
  - Software must make sure the address of source and destination are 64-word aligned
  - Support 64-burst in AHB bus
  - In RGB656 & RGB555mode, software must make sure each line aligned in word
- Camera interface module
  - Input image size up to 4096×4096 pixels
  - Supports CCIR656 data format
  - YCbCr 4:2:2 and YCbCr 4:4:4 data format
  - Raw data input
  - 64×32 image data receive FIFO with DMA support
- AC97/I2S/SPDIF controller
  - Supports 8, 16, 18, 20 and 24 bit for sample for AC-link and I2S/MSB-Justified format
  - Support 2/4/6/8 channels data out for I2S
  - Support compress data format for SPDIF
  - DMA transfer mode support
  - Support variable sample rate mode for AC-link format
  - Power down mode and two wake-up mode support for AC-link format
  - Programmable Interrupt function support
  - Support the on-chip CODEC
  - Support off-chip CODEC
  - Support off-chip HDMI transmitter audio
- Two PCM interfaces
  - Data starts with the frame PCMSYN or one PCMCLK later
  - Support three modes of operation for PCM: Short frame sync mode, Long frame sync mode, Multi-slot mode
  - Data is transferred and received with the MSB first

- Support master mode and slave mode
- The PCM serial output data, PCMDOUT, is clocked out using the rising edge of the PCMSCLK
- The PCM serial input data, PCMDIN, is clocked in on the falling edge of the PCMSCLK.
- 8/16 bit sample data sizes supported
- DMA transfer mode supported
- Two FIFOs for transmit and receive respectively with 16 samples capacity in every direction

- On-chip audio CODEC
  - 24-bit DAC, SNR: 95dB
  - 24-bit ADC, SNR: 90dB
  - Sample rate: 8/9.6/11.025/12/16/22.05/24/32/44.1/48/96kHz
  - L/R channels line input
  - 2 MICs input, differential or single-ended
  - L/R channels headphone output amplifier support up to 16ohm load
  - Capacitor-coupled
  - Mono differential line out
  - Mono 450mW amplifier for speaker out for 8ohm load

1.2.5 Memory Interface

- DDR Controller
  - Support DDR2, DDR, mobile DDR (LPDDR) memory
  - Support x16 and x32 external DDR data width
  - Support clock frequency ratio – (BUS clock) : (DDR clock) = 2:1
  - Support clock frequency ratio – (BUS clock) : (DDR clock) = 1:1
  - Support clock-stop mode
  - Support auto-refresh and self-refresh
  - Support power-down mode and deep-power-down mode
  - Programmable DDR timing parameters
  - Programmable DDR row and column address width
- Static memory interface
  - Direct interface to SRAM, ROM, Burst ROM, and NOR Flash
  - Six chip-select pins for static memory, each can be configured separately
  - Support 8 or 16 bits data width
  - 6 bits address
- NAND flash interface
  - Support 4-bit/8-bit/12-bit/16-bit/24-bit MLC/TLC NAND as well as SLC NAND
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - Support automatic boot up from NAND Flash devices
- BCH Controller
  - Implement 4-bit/8-bit/12-bit/16-bit/20-bit/ 24-bit data ECC encoding and decoding

1.2.6 System Functions

- Clock generation and power management
  - On-chip oscillator circuit for an 32768Hz clock and an 12MHz clock
  - On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
  - PLL on/off is programmable by software
  - ICLK, PCLK, HCLK, HHCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
  - Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function
  - Support module power-down
- Timer and counter unit with PWM output and/or input edge counter
  - Provide eight separate channels, Six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer
  - One channel
  - 32-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 32 maskable interrupt sources from on-chip peripherals and external request through GPIO ports
  - Interrupt source and pending registers for software handling
  - Unmasked interrupts can wake up the chip in sleep or standby mode
- Watchdog timer
  - 16-bit counter in RTC clock with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Generate power-on reset
- Direct memory access controllers
  - BDMA controller
    - Support up to 3 independent DMA channels
    - Support data transfer between normal memory (NAND, SRAM, etc.) / BCH and system memory (DDR)
  - MDMA controller
    - Support up to 2 independent DMA channels
    - Support data transfer in system memory (DDR)
  - General purpose DMA
    - Support up to 10 independent DMA channels
    - Support data transfer between On-chip Peripherals (e.g. SMB, MSC, etc.) and

system memory (DDR)
    - APB bus bridge
  - Common features
    - Descriptor or No-Descriptor Transfer
    - Transfer data units: byte, 2-byte (half word), 4-byte (word), 16-byte, 32-byte or 64-byte
    - Transfer number of data unit: 1 ~ 224
    - Independent source and target port width: 8-bit, 16-bit, 32-bit
- SADC
  - 12-bit, 1Msps/200ksps
  - XP/XN, YP/YN inputs for touch screen
  - Battery voltage inputs for internal/external resistor divider respectively
  - 2 generic input channels
  - 5mW@1Msps, 2.2mW@200ksps
- RTC (Real Time Clock)
  - 32-bit second counter
  - 1Hz from 32768hz
  - Alarm interrupt
  - Independent power
  - A 32-bits scratch register used to indicate whether power down happens for RTC power

1.2.7 Peripherals

- General-Purpose I/O ports
  - Total GPIO pin number is 166, where 8 are dedicated and all others are shared
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
  - Each pin can be configured as open-drain when output
  - Each pin can be configured as internal resistor pull-up
- One-wire bus interface
  - Overdrive and regular speed
  - Master only
  - LSB first
  - Bit or byte operate modes
- Two SMB bus interfaces
  - Only supports single master mode
  - Supports SMB standard-mode and F/S-mode up to 400 kHz
  - Double-buffered for receiver and transmitter
  - Supports general call address and START byte format after START condition
- Two Synchronous serial interfaces (SSI0, SSI1)
  - Up to 50MHz speed

- Supports three formats: TI's SSP, National Microwire, and Motorola's SPI
- Configurable 2 - 17 (or multiples of them) bits data transfer
- Full-duplex/transmit-only/receive-only operation
- Supports normal transfer mode or Interval transfer mode
- Programmable transfer order: MSB first or LSB first
- 17-bit width, 128-level deep transmit-FIFO and receive-FIFO
- Programmable divider/prescaler for SSI clock
- Back-to-back character transmission/reception mode

- Four UARTs (UART0, UART1, UART2, UART3)
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 32x8bit FIFO for transmit and 32x11bit FIFO for receive data
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions
  - Support slow infrared asynchronous interface (IrDA)
  - IrDA function up to 115200bps baudrate
  - UART function up to 3.7Mbps baudrate
  - Hardware flow control
- Three MMC/SD/SDIO controllers (MSC0, MSC1, MSC2)
  - Support automatic boot up from MSC0, which has 4-bit data bus
  - MSC1 with 4-bit data bus
  - Compliant with "The MultiMediaCard System Specification version 4.2"
  - Compliant with "SD Memory Card Specification version 2.0" and "SDIO Card Specification version 1.0" with 1 command channel and 4 data channels
  - Up to 320 Mbps data rate in MSC0
  - Up to 320 Mbps data rate in MSC1
  - Supports up to 10 cards (including one SD card)
  - Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status
- USB 1.1 host interface
  - Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible
  - Full speed and low speed
  - Embedded USB 1.1 PHY
- USB 2.0 OTG interface
  - Compliant with USB protocol revision 2.0 OTG
  - High speed and full speed supported for device role
  - High speed, full speed and low speed supported for host role
  - Embedded USB OTG PHY
- Transport stream slave interface
  - 8-bit or 1-bit data bus selectable
  - Support PID filtering
- SIM IF
  - Supports normal card and UIM card

- 8-bit, 16-level receive-/transmit- FIFO
- Supports asynchronous character (T=0) communication modes
- Supports asynchronous block (T=1) communication modes
- Supports setting of clock-rate conversion factor F (372, 512, 558, etc.), and bit-rate adjustment factor D (1, 2, 4, 8, 16, 32, 12, 20, etc.)
- Supports extra guard time waiting
- Auto-error detection in T=0 receive mode
- Auto-character repeat in T=0 transmit mode
- Transforms inverted format to regular format and vice versa
- Support stop clock function in some power consuming sensitive applications

- OTP Slave Interface
  - Total 256 bits. Lower 128bits are read-able and write-able, Higher 128bits are read-able only

1.2.8 Bootrom

- 8kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	0.13um CMOS
Power supply voltage	General purpose I/O: 3.3 ± 0.3V DDR I/O for mDDR: 1.8V± 0.2V DDR I/O for DDR: 2.5V± 0.2V DDR I/O for DDR2: 1.8V± 0.2V NAND/SRAM I/O: 1.62V~3.6V RTC I/O: 1.7V~3.6V Core: 1.2 -0.1/+0.2 V
Package	BGA345 14mm x 14mm x 1.1mm, 0.65mm pitch
Operating frequency	528~600MHz

2 Packaging and Pinout Information

2.1 Overview

JZ4760B processor is offered in 345-pin LFBGA package, which is 14mm x 14mm x 1.1mm outline, 21 x 21 matrix ball grid array and 0.65mm ball pitch, show in Figure 2-1. The JZ4760B pin to ball assignment is show in Figure 2-2.

The detailed pin description is listed in Table2-1~Table2-26.

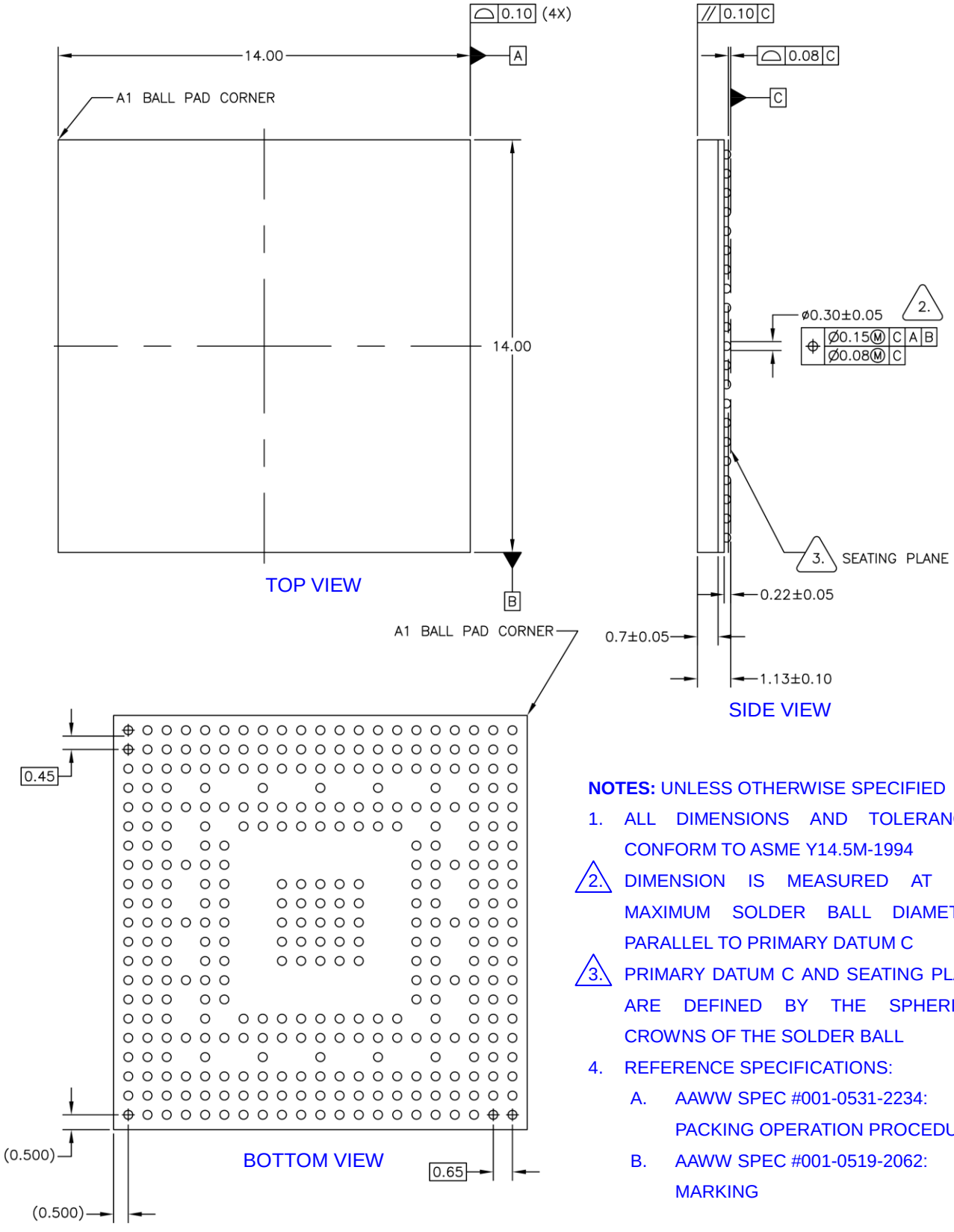
2.2 Solder Process

JZ4760B package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

JZ4760B package moisture sensitivity is level 3.

2.4 JZ4760B Package



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALL
4. REFERENCE SPECIFICATIONS:
   - A. AAWW SPEC #001-0531-2234: PACKING OPERATION PROCEDURE
   - B. AAWW SPEC #001-0519-2062: MARKING

Figure 2-1 JZ4760B package outline drawing

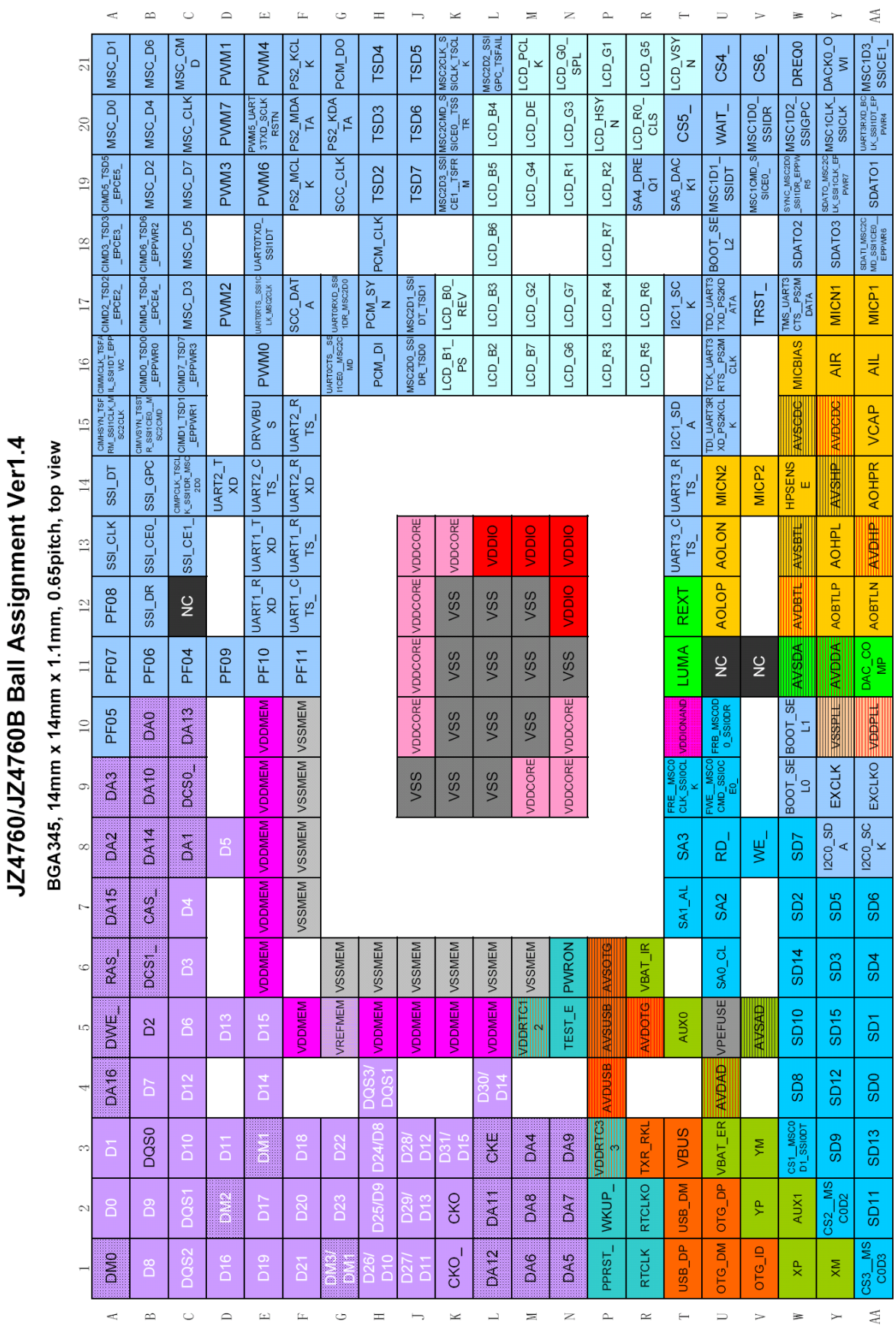


Figure 2-2 JZ4760B pin to ball assignment

2.5 Pin Description [1][2]

2.5.1 DDR

Table 2-1 DDR(mDDR, DDR2, DDR) Pins (66)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
D0	IO	A2	Bi-dir, Single-end	D0: DDR data bus bit 0 in 32-bit and 16-bit data bus	VDD_{MEM}
D1	IO	A3	Bi-dir, Single-end	D1: DDR data bus bit 1 in 32-bit and 16-bit data bus	VDD_{MEM}
D2	IO	B5	Bi-dir, Single-end	D2: DDR data bus bit 2 in 32-bit and 16-bit data bus	VDD_{MEM}
D3	IO	C6	Bi-dir, Single-end	D3: DDR data bus bit 3 in 32-bit and 16-bit data bus	VDD_{MEM}
D4	IO	C7	Bi-dir, Single-end	D4: DDR data bus bit 4 in 32-bit and 16-bit data bus	VDD_{MEM}
D5	IO	D8	Bi-dir, Single-end	D5: DDR data bus bit 5 in 32-bit and 16-bit data bus	VDD_{MEM}
D6	IO	C5	Bi-dir, Single-end	D6: DDR data bus bit 6 in 32-bit and 16-bit data bus	VDD_{MEM}
D7	IO	B4	Bi-dir, Single-end	D7: DDR data bus bit 7 in 32-bit and 16-bit data bus	VDD_{MEM}
D8	IO	B1	Bi-dir, Single-end	D8: DDR data bus bit 8 in 32-bit data bus	VDD_{MEM}
D9	IO	B2	Bi-dir, Single-end	D9: DDR data bus bit 9 in 32-bit data bus	VDD_{MEM}
D10	IO	C3	Bi-dir, Single-end	D10: DDR data bus bit 10 in 32-bit data bus	VDD_{MEM}
D11	IO	D3	Bi-dir, Single-end	D11: DDR data bus bit 11 in 32-bit data bus	VDD_{MEM}
D12	IO	C4	Bi-dir, Single-end	D12: DDR data bus bit 12 in 32-bit data bus	VDD_{MEM}
D13	IO	D5	Bi-dir, Single-end	D13: DDR data bus bit 13 in 32-bit data bus	VDD_{MEM}
D14	IO	E4	Bi-dir, Single-end	D14: DDR data bus bit 14 in 32-bit data bus	VDD_{MEM}
D15	IO	E5	Bi-dir, Single-end	D15: DDR data bus bit 15 in 32-bit data bus	VDD_{MEM}
D16	IO	D1	Bi-dir, Single-end	D16: DDR data bus bit 16 in 32-bit data bus	VDD_{MEM}
D17	IO	E2	Bi-dir, Single-end	D17: DDR data bus bit 17 in 32-bit data bus	VDD_{MEM}
D18	IO	F3	Bi-dir, Single-end	D18: DDR data bus bit 18 in 32-bit data bus	VDD_{MEM}
D19	IO	E1	Bi-dir, Single-end	D19: DDR data bus bit 19 in 32-bit data bus	VDD_{MEM}
D20	IO	F2	Bi-dir, Single-end	D20: DDR data bus bit 20 in 32-bit data bus	VDD_{MEM}
D21	IO	F1	Bi-dir, Single-end	D21: DDR data bus bit 21 in 32-bit data bus	VDD_{MEM}
D22	IO	G3	Bi-dir, Single-end	D22: DDR data bus bit 22 in 32-bit data bus	VDD_{MEM}
D23	IO	G2	Bi-dir, Single-end	D23: DDR data bus bit 23 in 32-bit data bus	VDD_{MEM}
D24 D8	IO	H3	Bi-dir, Single-end	D24: DDR data bus bit 24 in 32-bit data bus D8: DDR data bus bit 8 in 16-bit data bus	VDD_{MEM}
D25 D9	IO	H2	Bi-dir, Single-end	D25: DDR data bus bit 25 in 32-bit data bus D9: DDR data bus bit 9 in 16-bit data bus	VDD_{MEM}
D26 D10	IO	H1	Bi-dir, Single-end	D26: DDR data bus bit 26 in 32-bit data bus D10: DDR data bus bit 10 in 16-bit data bus	VDD_{MEM}
D27 D11	IO	J1	Bi-dir, Single-end	D27: DDR data bus bit 27 in 32-bit data bus D11: DDR data bus bit 11 in 16-bit data bus	VDD_{MEM}
D28 D12	IO	J3	Bi-dir, Single-end	D28: DDR data bus bit 28 in 32-bit data bus D12: DDR data bus bit 12 in 16-bit data bus	VDD_{MEM}
D29 D13	IO	J2	Bi-dir, Single-end	D29: DDR data bus bit 29 in 32-bit data bus D13: DDR data bus bit 13 in 16-bit data bus	VDD_{MEM}
D30 D14	IO	L4	Bi-dir, Single-end	D30: DDR data bus bit 30 in 32-bit data bus D14: DDR data bus bit 14 in 16-bit data bus	VDD_{MEM}
D31 D15	IO	K3	Bi-dir, Single-end	D31: DDR data bus bit 31 in 32-bit data bus D15: DDR data bus bit 15 in 16-bit data bus	VDD_{MEM}
DA0	O	B10	Output, Single-end	DA0: DDR address bus bit 0	VDD_{MEM}
DA1	O	C8	Output, Single-end	DA1: DDR address bus bit 1	VDD_{MEM}
DA2	O	A8	Output, Single-end	DA2: DDR address bus bit 2	VDD_{MEM}
DA3	O	A9	Output, Single-end	DA3: DDR address bus bit 3	VDD_{MEM}

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DA4	O	M3	Output, Single-end	DA4: DDR address bus bit 4	VDD_{MEM}
DA5	O	N1	Output, Single-end	DA5: DDR address bus bit 5	VDD_{MEM}
DA6	O	M1	Output, Single-end	DA6: DDR address bus bit 6	VDD_{MEM}
DA7	O	N2	Output, Single-end	DA7: DDR address bus bit 7	VDD_{MEM}
DA8	O	M2	Output, Single-end	DA8: DDR address bus bit 8	VDD_{MEM}
DA9	O	N3	Output, Single-end	DA9: DDR address bus bit 9	VDD_{MEM}
DA10	O	B9	Output, Single-end	DA10: DDR address bus bit 10	VDD_{MEM}
DA11	O	L2	Output, Single-end	DA11: DDR address bus bit 11	VDD_{MEM}
DA12	O	L1	Output, Single-end	DA12: DDR address bus bit 12	VDD_{MEM}
DA13	O	C10	Output, Single-end	DA13: DDR address bus bit 13	VDD_{MEM}
DA14	O	B8	Output, Single-end	DA14: DDR address bus bit 14	VDD_{MEM}
DA15	O	A7	Output, Single-end	DA15: DDR address bus bit 15	VDD_{MEM}
DA16	O	A4	Output, Single-end	DA16: DDR address bus bit 16	VDD_{MEM}
DCS0_	O	C9	Output, Single-end	DCS0_: DDR chip select 0	VDD_{MEM}
DCS1_	O	B6	Output, Single-end	DCS1_: DDR chip select 1	VDD_{MEM}
RAS_	O	A6	Output, Single-end	RAS_: DDR row address strobe	VDD_{MEM}
CAS_	O	B7	Output, Single-end	CAS_: DDR column address strobe	VDD_{MEM}
DWE_	O	A5	Output, Single-end	DWE_: DDR write enable	VDD_{MEM}
DQS0	IO	B3	Bi-dir, Single-end	DQS0: DDR data byte 0 strobe in 32-bit and 16-bit data bus	VDD_{MEM}
DQS1	IO	C2	Bi-dir, Single-end	DQS1: DDR data byte 1 strobe in 32-bit data bus	VDD_{MEM}
DQS2	IO	C1	Bi-dir, Single-end	DQS2: DDR data byte 2 strobe in 32-bit data bus	VDD_{MEM}
DQS3 DQS1	IO	H4	Bi-dir, Single-end	DQS3: DDR data byte 3 strobe in 32-bit data bus DQS1: DDR data byte 1 strobe in 16-bit data bus	VDD_{MEM}
DM0	O	A1	Output, Single-end	DM0: DDR data byte 0 mask in 32-bit and 16-bit data bus	VDD_{MEM}
DM1	O	E3	Output, Single-end	DM1: DDR data byte 1 mask in 32-bit data bus	VDD_{MEM}
DM2	O	D2	Output, Single-end	DM2: DDR data byte 2 mask in 32-bit data bus	VDD_{MEM}
DM3 DM1	O	G1	Output, Single-end	DM3: DDR data byte 3 mask in 32-bit data bus DM1: DDR data byte 1 mask in 16-bit data bus	VDD_{MEM}
CKO	O	K2	Output, Differential	CKO: DDR clock output	VDD_{MEM}
CKO_	O	K1		CKO_: DDR inverse clock output	VDD_{MEM}
CKE	O	L3	Output, Single-end	CKE: DDR clock enable	VDD_{MEM}
VREFmem	AI	G5		VREFmem: DDR/DDR2 input reference voltage	VDD_{MEM}

2.5.2 BOOT and storage

Table 2-2 Static-Memory/MSC0/SPI0/DMA/1WIRE Pins (36; all GPIO shared: PA0~29, PB0~5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD0 PA0	IO IO	AA4	4mA, pullup-pe	SD0: Static memory data bus bit 0 PA0: GPIO group A bit 0	VDDIOn
SD1 PA1	IO IO	AA5	4mA, pullup-pe	SD1: Static memory data bus bit 1 PA1: GPIO group A bit 1	VDDIOn
SD2 PA2	IO IO	W7	4mA, pullup-pe	SD2: Static memory data bus bit 2 PA2: GPIO group A bit 2	VDDIOn
SD3 PA3	IO IO	Y6	4mA, pullup-pe	SD3: Static memory data bus bit 3 PA3: GPIO group A bit 3	VDDIOn
SD4 PA4	IO IO	AA6	4mA, pullup-pe	SD4: Static memory data bus bit 4 PA4: GPIO group A bit 4	VDDIOn

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD5 PA5	IO IO	Y7	4mA, pullup-pe	SD5: Static memory data bus bit 5 PA5: GPIO group A bit 5	VDDIOn
SD6 PA6	IO IO	AA7	4mA, pullup-pe	SD6: Static memory data bus bit 6 PA6: GPIO group A bit 6	VDDIOn
SD7 PA7	IO IO	W8	4mA, pullup-pe	SD7: Static memory data bus bit 7 PA7: GPIO group A bit 7	VDDIOn
SD8 PA8	IO IO	W4	4mA, pullup-pe	SD8: Static memory data bus bit 8 PA8: GPIO group A bit 8	VDDIOn
SD9 PA9	IO IO	Y3	4mA, pullup-pe	SD9: Static memory data bus bit 9 PA9: GPIO group A bit 9	VDDIOn
SD10 PA10	IO IO	W5	4mA, pullup-pe	SD10: Static memory data bus bit 10 PA10: GPIO group A bit 10	VDDIOn
SD11 PA11	IO IO	AA2	4mA, pullup-pe	SD11: Static memory data bus bit 11 PA11: GPIO group A bit 11	VDDIOn
SD12 PA12	IO IO	Y4	4mA, pullup-pe	SD12: Static memory data bus bit 12 PA12: GPIO group A bit 12	VDDIOn
SD13 PA13	IO IO	AA3	4mA, pullup-pe	SD13: Static memory data bus bit 13 PA13: GPIO group A bit 13	VDDIOn
SD14 PA14	IO IO	W6	4mA, pullup-pe	SD14: Static memory data bus bit 14 PA14: GPIO group A bit 14	VDDIOn
SD15 PA15	IO IO	Y5	4mA, pullup-pe	SD15: Static memory data bus bit 15 PA15: GPIO group A bit 15	VDDIOn
SA0 (CL) PB0	O IO	U6	4mA, pullup-pe	SA0: Static memory address bus bit 0 If NAND flash is used, this pin is used as NAND CL (command latch) pin PB0: GPIO group B bit 0	VDDIOn
SA1 (AL) PB1	O IO	T7	4mA, pullup-pe	SA1: Static memory address bus bit 1 If NAND flash is used, this pin is used as NAND AL (address latch) pin PB1: GPIO group B bit 1	VDDIOn
SA2 PB2	O IO	U7	2mA, pullup-pe	SA2: Static memory address bus bit 2 PB2: GPIO group B bit 2	VDDIOn
SA3 PB3	O IO	T8	2mA, pullup-pe	SA3: Static memory address bus bit 3 PB3: GPIO group B bit 3	VDDIOn
SA4 DREQ1 PB4	O I IO	R19	2mA, pullup-pe	SA4: Static memory address bus bit 4 DREQ1: External DMA request input 1 PB4: GPIO group B bit 4	VDDIO
SA5 DACK1 PB5	O O IO	T19	2mA, pullup-pe	SA5: Static memory address bus bit 5 DACK1: External DMA acknowledge output 1 PB5: GPIO group B bit 5	VDDIO
RD_ PA16	O IO	U8	2mA, pullup-pe	RD_: Static memory read strobe PA16: GPIO group A bit 16	VDDIOn
WE_ PA17	O IO	V8	2mA, pullup-pe	WE_: Static memory write strobe PA17: GPIO group A bit 17	VDDIOn
FRE_ MSC0_CLK SSI0_CLK PA18	O O O IO	T9	4mA, pullup-pe	FRE_: NAND read enable MSC0_CLK: MSC (MMC/SD) 0 clock output SSI0_CLK: SSI 0 clock output PA18: GPIO group A bit 18	VDDIOn
FWE_ MSC0_CMD SSI0_CE0_ PA19	O IO O IO	U9	4mA, pullup-pe	FEW_: NAND write enable MSC0_CMD: MSC (MMC/SD) 0 command SSI0_CE0_: SSI 0 chip enable 0 PA19: GPIO group A bit 19	VDDIOn
MSC0_D0 SSI0_DR PA20 (FRB)	IO I IO I	U10	4mA, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 SSI0_DR: SSI 0 data input PA20: GPIO group A bit 20. If NAND flash is used, this pin should be used as NAND FRB (NAND flash ready/busy) input	VDDIOn
CS1_ MSC0_D1 SSI0_DT PA21	O IO O IO	W3	4mA, pullup-pe	CS1_: NAND/NOR/SRAM chip select 1 MSC0_D1: MSC (MMC/SD) 0 data bit 1 SSI0_DT: SSI 0 data output PA21: GPIO group A bit 21	VDDIOn

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CS2_ MSC0_D2 PA22	O IO IO	Y2	4mA, pullup-pe	CS2_: NAND/NOR/SRAM chip select 2 MSC0_D2: MSC (MMC/SD) 0 data bit 2 PA22: GPIO group A bit 22	VDDIOn
CS3_ MSC0_D3 PA23	O IO IO	AA1	4mA, pullup-pe	CS3_: NAND/NOR/SRAM chip select 3 MSC0_D3: MSC (MMC/SD) 0 data bit 3 PA23: GPIO group A bit 23	VDDIOn
CS4_ PA24	O IO	U21	2mA, pullup-pe	CS4_: NAND/NOR/SRAM chip select 4 PA24: GPIO group A bit 24	VDDIO
CS5_ PA25	O IO	T20	2mA, pullup-pe	CS5_: NAND/NOR/SRAM chip select 5 PA25: GPIO group A bit 25	VDDIO
CS6_ PA26	O IO	V21	2mA, pullup-pe	CS6_: NAND/NOR/SRAM chip select 6 PA26: GPIO group A bit 26	VDDIO
WAIT_ PA27	I IO	U20	2mA, pullup-pe	WAIT_: Slow static memory/device wait signal PA27: GPIO group A bit 27	VDDIO
DREQ0 PA28	I IO	W21	2mA, pullup-pe	DREQ0: External DMA request input 0 PA28: GPIO group A bit 28	VDDIO
DACK0 OWI PA29	O IO IO	Y21	2mA, pullup-pe	DACK0: External DMA acknowledge output 0 OWI: One wire interface PA29: GPIO group A bit 29	VDDIO

2.5.3 LCD

Table 2-3 LCDC Pins (28; all GPIO shared: PC0~27)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_B0 LCD_REV PC0	O O IO	K17	DrvP, SLP, pullup-pe	LCD_B0: LCD Blue data bit 0 LCD_REV: LCD REV output for special TFT PC0: GPIO group C bit 0	VDDIO[4]
LCD_B1 LCD_PS PC1	O O IO	K16	DrvP, SLP, pullup-pe	LCD_B1: LCD Blue data bit 1 LCD_PS: LCD PS output for special TFT PC1: GPIO group C bit 1	VDDIO[4]
LCD_B2 PC2	O IO	L16	DrvP, SLP, pullup-pe	LCD_B2: LCD Blue data bit 2 PC2: GPIO group C bit 2	VDDIO[4]
LCD_B3 PC3	O IO	L17	DrvP, SLP, pullup-pe	LCD_B3: LCD Blue data bit 3 PC3: GPIO group C bit 3	VDDIO[4]
LCD_B4 PC4	O IO	L20	DrvP, SLP, pullup-pe	LCD_B4: LCD Blue data bit 4 PC4: GPIO group C bit 4	VDDIO[4]
LCD_B5 PC5	O IO	L19	DrvP, SLP, pullup-pe	LCD_B5: LCD Blue data bit 5 PC5: GPIO group C bit 5	VDDIO[4]
LCD_B6 PC6	O IO	L18	DrvP, SLP, pullup-pe	LCD_B6: LCD Blue data bit 6 PC6: GPIO group C bit 6	VDDIO[4]
LCD_B7 PC7	O IO	M16	DrvP, SLP, pullup-pe	LCD_B7: LCD Blue data bit 7 PC7: GPIO group C bit 7	VDDIO[4]
LCD_PCLK PC8	O IO	M21	DrvP, SLP, pullup-pe	LCD_PCLK: LCD pixel clock PC8: GPIO group C bit 8	VDDIO[4]
LCD_DE PC9	O IO	M20	DrvP, SLP, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PC9: GPIO group C bit 9	VDDIO[4]
LCD_G0 LCD_SPL PC10	O O IO	N21	DrvP, SLP, pullup-pe	LCD_G0: LCD Green data bit 0 LCD_SPL: LCD SPL output PC10: GPIO group C bit 10	VDDIO[4]
LCD_G1 PC11	O IO	P21	DrvP, SLP, pullup-pe	LCD_G1: LCD Green data bit 1 PC11: GPIO group C bit 11	VDDIO[4]
LCD_G2 PC12	O IO	M17	DrvP, SLP, pullup-pe	LCD_G2: LCD Green data bit 2 PC12: GPIO group C bit 12	VDDIO[4]

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_G3 PC13	O IO	N20	DrvP, SLP, pullup-pe	LCD_G3: LCD Green data bit 3 PC13: GPIO group C bit 13	VDDIO[4]
LCD_G4 PC14	O IO	M19	DrvP, SLP, pullup-pe	LCD_G4: LCD Green data bit 4 PC14: GPIO group C bit 14	VDDIO[4]
LCD_G5 PC15	O IO	R21	DrvP, SLP, pullup-pe	LCD_G5: LCD Green data bit 5 PC15: GPIO group C bit 15	VDDIO[4]
LCD_G6 PC16	O IO	N16	DrvP, SLP, pullup-pe	LCD_G6: LCD Green data bit 6 PC16: GPIO group C bit 16	VDDIO[4]
LCD_G7 PC17	O IO	N17	DrvP, SLP, pullup-pe	LCD_G7: LCD Green data bit 7 PC17: GPIO group C bit 17	VDDIO[4]
LCD_HSYN PC18	IO IO	P20	DrvP, SLP, pullup-pe	LCD_HSYN: LCD line clock/horizontal sync PC18: GPIO group C bit 18	VDDIO[4]
LCD_VSYN PC19	IO IO	T21	DrvP, SLP, pullup-pe	LCD_VSYN: LCD frame clock/vertical sync PC19: GPIO group C bit 19	VDDIO[4]
LCD_R0 LCD_CLS PC20	O O IO	R20	DrvP, SLP, pullup-pe	LCD_R0: LCD Red data bit 0 LCD_CLS: LCD CLS output PC20: GPIO group C bit 20	VDDIO[4]
LCD_R1 PC21	O IO	N19	DrvP, SLP, pullup-pe	LCD_R1: LCD Red data bit 1 PC21: GPIO group C bit 21	VDDIO[4]
LCD_R2 PC22	O IO	P19	DrvP, SLP, pullup-pe	LCD_R2: LCD Red data bit 2 PC22: GPIO group C bit 22	VDDIO[4]
LCD_R3 PC23	O IO	P16	DrvP, SLP, pullup-pe	LCD_R3: LCD Red data bit 3 PC23: GPIO group C bit 23	VDDIO[4]
LCD_R4 PC24	O IO	P17	DrvP, SLP, pullup-pe	LCD_R4: LCD Red data bit 4 PC24: GPIO group C bit 24	VDDIO[4]
LCD_R5 PC25	O IO	R16	DrvP, SLP, pullup-pe	LCD_R5: LCD Red data bit 5 PC25: GPIO group C bit 25	VDDIO[4]
LCD_R6 PC26	O IO	R17	DrvP, SLP, pullup-pe	LCD_R6: LCD Red data bit 6 PC26: GPIO group C bit 26	VDDIO[4]
LCD_R7 PC27	O IO	P18	DrvP, SLP, pullup-pe	LCD_R7: LCD Red data bit 7 PC27: GPIO group C bit 27	VDDIO[4]

2.5.4 CIM

Table 2-4 CIM/TSSI/SSI1/MSC2/EPD Pins (12; all GPIO shared: PB6~17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM_PCLK TSCLK SSI1_DR MSC2_D0 PB6	I I I IO IO	C14	2mA, pullup-pe	CIM_PCLK: CIM pixel clock input TSCLK: TS interface clock input SSI1_DR: SSI 1 data input MSC2_D0: MSC (MMC/SD) 2 data bit 0 PB6: GPIO group B bit 6	VDDIO[3]
CIM_HSYN TSFRM SSI1_CLK MSC2_CLK PB7	I I O O IO	A15	2mA, pullup-pe	CIM_HSYN: CIM horizontal sync input TSFRM: TS interface frame valid input SSI1_CLK: SSI 1 clock output MSC2_CLK: MSC (MMC/SD) 2 clock output PB7: GPIO group B bit 7	VDDIO[3]
CIM_VSYN TSSTR SSI1_CE0_ MSC2_CMD PB8	I I O IO IO	B15	2mA, pullup-pe	CIM_VSYN: CIM vertical sync input TSSTR: TS interface frame start input SSI1_CE0_: SSI 1 chip enable 0 MSC2_CMD: MSC (MMC/SD) 2 command PB8: GPIO group B bit 8	VDDIO[3]

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM_MCLK TSFAIL SSI1_DT EPD_PWC PB9	O I O O IO	A16	2mA, pullup-pe	CIM_MCLK: CIM master clock output TSFAIL: TS interface error package indicator input SSI1_DT: SSI 1 data output EPD_PWC: EPD power control common PB9: GPIO group B bit 9	VDDIO[3]
CIM_D0 TSD0 EPD_PWR0 PB10	I I O IO	B16	2mA, pulldown-pe	CIM_D0: CIM data input bit 0 TSD0: TS interface input data bus bit 0 EPD_PWR0: EPD power control bit 0 PB10: GPIO group B bit 10	VDDIO[3]
CIM_D1 TSD1 EPD_PWR1 PB11	I I O IO	C15	2mA, pulldown-pe	CIM_D1: CIM data input bit 1 TSD1: TS interface input data bus bit 1 EPD_PWR1: EPD power control bit 1 PB11: GPIO group B bit 11	VDDIO[3]
CIM_D2 TSD2 EPD_SCE2_ PB12	I I O IO	A17	2mA, pullup-pe	CIM_D2: CIM data input bit 2 TSD2: TS interface input data bus bit 2 EPD_SCE2_: EPD source driver chip select 2 PB12: GPIO group B bit 12	VDDIO[3]
CIM_D3 TSD3 EPD_SCE3_ PB13	I I O IO	A18	2mA, pullup-pe	CIM_D3: CIM data input bit 3 TSD3: TS interface input data bus bit 3 EPD_SCE3_: EPD source driver chip select 3 PB13: GPIO group B bit 13	VDDIO[3]
CIM_D4 TSD4 EPD_SCE4_ PB14	I I O IO	B17	2mA, pullup-pe	CIM_D4: CIM data input bit 4 TSD4: TS interface input data bus bit 4 EPD_SCE4_: EPD source driver chip select 4 PB14: GPIO group B bit 14	VDDIO[3]
CIM_D5 TSD5 EPD_SCE5_ PB15	I I O IO	A19	2mA, pullup-pe	CIM_D5: CIM data input bit 5 TSD5: TS interface input data bus bit 5 EPD_SCE5_: EPD source driver chip select 5 PB15: GPIO group B bit 15	VDDIO[3]
CIM_D6 TSD6 EPD_PWR2 PB16	I I O IO	B18	2mA, pulldown-pe	CIM_D6: CIM data input bit 6 TSD6: TS interface input data bus bit 6 EPD_PWR2: EPD power control bit 2 PB16: GPIO group B bit 16	VDDIO[3]
CIM_D7 TSD7 EPD_PWR3 PB17	I I O IO	C16	2mA, pulldown-pe	CIM_D7: CIM data input bit 7 TSD7: TS interface input data bus bit 7 EPD_PWR3: EPD power control bit 3 PB17: GPIO group B bit 17	VDDIO[3]

2.5.5 TSSI/SSI/MSC/UART/SMB

Table 2-5 TSSI/MSC2/SSI Pins (12; all GPIO shared: PB20~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC2_D0 SSI0_DR SSI1_DR TSD0 PB20	IO I I I IO	J16	DrvP, SLP, pullup-pe	MSC2_D0: MSC (MMC/SD) 2 data bit 0 SSI0_DR: SSI 0 data input SSI1_DR: SSI 1 data input TSD0: TS slave interface input data bus bit 0 PB20: GPIO group B bit 20	VDDIO[4]
MSC2_D1 SSI0_DT SSI1_DT TSD1 PB21	IO O O I IO	J17	DrvP, SLP, pullup-pe	MSC2_D1: MSC (MMC/SD) 2 data bit 1 SSI0_DT: SSI 0 data output SSI1_DT: SSI 1 data output TSD1: TS interface input data bus bit 1 PB21: GPIO group B bit 21	VDDIO[4]
TSD2 PB22	I IO	H19	DrvP, SLP, pullup-pe	TSD2: TS interface input data bus bit 2 PB22: GPIO group B bit 22	VDDIO[4]
TSD3 PB23	I IO	H20	DrvP, SLP, pullup-pe	TSD3: TS interface input data bus bit 3 PB23: GPIO group B bit 23	VDDIO[4]

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TSD4 PB24	I IO	H21	DrvP, SLP, pullup-pe	TSD4: TS interface input data bus bit 4 PB24: GPIO group B bit 24	VDDIO[4]
TSD5 PB25	I IO	J21	DrvP, SLP, pullup-pe	TSD5: TS interface input data bus bit 5 PB25: GPIO group B bit 25	VDDIO[4]
TSD6 PB26	I IO	J20	DrvP, SLP, pullup-pe	TSD6: TS interface input data bus bit 6 PB26: GPIO group B bit 26	VDDIO[4]
TSD7 PB27	I IO	J19	DrvP, SLP, pullup-pe	TSD7: TS interface input data bus bit 7 PB27: GPIO group B bit 27	VDDIO[4]
MSC2_CLK SSI0_CLK SSI1_CLK TSCLK PB28	O O O I IO	K21	DrvP, SLP, pullup-pe	MSC2_CLK: MSC (MMC/SD) 2 clock output SSI0_CLK: SSI 0 clock output SSI1_CLK: SSI 1 clock output TSCLK: TS interface clock input PB28: GPIO group B bit 28	VDDIO[4]
MSC2_CMD SSI0_CE0_ SSI1_CE0_ TSSTR PB29	IO O O I IO	K20	DrvP, SLP, pullup-pe	MSC2_CMD: MSC (MMC/SD) 2 command SSI0_CE0_: SSI 0 chip enable 0 SSI1_CE0_: SSI 1 chip enable 0 TSSTR: TS interface frame start input PB29: GPIO group B bit 29	VDDIO[4]
MSC2_D2 SSI0_GPC SSI1_GPC TSFAIL PB30	IO O O I IO	L21	DrvP, SLP, pullup-pe	MSC2_D2: MSC (MMC/SD) 2 data bit 2 SSI0_GPC: SSI 0 general-purpose control signal SSI1_GPC: SSI 1 general-purpose control signal TSFAIL: TS interface error package indicator input PB30: GPIO group B bit 30	VDDIO[4]
MSC2_D3 SSI0_CE1_ SSI1_CE1_ TSFRM PB31	IO O O I IO	K19	DrvP, SLP, pullup-pe	MSC2_D3: MSC (MMC/SD) 2 data bit 3 SSI0_CE1_: SSI 0 chip enable 1 SSI1_CE1_: SSI 1 chip enable 1 TSFRM: TS interface frame valid input PB31: GPIO group B bit 31	VDDIO[4]

Table 2-6 UART0/SSI1/MSC2 Pins (4; all GPIO shared: PF0~3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RxD SSI1_DR MSC2_D0 PF0	I I IO IO	G17	DrvP, SLP, pullup-pe	UART0_RxD: UART 0 Receiving data SSI1DR: SSI 1 data input MSC2_D0: MSC (MMC/SD) 2 data bit 0 PF0: GPIO group F bit 0	VDDIO[4]
UART0_CTS_ SSI1_CE0_ MSC2_CMD PF1	I O IO IO	G16	DrvP, SLP, pullup-pe	UART0_CTS_: UART 0 CTS_ input SSI1_CE0_: SSI 1 chip enable 0 MSC2_CMD: MSC (MMC/SD) 2 command PF1: GPIO group F bit 1	VDDIO[4]
UART0_RTS_ SSI1_CLK MSC2_CLK PF2	O O O IO	E17	DrvP, SLP, pullup-pe	UART0_RTS_: UART 0 RTS_ output SSI1_CLK: SSI 1 clock output MSC2_CLK: MSC (MMC/SD) 2 clock output PF2: GPIO group F bit 2	VDDIO[4]
UART0_TxD SSI1_DT PF3	O O IO	E18	DrvP, SLP, pullup-pe	UART0_TxD: UART 0 transmitting data SSI1_DT: SSI 1 data output PF3: GPIO group F bit 3	VDDIO[4]

Table 2-7 MSC1/SSI, Pins (6; all GPIO shared: PD20~25)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC1_D0 SSI0_DR SSI1_DR PD20	IO I I IO	V20	4mA, pullup-pe	MSC1_D0: MSC (MMC/SD) 1 data bit 0 SSI0_DR: SSI 0 data input SSI1_DR: SSI 1 data input PD20: GPIO group D bit 20	VDDIO
MSC1_D1	IO	U19	4mA,	MSC1_D1: MSC (MMC/SD) 1 data bit 1	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI0_DT SSI1_DT PD21	O O IO		pullup-pe	SSI0_DT: SSI 0 data output SSI1_DT: SSI 1 data output PD21: GPIO group D bit 21	
MSC1_D2 SSI0_GPC SSI1_GPC PD22	IO O O IO	W20	4mA, pullup-pe	MSC1_D2: MSC (MMC/SD) 1 data bit 2 SSI0_GPC: SSI 0 general-purpose control signal SSI1_GPC: SSI 1 general-purpose control signal PD22: GPIO group D bit 22	VDDIO
MSC1_D3 SSI0_CE1_ SSI1_CE1_ PD23	IO O O IO	AA21	4mA, pullup-pe	MSC1_D3: MSC (MMC/SD) 1 data bit 3 SSI0_CE1_: SSI 0 chip enable 1 SSI1_CE1_: SSI 1 chip enable 1 PD23: GPIO group D bit 23	VDDIO
MSC1_CLK SSI0_CLK SSI1_CLK PD24	O O O IO	Y20	4mA, pullup-pe	MSC1_CLK: MSC (MMC/SD) 1 clock output SSI0_CLK: SSI 0 clock output SSI1_CLK: SSI 1 clock output PD24: GPIO group D bit 24	VDDIO
MSC1_CMD SSI0_CE0_ SSI1_CE0_ PD25	IO O O IO	V19	4mA, pullup-pe	MSC1_CMD: MSC (MMC/SD) 1 command SSI0_CE0_: SSI 0 chip enable 0 SSI1_CE0_: SSI 1 chip enable 0 PD25: GPIO group D bit 25	VDDIO

Table 2-8 UART1 Pins (4; all GPIO shared: PD26~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART1_RxD PD26	I IO	E12	2mA, pullup-pe	UART1_RxD: UART 1 Receiving data PD26: GPIO group D bit 26	VDDIO[3]
UART1_CTS_ PD27	I IO	F12	2mA, pullup-pe	UART1_CTS_: UART 1 CTS_ input PD27: GPIO group D bit 27	VDDIO[3]
UART1_TxD PD28	O IO	E13	2mA, pullup-pe	UART1_TxD: UART 1 transmitting data PD28: GPIO group D bit 28	VDDIO[3]
UART1_RTS_ PD29	O IO	F13	2mA, pullup-pe	UART1_RTS_: UART 1 RTS_ output PD29: GPIO group D bit 29	VDDIO[3]

Table 2-9 UART2 Pins (0/4/4; all GPIO shared: PC28~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART2_RxD PC28	I IO	F14	2mA, pullup-pe	UART2_RxD: UART 2 Receiving data PC28: GPIO group C bit 28	VDDIO[3]
UART2_CTS_ PC29	I IO	E14	2mA, pullup-pe	UART2_CTS_: UART 2 CTS_ input PC29: GPIO group C bit 29	VDDIO[3]
UART2_TxD PC30	O IO	D14	2mA, pullup-pe	UART2_TxD: UART 2 transmitting data PC30: GPIO group C bit 30	VDDIO[3]
UART2_RTS_ PC31	O IO	F15	2mA, pullup-pe	UART2_RTS_: UART 2 RTS_ output PC31: GPIO group C bit 31	VDDIO[3]

Table 2-10 SMB0/SMB1 Pins (4; all GPIO shared: PD30~31, PE30~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SMB0_SDA PD30	IO IO	Y8	4mA, pullup-pe	SMB0_SDA: SMB 0 serial data PD30: GPIO group D bit 30	VDDIO
SMB0_SCK PD31	IO IO	AA8	4mA, pullup-pe	SMB0_SCK: SMB 0 serial clock PD31: GPIO group D bit 31	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SMB1_SDA PE30	IO IO	T15	4mA, pullup-pe	SMB1_SDA: SMB 1 serial data PE30: GPIO group E bit 30	VDDIO
SMB1_SCK PE31	IO IO	T17	4mA, pullup-pe	SMB1_SCK: SMB 1 serial clock PE31: GPIO group E bit 31	VDDIO

Table 2-11 MSC0/MSC1/MSC2 Pins (10; all GPIO shared: PE20~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_CLK MSC1_CLK MSC2_CLK PE28	O O O IO	C20	DrvP, SLP, pullup-pe	MSC0_CLK: MSC (MMC/SD) 0 clock output MSC1_CLK: MSC (MMC/SD) 1 clock output MSC2_CLK: MSC (MMC/SD) 2 clock output PE28: GPIO group E bit 28	VDDIO[4]
MSC0_CMD MSC1_CMD MSC2_CMD PE29	IO IO IO IO	C21	DrvP, SLP, pullup-pe	MSC0_CMD: MSC (MMC/SD) 0 command MSC1_CMD: MSC (MMC/SD) 1 command MSC2_CMD: MSC (MMC/SD) 2 command PE29: GPIO group E bit 29	VDDIO[4]
MSC0_D0 MSC1_D0 MSC2_D0 PE20	IO IO IO IO	A20	DrvP, SLP, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 MSC1_D0: MSC (MMC/SD) 1 data bit 0 MSC2_D0: MSC (MMC/SD) 2 data bit 0 PE20: GPIO group E bit 20	VDDIO[4]
MSC0_D1 MSC1_D1 MSC2_D1 PE21	IO IO IO IO	A21	DrvP, SLP, pullup-pe	MSC0_D1: MSC (MMC/SD) 0 data bit 1 MSC1_D1: MSC (MMC/SD) 1 data bit 1 MSC2_D1: MSC (MMC/SD) 2 data bit 1 PE21: GPIO group E bit 21	VDDIO[4]
MSC0_D2 MSC1_D2 MSC2_D2 PE22	IO IO IO IO	B19	DrvP, SLP, pullup-pe	MSC0_D2: MSC (MMC/SD) 0 data bit 2 MSC1_D2: MSC (MMC/SD) 1 data bit 2 MSC2_D2: MSC (MMC/SD) 2 data bit 2 PE22: GPIO group E bit 22	VDDIO[4]
MSC0_D3 MSC1_D3 MSC2_D3 PE23	IO IO IO IO	C17	DrvP, SLP, pullup-pe	MSC0_D3: MSC (MMC/SD) 0 data bit 3 MSC1_D3: MSC (MMC/SD) 1 data bit 3 MSC2_D3: MSC (MMC/SD) 2 data bit 3 PE23: GPIO group E bit 23	VDDIO[4]
MSC0_D4 MSC1_D4 MSC2_D4 PE24	IO IO IO IO	B20	DrvP, SLP, pullup-pe	MSC0_D4: MSC (MMC/SD) 0 data bit 4 MSC1_D4: MSC (MMC/SD) 1 data bit 4 MSC2_D4: MSC (MMC/SD) 2 data bit 4 PE24: GPIO group E bit 24	VDDIO[4]
MSC0_D5 MSC1_D5 MSC2_D5 PE25	IO IO IO IO	C18	DrvP, SLP, pullup-pe	MSC0_D5: MSC (MMC/SD) 0 data bit 5 MSC1_D5: MSC (MMC/SD) 1 data bit 5 MSC2_D5: MSC (MMC/SD) 2 data bit 5 PE25: GPIO group E bit 25	VDDIO[4]
MSC0_D6 MSC1_D6 MSC2_D6 PE26	IO IO IO IO	B21	DrvP, SLP, pullup-pe	MSC0_D6: MSC (MMC/SD) 0 data bit 6 MSC1_D6: MSC (MMC/SD) 1 data bit 6 MSC2_D6: MSC (MMC/SD) 2 data bit 6 PE26: GPIO group E bit 26	VDDIO[4]
MSC0_D7 MSC1_D7 MSC2_D7 PE27	IO IO IO IO	C19	DrvP, SLP, pullup-pe	MSC0_D7: MSC (MMC/SD) 0 data bit 7 MSC1_D7: MSC (MMC/SD) 1 data bit 7 MSC2_D7: MSC (MMC/SD) 2 data bit 7 PE27: GPIO group E bit 27	VDDIO[4]

Table 2-12 SSI0/SSI1 Pins (6; all GPIO shared: PE14~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI0_DR SSI1_DR PE14	I I IO	B12	2mA, pullup-pe	SSI0_DR: SSI 0 data input SSI1_DR: SSI 1 data input PE14: GPIO group E bit 14	VDDIO[3]
SSI0_CLK	O	A13	2mA,	SSI0_CLK: SSI 0 clock output	VDDIO[3]

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI1_CLK PE15	O IO		pullup-pe	SSI1_CLK: SSI 1 clock output PE15: GPIO group E bit 15	
SSI0_CE0_ SSI1_CE0_ PE16	O O IO	B13	2mA, pullup-pe	SSI0_CE0_: SSI 0 chip enable 0 SSI1_CE0_: SSI 1 chip enable 0 PE16: GPIO group E bit 16	VDDIO[3]
SSI0_DT SSI1_DT PE17	O O IO	A14	2mA, pullup-pe	SSI0_DT: SSI 0 data output SSI1_DT: SSI 1 data output PE17: GPIO group E bit 17	VDDIO[3]
SSI0_CE1_ SSI1_CE1_ PE18	O O IO	C13	2mA, pullup-pe	SSI0_CE1_: SSI 0 chip enable 1 SSI1_CE1_: SSI 1 chip enable 1 PE18: GPIO group E bit 18	VDDIO[3]
SSI0_GPC SSI1_GPC PE19	O O IO	B14	2mA, pullup-pe	SSI0_GPC: SSI 0 general-purpose control signal SSI1_GPC: SSI 1 general-purpose control signal PE19: GPIO group E bit 19	VDDIO[3]

2.5.6 PCM0/PCM1/PS2/SCC/PWM/AIC/UART

Table 2-13 PCM0/PS2/SCC Pins (10; all GPIO shared: PD0~9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PCM0_DO PD0	O IO	G21	DrvP, SLP, pullup-pe	PCM0_DO: PCM0 data out PD0: GPIO group D bit 0	VDDIO[4]
PCM0_CLK PD1	IO IO	H18	DrvP, SLP, pullup-pe	PCM0_CLK: PCM0 clock PD1: GPIO group D bit 1	VDDIO[4]
PCM0_SYN PD2	IO IO	H17	DrvP, SLP, pullup-pe	PCM0_SYN: PCM0 sync PD2: GPIO group D bit 2	VDDIO[4]
PCM0_DI PD3	I IO	H16	DrvP, SLP, pullup-pe	PCM0_DI: PCM0 data in PD3: GPIO group D bit 3	VDDIO[4]
PS2_MCLK PD4	IO IO	F19	DrvP, SLP, pullup-pe	PS2_MCLK: PS/2 mouse clock PD4: GPIO group D bit 4	VDDIO[4]
PS2_MDATA PD5	IO IO	F20	DrvP, SLP, pullup-pe	PS2_MDATA: PS/2 mouse data PD5: GPIO group D bit 5	VDDIO[4]
PS2_KCLK PD6	IO IO	F21	DrvP, SLP, pullup-pe	PS2_KCLK: PS/2 keyboard clock PD6: GPIO group D bit 6	VDDIO[4]
PS2_KDATA PD7	IO IO	G20	DrvP, SLP, pullup-pe	PS2_KDATA: PS/2 keyboard data PD7: GPIO group D bit 7	VDDIO[4]
SCC_DATA PD8	IO IO	F17	DrvP, SLP, pullup-pe	SCC_DATA: Smartcard controller (7816-3) data PD8: GPIO group D bit 8	VDDIO[4]
SCC_CLK PD9	O IO	G19	DrvP, SLP, pullup-pe	SCC_CLK: Smartcard controller (7816-3) clock PD9: GPIO group D bit 9	VDDIO[4]

Table 2-14 UART3/AIC/PWM/EPD/PCM1 Pins (17; all GPIO shared: PE0~9, 11~13, PD10~13)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 PE0	IO IO	E16	DrvP, SLP, pulldown-pe	PWM0: PWM output or pulse input 0 PE0: GPIO group E bit 0. Pull-down not enabled at and after reset	VDDIO[4]
PWM1 PE1	O IO	D21	DrvP, SLP, pulldown-pe	PWM1: PWM 1 output. This PWM can run in sleep mode in RTCLK clock PE1: GPIO group E bit 1. Pull-down not enabled at and after reset	VDDIO[4]
PWM2 PE2	O IO	D17	DrvP, SLP, pullup-pe	PWM2: PWM 2 output. This PWM can run in sleep mode in RTCLK clock PE2: GPIO group E bit 2. Pull-up not enabled at and after reset	VDDIO[4]
PWM3 PE3	IO IO	D19	DrvP, SLP, pullup-pe	PWM3: PWM output or pulse input 3 PE3: GPIO group E bit 3. Pull-up not enabled at and after reset	VDDIO[4]

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM4 PE4	IO IO	E21	DrvP, SLP, pullup-pe	PWM4: PWM output or pulse input 4 PE4: GPIO group E bit 4	VDDIO[4]
PWM5 UART3_TxD SCLK_RSTN PCM1_DO PE5	IO O O O IO	E20	DrvP, SLP, pullup-pe	PWM5: PWM output or pulse input 5 UART3_TxD: UART 3 transmitting data SCLK_RSTN: AIC I2S system clock output or AC97 reset output PCM1_DO: PCM1 data out PE5: GPIO group E bit 5	VDDIO[4]
PWM6 PD10	IO IO	E19	DrvP, SLP, pullup-pe	PWM6: PWM output or pulse input 6 PD10: GPIO group D bit 10	VDDIO[4]
PWM7 PD11	IO IO	D20	DrvP, SLP, pullup-pe	PWM7: PWM output or pulse input 7 PD11: GPIO group D bit 11	VDDIO[4]
UART3_RxD BCLK EPD_PWR4 PCM1_SYN PD12	I IO O IO IO	AA20	2mA, pulldown-pe	UART3_RxD: UART 3 Receiving data BCLK: AIC AC97/I2S bit clock EPD_PWR4: EPD power control bit 4 PCM1_SYN: PCM1 sync PD12: GPIO group D bit 12	VDDIO
SYNC MSC2_D0 EPD_PWR5 PD13	IO IO O IO	W19	2mA, pulldown-pe	SYNC: AC97 frame SYNC or I2S Left/Right MSC2_D0: MSC (MMC/SD) 2 data bit 0 EPD_PWR5: EPD power control bit 5 PD13: GPIO group D bit 13	VDDIO
SDATI MSC2_CMD EPD_PWR6 PE6	I IO O IO	AA18	2mA, pullup-pe	SDATI: AC97/I2S serial data input MSC2_CMD: MSC (MMC/SD) 2 command EPD_PWR6: EPD power control bit 6 PE6: GPIO group E bit 6	VDDIO
SDATO MSC2_CLK EPD_PWR7 PE7	O O O IO	Y19	2mA, pulldown-pe	SDATO: AC97/I2S serial data output or SPDIF output MSC2_CLK: MSC (MMC/SD) 2 clock output EPD_PWR7: EPD power control bit 7 PE7: GPIO group E bit 7	VDDIO
UART3_CTS_ PCM1_DI PE8	I I IO	T13	2mA, pullup-pe	UART3_CTS_: UART 3 CTS_ input PCM1_DI: PCM1 data in PE8: GPIO group E bit 8	VDDIO
UART3_RTS_ PCM1_CLK PE9	O O O	T14	2mA, pullup-pe	UART3_RTS_: UART 3 RTS_ output PCM1_CLK: PCM1 clock PE9: GPIO group E bit 9	VDDIO
SDATO1 PE11	O IO	AA19	2mA, pullup-pe	SDATO1: AIC I2S serial data output 1 PE11: GPIO group E bit 11	VDDIO
SDATO2 PE12	O IO	W18	2mA, pullup-pe	SDATO2: AIC I2S serial data output 2 PE12: GPIO group E bit 12	VDDIO
SDATO3 PE13	O IO	Y18	2mA, pullup-pe	SDATO3: AIC I2S serial data output 3 PE13: GPIO group E bit 13	VDDIO

2.5.7 System/JTAG/UART3/OTG/GPIO

Table 2-15 GPIO Pins (8, GPIO PF04~11)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PF4	IO	C11	2mA, pulldown-pe	PF4: GPIO group F bit 4. Pull-down not enabled at and after reset	VDDIO[3]
PF5	IO	A10	2mA, pulldown-pe	PF5: GPIO group F bit 5. Pull-down not enabled at and after reset	VDDIO[3]
PF6	IO	B11	2mA, pulldown-pe	PF6: GPIO group F bit 6. Pull-down not enabled at and after reset	VDDIO[3]
PF7	IO	A11	2mA, pulldown-pe	PF7: GPIO group F bit 7. Pull-down not enabled at and after reset	VDDIO[3]
PF8	IO	A12	2mA, pulldown-pe	PF8: GPIO group F bit 8. Pull-down not enabled at and after reset	VDDIO[3]

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PF9	IO	D11	2mA, pulldown-pe	PF9: GPIO group F bit 9. Pull-down not enabled at and after reset	VDDIO[3]
PF10	IO	E11	2mA, pulldown-pe	PF10: GPIO group F bit 10. Pull-down not enabled at and after reset	VDDIO[3]
PF11	IO	F11	2mA, pulldown-pe	PF11: GPIO group F bit 11. Pull-down not enabled at and after reset	VDDIO[3]

Table 2-16 JTAG/UART3/PS2 Pins (5, GPIO PA03~31 are used to control)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST_	I	V17	Schmitt, pull-down	TRST_: JTAG reset	VDDIO
TCK UART3_RTS_ PS2_MCLK	I O IO	U16	2mA, Schmitt, pull-down	TCK: JTAG clock UART3_RTS_: UART 3 RTS_ output, PA31 is used to select between JTAG and UART PS2_MCLK: PS/2 mouse clock, PA30 is used to select between JTAG and PS2	VDDIO
TMS UART3_CTS_ PS2_MDATA	I I IO	W17	2mA, Schmitt, pull-up	TMS: JTAG mode select UART3_CTS_: UART 3 CTS_ input, PA31 is used to select between JTAG and UART PS2_MDATA: PS/2 mouse data, PA30 is used to select between JTAG and PS2	VDDIO
TDI UART3_RxD PS2_KCLK	I I IO	U15	2mA, Schmitt, pull-up	TDI: JTAG serial data input UART3_RxD: UART 3 Receiving data, PA31 is used to select between JTAG and UART PS2_KCLK: PS/2 keyboard clock, PA30 is used to select between JTAG and PS2	VDDIO
TDO UART3_TxD PS2_KDATA	O O IO	U17	4mA, Schmitt, pull-up	TDO: JTAG serial data output UART3_TxD: UART 3 transmitting data, PA31 is used to select between JTAG and UART PS2_KDATA: PS/2 keyboard data, PA30 is used to select between JTAG and PS2	VDDIO

Table 2-17 System Pins (3, all GPIO shared: PD17~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PD17 (BOOT_SEL0)	I IO	W9	2mA, pullup-pe	PD17: GPIO group D bit 17 It is taken as BOOT select bit 0 by Boot ROM code	VDDIO
PD18 (BOOT_SEL1)	I IO	W10	2mA, pullup-pe	PD18: GPIO group D bit 18 It is taken as BOOT select bit 1 by Boot ROM code	VDDIO
PD19 (BOOT_SEL2)	I IO	U18	2mA, pullup-pe	PD19: GPIO group D bit 19 It is taken as BOOT select bit 2 by Boot ROM code	VDDIO

Table 2-18 USB OTG Digital Pins (0/1/1, all GPIO shared: PE10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DRVVBUS PE10	O IO	E15	2mA, pulldown-pe	DRVVBUS: USB OTG VBUS driver control signal PE10: GPIO group E bit 10	VDDIO[3]

2.5.8 Digital power/ground

Table 2-19 IO/Core power supplies for FBGA-345 package (46)

Pin Names	IO	Loc	Pin Description	Power
VDDmem	P	E6 E7 E8 E9 E10 F5 H5 J5 K5 L5	VDDmem: 10 IO digital power for DDR, 1.8V~2.5V	-
VSSmem	P	F7 F8 F9 F10 G6 H6 J6 K6 L6 M6	VSSmem: 10 IO digital ground for DDR, 0V	-
VDDIOn	P	T10	VDDIOn: (or VDDIOnand) 1 IO digital power for NAND power domain, 1.8V~3.3V	-
VDDIO	P	L13 M13 N12 N13	VDDIO: 4 IO digital power for none DDR/NAND, 3.3V	-
VSS	P	J9 K9 K10 K11 K12 L9 L10 L11 L12 M10 M11 M12 N11	VSS: 13 IO digital ground for none DDR and CORE digital ground, 0V	-
VDDcore	P	J10 J11 J12 J13 K13 M9 N9 N10	VDDcore: 8 CORE digital power, 1.2V	-

2.5.9 Analog

Table 2-20 Audio CODEC Pins (21)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AOHPL	AO	Y13		AOHPL: Left headphone out	AVD_{CDC}
AOHPR	AO	AA14		AOHPR: Right headphone out	AVD_{CDC}
AOBTLP	AO	Y12		AOBTLP: BTL out positive	AVD_{CDC}
AOBTLN	AO	AA12		AOBTLN: BTL out negative	AVD_{CDC}
AOLP	AO	U12		AOLP: Line out positive	AVD_{CDC}
AOLN	AO	U13		AOLN: Line out negative	AVD_{CDC}
MICP1	AI	AA17		MICP1: Microphone 1 input positive This pin should be floating if MIC1 is used as single-ended MIC input.	AVD_{CDC}
MICN1	AI	Y17		MICN1: Microphone 1 input negative.	AVD_{CDC}
MICP2	AI	V14		MICP2: Microphone 2 input positive. This pin should be floating if MIC2 is used as single-ended MIC input.	AVD_{CDC}
MICN2	AI	U14		MICN2: Microphone 2 input negative.	AVD_{CDC}
MICBIAS	AO	W16		MICBIAS: Microphone bias	AVD_{CDC}
AIL	AI	AA16		AIL: Left line input	AVD_{CDC}
AIR	AI	Y16		AIR: Right line input	AVD_{CDC}
VCAP	AO	AA15		VCAP: Voltage Reference Output. An electrolytic capacitor more than 10μF in parallel with a 0.1μF ceramic capacitor attached from this pin to AVSCDC eliminates the effects of high frequency noise.	AVD_{CDC}
HPSENSE	AI	W14		HPSENSE: Sense of headphone jack insertion	AVD_{CDC}
AVDCDC	P	Y15		AVDCDC: CODEC analog power, 3.3V (VDDA + VREFP)	-
AVSCDC	P	W15		AVSCDC: CODEC analog ground (VSSA + VREFN)	-
AVDHP	P	AA13		AVDHP: Headphone amplifier power, 3.3V (VDDAO, double PAD)	-
AVSHP	P	Y14		AVSHP: Headphone amplifier ground (VSSAO, double PAD)	-
AVDBTL	P	W12		AVDBTL: BTL amplifier power, 3.3V (VDDAO, double PAD)	-
AVSBTL	P	W13		AVSBTL: BTL amplifier ground (VSSAO, double PAD)	-

Table 2-21 USB 2.0 OTG, USB 1.1 host (9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
OTG_DP	AIO	U2		OTG_DP: USB OTG data plus	AVD_{OTG}[3]
OTG_DM	AIO	U1		OTG_DM: USB OTG data minus	AVD_{OTG}[3]
VBUS	AIO	T3		VBUS: USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin	AVD_{OTG}[3]
OTG_ID	AI	V1		OTG_ID: USB mini-receptacle identifier. It differentiates a mini-A from a mini-B plug. If this signal is not used, internal resistance pulls the signal's voltage level to AVDOTG.	AVD_{OTG}
TXR_RKL	AIO	R3		TXR_RKL: Transmitter resister tune. It connects to an external resistor of 44.2Ω with 1% tolerance to analog ground AVSOTG, that adjusts the USB 2.0 high-speed source impedance	AVD_{OTG}
AVDOTG	P	R5		AVDOTG: USB OTG analog power, 3.3V	-
AVSOTG	P	P6		AVSOTG: USB OTG analog ground	-
USB_DP	AIO	T1		USB_DP: USB 1.1 host data plus	AVD_{USB}
USB_DM	AIO	T2		USB_DM: USB 1.1 host data minus	AVD_{USB}
AVDUSB	P	P4		AVDUSB: USB 1.1 host analog power, 3.3V	-
AVSUSB	P	P5		AVSUSB: USB 1.1 host analog ground	-

Table 2-22 SAR ADC Pins (10)[3]

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
XP	AI	W1		XP: Touch screen X+ input	AVD_{AD}
XM	AI	Y1		XM: Touch screen X- input	AVD_{AD}
YP	AI	V2		YP: Touch screen Y+ input	AVD_{AD}
YM	AI	V3		YM: Touch screen Y- input. It is recommended to connect YM to top, YP to bottom, XM to left and XP to right.	AVD_{AD}
VBAT_IR	AI	R6		VBAT_IR: Battery voltage input with internal resistance divider	AVD_{AD}
AUX0	AI	T5		AUX0: ADC general purpose input 0, high speed ADC	AVD_{AD}
AUX1	AI	W2		AUX1: ADC general purpose input 1	AVD_{AD}
VBAT_ER	AI	U3		VBAT_ER: ADC general purpose input 2 or battery voltage input with external resistance divider	AVD_{AD}
AVDAD	P	U4		AVDAD: ADC analog power, 3.3 V	-
AVSAD	P	V5		AVDAD: ADC analog ground	-

Table 2-23 EFUSE Pins (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VPEFUSE	P	U5		VPEFUSE: EFUSE programming power, 3.3V/6.5V. Normal VPEFUSE = 3.3V； During program VPEFUSE = 6.5 +/- 0.25V	AVD_{AD}

Table 2-24 Video DAC Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LUMA	AO	T11		LUMA: DAC analog output for CVBS or luminance of S-Video	AVD_{DA}
AVDDA	P	Y11		AVDDA: Power supply for LUMA output, 3.3 V (IO1:AVD33R, IO2:AVD33G, IO3:AVDD, VDWELL)	-
AVSDA	P	W11		AVSDA: Ground for LUMA output (IO1/IO2: AVS33R, AVS33G, AVSS, VSSUB)	-
REXT	AO	T12		REXT: For external resistor. REXT(ohm)=265	AVD_{DA}
COMP	AIO	AA11		COMP: Compensation pin. This pin should be connected with 0.01uf ceramic cap parallel with a 10uf tantalum cap to AVDDAO externally	AVD_{DA}

Table 2-25 CPM Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK	AI	Y9	2~30 MHz Oscillator, OSC on/off	EXCLK: OSC input or 12MHz clock input	VDDIO
EXCLKO	AO	AA9		EXCLKO: OSC output	VDDIO
VDDPLL	P	AA10		VDDPLL: PLL analog power, 1.2V	-
VSSPLL	P	Y10		VSSPLL: PLL analog ground	-

Table 2-26 RTC Pins (8, 1 with GPIO input: PA30)[3]

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	R1	32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
RTCLKO	AO	R2		RTCLKO: OSC output or 32768Hz clock input	VDD_{RTC}
PWRON	O	N6	2mA	PWRON: Power on/off control of main power	VDD_{RTC} [3]
WKUP PA30	I I	P2	Schmitt	WKUP: Wakeup signal after main power down PA30: GPIO group A bit 30, input/interrupt only	VDD_{RTC} [3]
PPRST_	I	P1	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC} [3]
VDDRTC	P	P3		VDDRTC: 1.8V power for RTC and hibernating mode controlling that never power down	-
VDDRTC12	P	M5		VDDRTC12: 1.2V power for RTC and hibernating mode controlling that never power down	-
TEST_E	I	N5	Schmitt, pull-down	TEST_E: Manufacture test enable, program readable	VDD_{RTC} [3]

NOTES:

1 The meaning of phases in IO cell characteristics are:

a Bi-dir, Single-end: bi-direction and single-ended DDR IO are used.

b Output, Single-end: output and single-ended DDR IO are used.

c Output, Differential: output and differential signal DDR IO are used.

d 2/4mA out: The IO cell's output driving strength is about 2/4mA.

e Pull-up: The IO cell contains a pull-up resistor.

f Pull-down: The IO cell contains a pull-down resistor.

g Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.

h Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be

enabled or disabled by setting corresponding register.

i Schmitt: The IO cell is Schmitt trig input.

j DrvP: IO output driven strength programmable, which can be select from 2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA and 16mA

k SLP: IO output slew rate control able, which can be enabled or disabled

2 Except following pins, all GPIO shared pins are reset to GPIO input with internal pull-up or pull-down enabled. The following GPIO shared pins are reset to GPIO input with internal pull-up or pull-down disabled:
PWM0/PE0, PWM1/PE1, PWM2/PE2, PWM3/PE3, PF4~PF11.

3 These IOs are 5V input tolerance.

4 These IOs are with programmable output driven strength

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDmem power supplies voltage	-0.5	4.6	V
VDDIO power supplies voltage	-0.5	4.6	V
VDDIOn power supplies voltage	-0.5	4.6	V
VDDRTC power supplies voltage	-0.5	4.6	V
VDDRTC12 power supplies voltage	-0.2	2.2	V
AVDOTG power supplies voltage	-0.5	4.6	V
AVDUSB power supplies voltage	-0.5	4.6	V
AVDAD power supplies voltage	-0.5	4.6	V
VPEFUSE power supplies voltage	-0.5	4.6	V
VDDcore power supplies voltage	-0.2	2.2	V
VDDPLL power supplies voltage	-0.5	2.5	V
AVDDA power supplies voltage	-0.5	4.6	V
AVDCDC power supplies voltage	-0.5	4.6	V
AVDHP power supplies voltage	-0.5	4.6	V
AVDBTL power supplies voltage	-0.5	4.6	V
Input voltage to VDDmem supplied non-supply pins	-0.3	4.6	V
Input voltage to VDDIO supplied non-supply pins with 5V tolerance	-0.5	6	V
Input voltage to VDDIO supplied non-supply pins without 5V tolerance	-0.5	4.6	V
Input voltage to VDDIOn supplied non-supply pins	-0.5	4.6	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	6	V
Input voltage to AVDOTG supplied non-supply pins	-0.5	5.25	V
Input voltage to AVDUSB supplied non-supply pins	-0.5	6	V
Input voltage to AVDAD supplied non-supply pins	-0.5	6	V
Input voltage to AVDDA supplied non-supply pins	-0.5	4.6	V
Input voltage to AVDCDC supplied non-supply pins	-0.5	4.6	V
Output voltage from VDDmem supplied non-supply pins	-0.5	4.6	V
Output voltage from VDDIO supplied non-supply pins	-0.5	4.6	V
Output voltage from VDDIOn supplied non-supply pins	-0.5	4.6	V

Output voltage from VDDRTC supplied non-supply pins	-0.5	4.6	V
Output voltage from AVDOTG supplied non-supply pins	-0.5	4.6	V
Output voltage from AVDUSB supplied non-supply pins	-0.5	4.6	V
Output voltage from AVDAD supplied non-supply pins	-0.5	4.6	V
Output voltage from AVDDA supplied non-supply pins	-0.5	4.6	V
Output voltage from AVDCDC supplied non-supply pins	-0.5	4.6	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
V_{MEM}	VDDmem voltage for SSTL18	1.7	1.8	1.9	V
	VDDmem voltage for SSTL2	2.3	2.5	2.7	V
	VDDmem voltage for LPDDR	1.7	1.8	1.9	V
V_{IO}	VDDIO voltage	2.97	3.3	3.63	V
V_{ION}	VDDIOn voltage for 1.8V NAND	1.62	1.8	1.98	V
	VDDIOn voltage for 2.5V NAND	2.25	2.5	2.75	V
	VDDIOn voltage for 3.3V NAND	2.97	3.3	3.63	V
V_{RTC}	VDDRTC voltage	1.7	3.3	3.63	V
V_{RTC12}	VDDRTC12 voltage	1.08	1.2	1.40	V
V_{OTG}	AVDOTG voltage	3.07	3.3	3.63	V
V_{USB}	AVDUSB voltage	3.0	–	3.6	V
V_{ADC}	AVDAD voltage	2.7	3.3	3.6	V
V_{EFUSE}	VPEFUSE voltage	2.97	3.3	–	V
V_{CORE}	VDDcore voltage	1.08	1.2	1.40	V
V_{PLL}	VDDPLL analog voltage	1.08	1.2	1.40	V
V_{DAC}	AVDDA voltage	2.97	3.3	3.63	V
V_{CDC}	AVDCDC voltage	2.7	–	3.6	V
V_{HP}	AVDHP voltage				V
V_{BTL}	AVDBTL voltage				V

Table 3-3 Recommended operating conditions for VDDmem supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{I18}	Input voltage for SSTL18/LPDDR signal	0		1.9	V
V_{O18}	Output voltage for SSTL18/LPDDR signal	0		1.9	V
V_{I25}	Input voltage for SSTL2 signal	0		2.7	V

V_{O25}	Output voltage for SSTL2 signal	0		2.7	V
V_{REFMEM}	Reference voltage supply for SSTL18/SSTL2	0.49	0.5	0.51	V_{MEM}

Table 3-4 Recommended operating conditions for VDDIO supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH5}	Input high voltage with 5V tolerance	1.7		5.5	V
V_{IL5}	Input low voltage with 5V tolerance	-0.3		0.7	V
V_{IH3}	Input high voltage without 5V tolerance	2.0		V_{IO}+0.3	V
V_{IL3}	Input low voltage without 5V tolerance	-0.3		0.8	V

Table 3-5 Recommended operating conditions for VDDIOn supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	V_{ION} * 0.65		V_{ION} + 0.3	V
V_{IL18}	Input low voltage for 1.8V I/O application	-0.3		V_{ION} * 0.35	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7		V_{ION} + 0.3	V
V_{IL25}	Input low voltage for 2.5V I/O application	-0.3		0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2.0		V_{ION} + 0.3	V
V_{IL33}	Input low voltage for 3.3V I/O application	-0.3		0.8	V

Table 3-6 Recommended operating conditions for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IHRTC}	Input high voltage	V_{RTC} * 0.65		V_{RTC} + 0.3	V
V_{ILRTC}	Input low voltage	-0.3		0.7	V

Table 3-7 Recommended operating conditions for USB 2.0 OTG pins

Symbol	Description	Min	Typical	Max	Unit
V_{IVBUS}	Input voltage range VBUS	0		5.25	V
V_{ID}	Input voltage range for all other pins	0		V_{OTG}	V

Table 3-8 Recommended operating conditions for USB 1.1 host DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{IUSB}	Input voltage range for DP/DM pins	0		V_{USB}	V

Table 3-9 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
V_{I-VBAT_IR}	VBAT_IR input voltage range	0		5.5	V
V_{I-VBAT_ER}	VBAT_ER input voltage range	0		2.5	V
V_{IADC}	AUX0/AUX1/XM/XP/YM/YP input voltage range	0		V_{ADC}	V

Table 3-10 Recommended operating conditions for AVDCDC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
$V_{ILH-CDC}$	Input voltage range	0		V_{CDC}	V

Table 3-11 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	0		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-12 DC characteristics for VDDmem supplied pins in LVTTL application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.52	1.66	1.83	V
V_{T+}	Schmitt trig low to high threshold point		1.75	1.90	2.08	V
V_{T-}	Schmitt trig high to low threshold point		1.25	1.37	1.52	V
I_L	Input Leakage Current				±10	μA
I_{OZ-IO}	Tri-State output leakage current				±10	μA
R_{PU}	Pull-up Resistor		35	50	70	kΩ
R_{PD}	Pull-down Resistor		68	140	230	kΩ
V_{OL-IO}	Output low voltage @I_{OL-IO}=12, 16, 24, 30mA				0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=12, 16, 24, 30mA		2.4			V
I_{OL-IO}	Low level output current @ V_{OL-IO} = 0.4V for cells of	12mA	13.2	20.5	27.3	mA
		16mA	17.6	27.3	36.5	mA
		24mA	24.3	37.7	50.2	mA
		30mA	30.8	47.8	63.8	mA
I_{OH-IO}	High level output current	12mA	17.9	36.5	60.3	mA

	@ V_{OH-IO} = 2.4V for cells of	16mA	23.9	48.6	80.3	mA
		24mA	32.9	66.9	110.5	mA
		30mA	41.8	85.1	140.6	mA

Table 3-13 DC characteristics for VDDIO supplied pins with 5V tolerance

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.30	1.41	1.53	V
V_{T+}	Schmitt trig low to high threshold point		1.53	1.64	1.73	V
V_{T-}	Schmitt trig high to low threshold point		0.95	1.02	1.09	V
I_L	Input Leakage Current				±1	μA
I_{OZ-IO}	Tri-State output leakage current				±1	μA
R_{PU}	Pull-up Resistor		62	77	112	kΩ
R_{PD}	Pull-down Resistor		48	85	174	kΩ
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4mA				0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4mA		2.4			V
I_{OL-IO}	Low level output current	2mA	2.2	3.5	4.2	mA
	@ V_{OL-IO} = 0.4V for cells of	4mA	4.4	6.9	8.4	mA
I_{OH-IO}	High level output current	2mA	2.8	5.8	9.2	mA
	@ V_{OH-IO} = 2.4V for cells of	4mA	5.5	11.6	18.3	mA

Table 3-14 DC characteristics for VDDIO supplied pins with programmable driven strength

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point		1.65		V
V_{T+}	Schmitt trig low to high threshold point	1.70		1.96	V
V_{T-}	Schmitt trig high to low threshold point	0.87		1.11	V
I_L	Input Leakage Current			±10	μA
I_{OZ-IO}	Tri-State output leakage current			±10	μA
R_{PU}	Pull-up Resistor	53	66	120	kΩ
R_{PD}	Pull-down Resistor	37	50	120	kΩ
V_{OL-IO}	Output low voltage @I_{OL-IO}=2~24mA			0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2~24mA	2.4			V

Table 3-15 DC characteristics for VDDIO supplied other pins

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.30	1.41	1.53	V
V_{T+}	Schmitt trig low to high threshold point	1.54	1.65	1.74	V
V_{T-}	Schmitt trig high to low threshold point	0.95	1.02	1.09	V
I_L	Input Leakage Current			±1	μA
I_{OZ-IO}	Tri-State output leakage current			±1	μA

R_{PU}	Pull-up Resistor		62	77	112	kΩ
R_{PD}	Pull-down Resistor		58	81	156	kΩ
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4, 8, 12mA				0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4, 8, 12mA		2.4			V
I_{OL-IO}	Low level output current	2mA	2.1	3.3	4.1	mA
	@ V_{OL-IO} = 0.4V for cells of	4mA	4.2	6.6	8.1	mA
I_{OH-IO}	High level output current	2mA	2.4	4.8	7.5	mA
	@ V_{OH-IO} = 2.4V for cells of	4mA	4.7	9.6	14.9	mA

Table 3-16 DC characteristics for VDDIOn supplied pins for 1.8V I/O application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		0.76	0.82	0.87	V
I_L	Input Leakage Current				±1	μA
I_{OZ-IO}	Tri-State output leakage current				±1	μA
R_{PU}	Pull-up Resistor		123	174	276	kΩ
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4mA				0.45	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4mA		V_{IO} - 0.45			V
I_{OL-IO}	Low level output current	2mA	1.0	1.8	2.6	mA
	@ V_{OL-IO} = 0.45V for cells of	4mA	2.0	3.7	5.3	mA
I_{OH-IO}	High level output current	2mA	0.9	1.5	2.1	mA
	@ V_{OH-IO} = VDD_{IO} - 0.45V for cells of	4mA	1.8	3.0	4.2	mA

Table 3-17 DC characteristics for VDDIOn supplied pins for 2.5V I/O application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.01	1.08	1.17	V
I_L	Input Leakage Current				±1	μA
I_{OZ-IO}	Tri-State output leakage current				±1	μA
R_{PU}	Pull-up Resistor		74	105	177	kΩ
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4mA				0.5	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4mA		1.8			V
I_{OL-IO}	Low level output current	2mA	1.7	3.1	4.1	mA
	@ V_{OL-IO} = 0.5V for cells of	4mA	3.5	6.0	8.0	mA
I_{OH-IO}	High level output current	2mA	1.4	3.1	5.2	mA
	@ V_{OH-IO} = 1.8V for cells of	4mA	2.8	6.2	10.4	mA

Table 3-18 DC characteristics for VDDIOn supplied pins for 3.3V I/O application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.30	1.41	1.53	V
I_L	Input Leakage Current			±1	μA

I_{OZ-IO}	Tri-State output leakage current				±1	μA
R_{PU}	Pull-up Resistor		62	77	112	kΩ
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4mA				0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4mA		2.4			V
I_{OL-IO}	Low level output current	2mA	2.1	3.3	4.1	mA
	@ V_{OL-IO} = 0.4V for cells of	4mA	4.2	6.6	8.1	mA
I_{OH-IO}	High level output current	2mA	2.4	4.8	7.5	mA
	@ V_{OH-IO} = 2.4V for cells of	4mA	4.7	9.6	14.9	mA

Table 3-19 DC characteristics for VDDRTC？ supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	0.76	0.82	0.87	V
V_{T+}	Schmitt trig low to high threshold point	0.94	1.04	1.08	V
V_{T-}	Schmitt trig high to low threshold point	0.55	0.59	0.62	V
I_L	Input Leakage Current			±1	μA
I_{OZ-IO}	Tri-State output leakage current			±1	μA
R_{PD}	Pull-down Resistor	126	202	416	kΩ
V_{OL-IO}	Output low voltage @I_{OL-IO} = 2, 4mA			0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO} = 2, 4mA	2.4			V
I_{OL-IO}	Low level output current @ V_{OL-IO} = 0.45V	1.0	1.9	2.6	mA
I_{OH-IO}	High level output current @ V_{OH-IO} = VDDRTC- 0.45V	1.0	1.8	2.5	mA

Table 3-20 DC characteristics for AVDUSB supplied pins

Symbol	Description	Min	Typical	Max	Unit
V_{O-USB}	Output voltage range	0		V_{USB}	V
V_{DIS}	Differential input sensitivity	0.2			V
V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single ended receiver threshold	0.8		2.0	V
I_{OZ-USB}	Tri-State leakage current			±10	μA
Z_{DRV}	Driver output resistance, including damping resistor	24		44	Ω
V_{OL-USB}	Static output low voltage			0.3	V
V_{OH-USB}	Static output high voltage	2.8			V

3.4 Audio codec electronic characteristics

3.4.1 Line input to audio ADC path

Measurement conditions: T = 25°C, AVDCDC = AVDHP = VREFP = 3.3V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GIDL, GIDR = 0dB (note 1)	2.49	2.8	3.15	Vpp
Input resistance		20			kOhm
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF

NOTE: The Full Scale input voltage scales with AVDCDC, equals to 0.85*VREF (typ).

3.4.2 Microphone input to audio ADC path

Measurement conditions: T = 25°C, AVDCDC = AVDHP = VREFP = 3.3V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GIDL, GIDR = 0dB, boost gain GIM1, GIM2 = 20dB (note 1)	0.249	0.28	0.315	Vpp
Input resistance	Boost gain GIM1,GIM2 = 0 dB	66	83	100	kOhm
	Boost gain GIM1,GIM2 = 20 dB	10	12.5	15	
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF

NOTE: The Full Scale input voltage scales with AVDCDC, equals to 0.085*VREF (typ).

3.4.3 Audio DAC to headphone output path

Measurement conditions: T = 25°C, AVDCDC = AVDHP = VREFP = 2.7V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96 kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
DAC playback on 16 Ohm HeadPhone					
Output level	Full Scale, Gain GOL, GOR = -6 dB, GODL, GODR=0dB	1	1.15	1.29	Vpp
Maximum output power	Rl = 16 Ohm		10		mW
Output resistance	R1	16			Ohm
Output bypass capacitor	Cl (Rl = 16 Ohm)			220	uF
DAC playback to 10k Ohms lineout single					
Output level	Full Scale, Gain GOL, GOR = 0 dB, GODL, GODR=0dB (note 1)	2.03	2.29	2.58	Vpp
Output resistance	R1	10k			Ohm
Output bypass capacitor	Cl (Rl = 10 kOhm)			1	uF
Common characteristics					
Output capacitance (note 2)	Cp			200	pF

NOTES:

1 The Full Scale output voltage scales with AVDCDC, equals to 0.85*VREF. The minimum and maximum output levels are given with gain accuracy.

2 Output may oscillate above specified load capacitances. The capacitance is equivalent to a 2-meter cable.

3.4.4 Audio DAC to mono line output path

Measurement conditions: T = 25°C, AVDCDC = AVDHP = AVDBTL = VREFP = 3.3V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96 kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Output level	Full Scale, Gain GODL, GODR = 0dB (note 1)	5	5.6	6.3	Vpp
Output resistance		10			kOhm
Output capacitance	Cp			100	pF

Output bypass capacitor	Cl (Rl = 10 kOhm)			1	uF

NOTE: The Full Scale output voltage scales with AVDCDC, equals to 1.7*VREF (typ).

3.4.5 Line input to headphone output path (analog bypass)

Measurement conditions: T = 25°C, AVDCDC = AVDHP = VREFP = 2.7V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96 kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale	2.03	2.29	2.58	Vpp
Input resistance		10			kOhm
bypass on 16 Ohm HeadPhone					
Output level	Full Scale, Gain GOL, GOR = -6 dB, GIL, GIR=0 dB	1	1.15	1.29	Vpp
Output resistance	R1	16			Ohm
bypass to 10k Ohms lineout single					
Output level	Full Scale, Gain GOL, GOR = 0 dB, GIL, GIR=0 dB (note 1)	2.03	2.29	2.58	Vpp
Common characteristics					
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF

NOTE: The Full Scale output voltage scales with AVDCDC, equals to 1.7*VREF (typ).

3.4.6 Microphone input to headphone output path (analog sidetone)

Measurement conditions: T = 25°C, AVDCDC = AVDHP = VREFP = 3.3V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs =8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GOL, GOR = 0dB, boost gain GIM1,GIM2 = 20dB (note 1)	0.249	0.28	0.315	Vpp
Output level	Full Scale, Gain GOL,GOR= 0dB, boost gain GIM1,GIM2 = 0 to 20dB, 10kOhm load (note 2)	2.49	2.8	3.15	Vpp

NOTES:

1 The Full Scale input voltage scales with AVDCDC, equals to 0.085*VREF (typ).

2 The Full Scale output voltage scales with AVDCDC, equals to 0.85*VREF (typ).

3.4.7 Micbias and reference

Measurement conditions: T = 25°C, AVDCDC = AVDHP = VREFP = 3.3V, input sine wave with a frequency of 1kHz, Fmclk = 12MHz, Fs = 8 to 96kHz, measurement bandwidth 20Hz – 20kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Micbias output level	(note 1)		2.75		V
Micbias output current				4	mA
Micbias decoupling capacitor	Cmic	0.75	1	1.25	nF
VCAP voltage	(note 2)		2.64		V

NOTES:

1 Micbias output voltage scales with AVDCDC, equals to 5/6*VREF (typ).

2 VCAP output voltage scales with AVDCDC, equals to 0.8*VREF (typ).

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the JZ4760B processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-21 gives the timing parameters. Following are the name of the power.

- VDDRTC
- VDDRTC12
- AVDAUD: AVDCDC, AVDHP
- VDD33: all other digital 3.3V or DDR power supplies, include VDDMEM, VDDIO, VDDIOn
- AVD33: all other analog 3.3V power supplies, include AVDAD, AVDDA, AVDOTG, AVDUSB, AVDBTL
- VDD12: all 1.2V power supplies, include VDDCORE, VDDPLL
- VPEFUSE

Table 3-21 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDDRTC}	VDDRTC rise time[1]	0	5	ms
$t_{R\_VDDRTC12}$	VDDRTC12 rise time[1]	0	5	ms
t_{D_RTC-12}	Delay between VDDRTC arriving 50% (or 90%) to VDDRTC12 arriving 50% (or 90%)	0	1	ms
t_{R_VDD33}	VDD33 rise time[1]	0	5	ms
t_{D_VDD33}	Delay between VDDRTC arriving 50% (or 90%) to VDD33 arriving 50% (or 90%)	0	–	ms
t_{R_VDD12}	VDD12 rise time[1]	0	5	ms
t_{D_33-12}	Delay between VDD33 arriving 50% (or 90%) to VDD12 arriving 50% (or 90%)	0	1	ms
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms
t_{D_AVDAUD}	Delay between VDD12 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%)	0.01	1	ms
t_{R_AVD33}	AVD33 rise time[1]	0	5	ms
t_{D_AVDA33}	Delay between VDD33 arriving 50% to AVD33 arriving 50%	-1	1	ms
$t_{D\_PPRST\_}$	Delay between VDDAUD stable and PPRST_ deasserted	0	–	ms[2]
$t_{D\_VPEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

1 The power rise time is defined as 10% to 90%.

2 The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

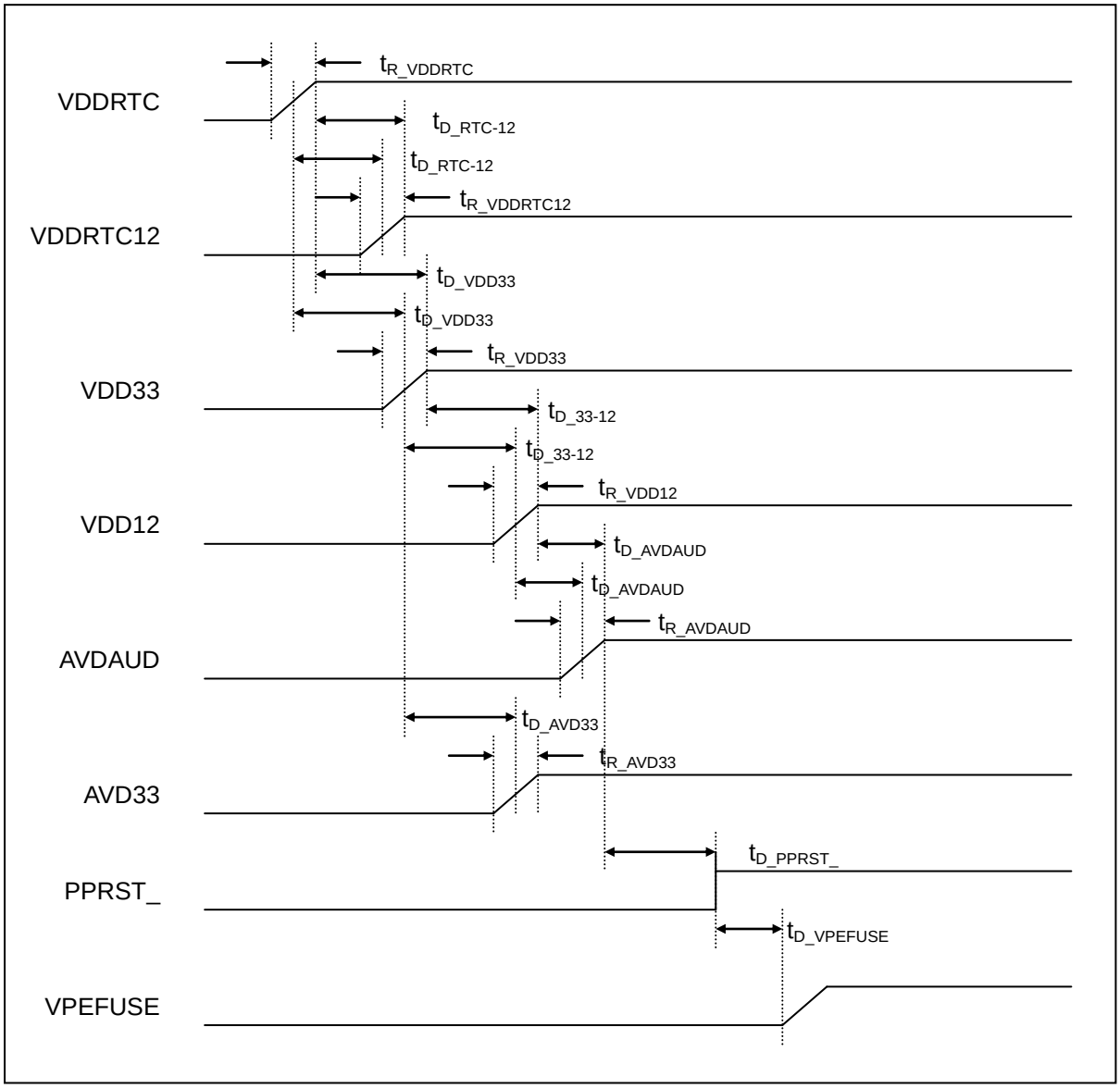


Figure 3-1 Power-On Timing Diagram

3.5.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.

This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see "2.5Pin Description [1][2]" for details. The PWRON is output 1. The oscillators are on. The USB 2.0 OTG PHY and USB 1.1 PHY, the audio CODEC DAC/ADC, the SAR-ADCs and the video DAC are put in suspend mode.

3.5.3 BOOT

JZ4760B supports 5 different boot sources depending on BOOT_SEL0, BOOT_SEL1 and BOOT_SEL2 pins values. Table 3-22 lists them.

Table 3-22 Boot from 3 boot sources

BOOT_SEL2	BOOT_SEL1	BOOT_SEL0	Boot From
1	1	1	NAND flash at CS1
1	0	0	SD card: MSC0
1	0	1	SPI: SPI0/CE0
0	1	1	NOR flash at CS4
1	1	0	USB2.0 OTG as device with EXCLK = 12MHz
0	0	0	USB2.0 OTG as device with EXCLK = 13MHz
0	0	1	USB2.0 OTG as device with EXCLK = 26MHz
0	1	0	USB2.0 OTG as device with EXCLK = 19.2MHz

The boot procedure is showed in the following flow chart:

- In case of NAND/SDcard/SPI boot, if it fails, enter USB-12MHz boot.
- In case of USB boot, if it cannot connect to USB host within 10 seconds, restart the boot procedure.
- In case of NOR boot, if it fails, restart the boot procedure.
- If the boot procedure has been repeated more than 10 times, enter hibernating mode.