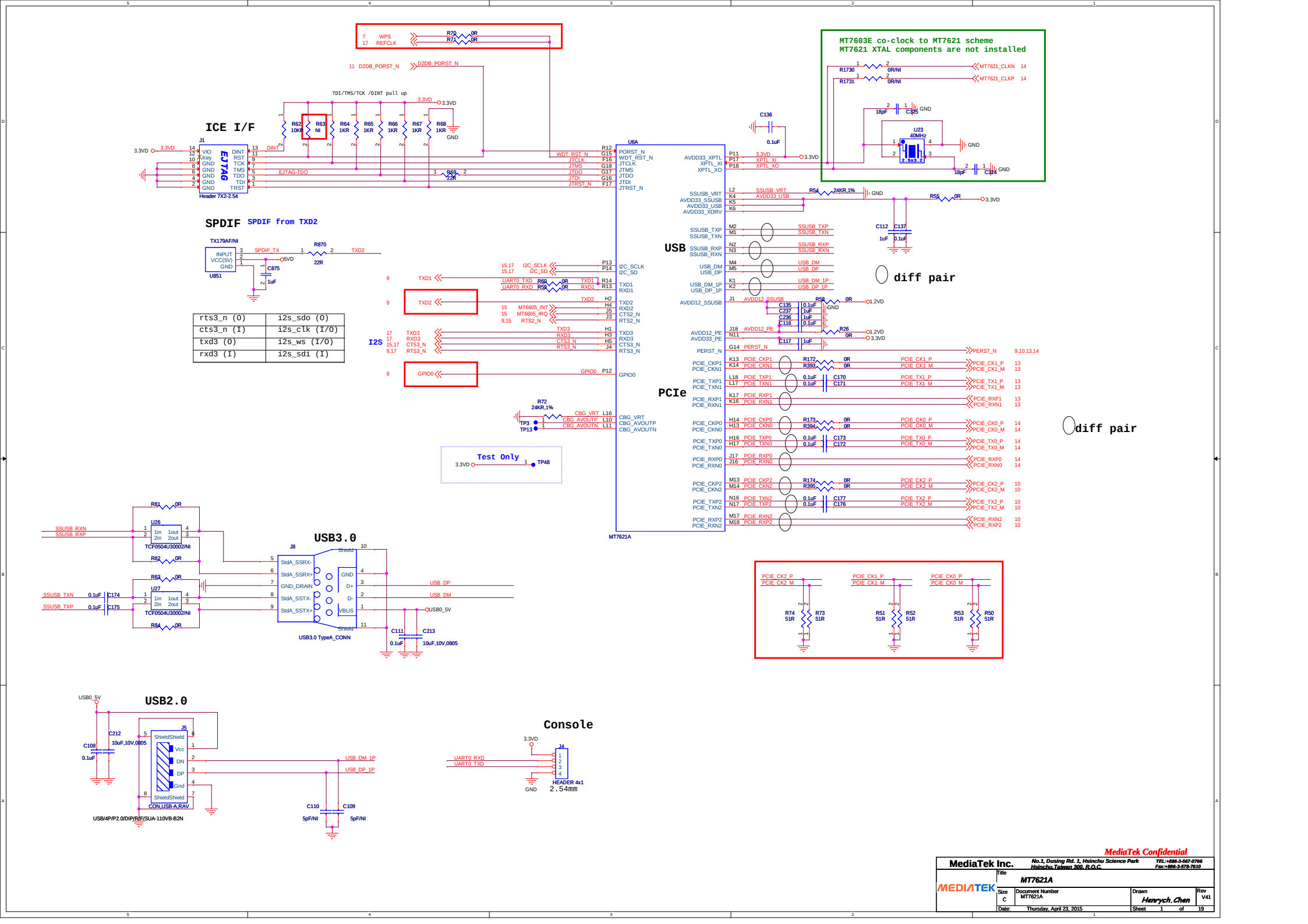

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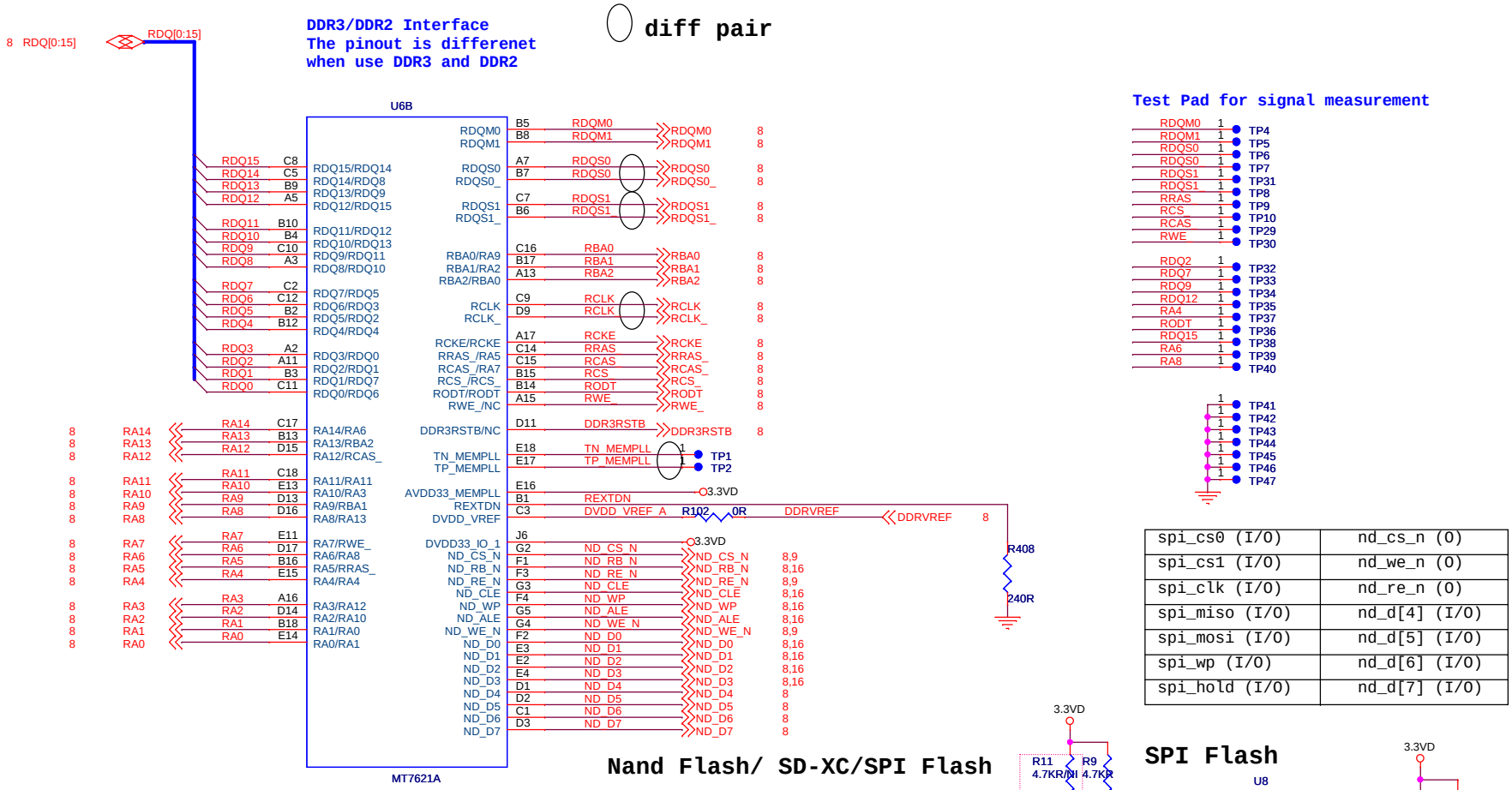

spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)

sd_wp (I)	nd_wp (O)
sd_clk (I/O)	nd_rb_n (I)
sd_cd (I)	nd_cle (O)
sd_cmd (I/O)	nd_ale (O)
sd_data[0] (I/O)	nd_d[0] (I/O)
sd_data[1] (I/O)	nd_d[1] (I/O)
sd_data[2] (I/O)	nd_d[2] (I/O)
sd_data[3] (I/O)	nd_d[3] (I/O)

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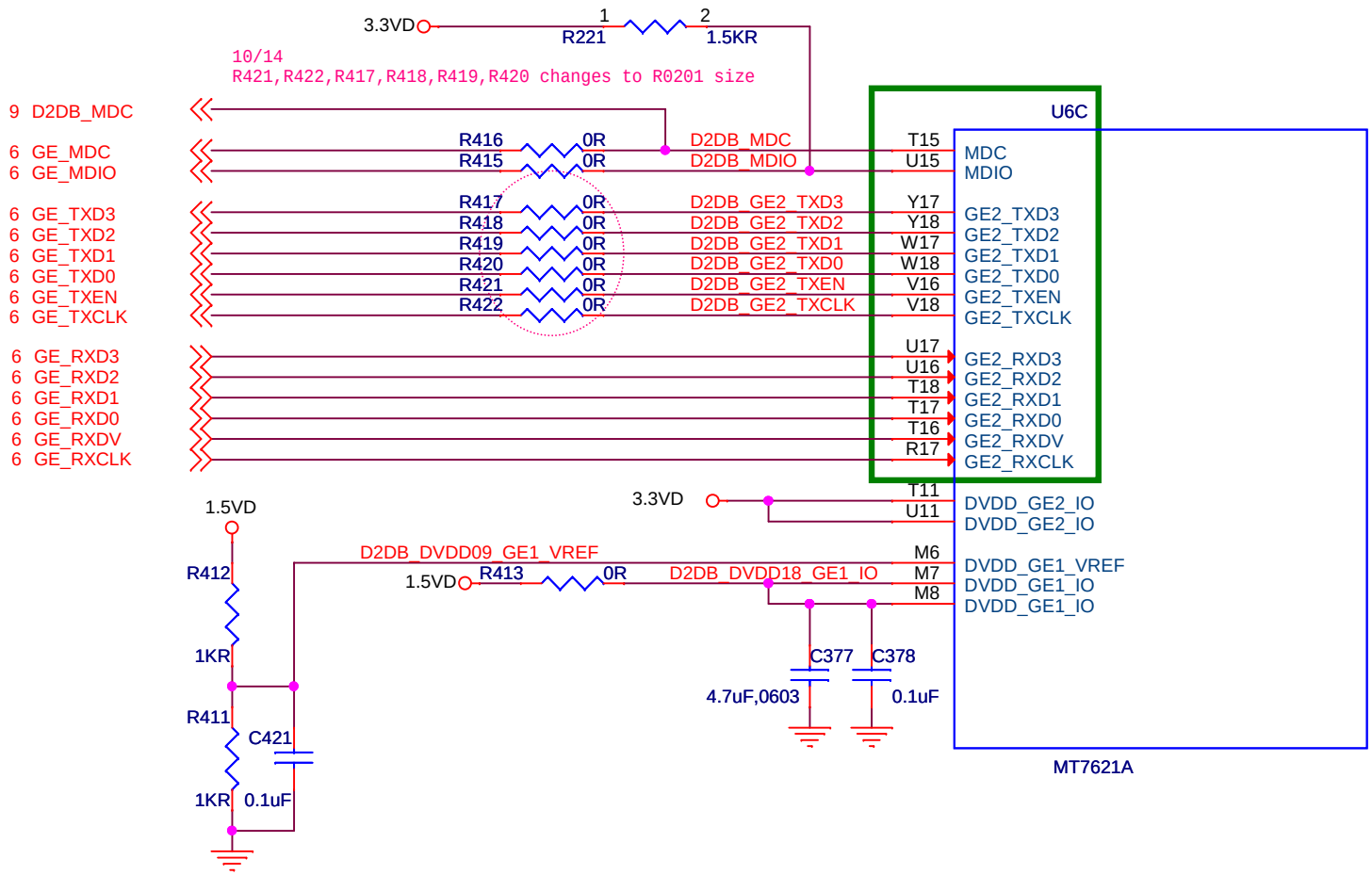
RGMII Interface



Note:
1. MT7621A/S MDC/MDIO cannot use to GPIO when needs control external/internal PHY
2. GE2 group cannot use to GPIO when WAN/LAN total bandwidth is up to 2G. Keeps the pin floating.

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MEDIATEK	Title: MT7621A		
Size: A	Document Number: MT7621A	Drawn: Henrych.Chen	Rev: V41
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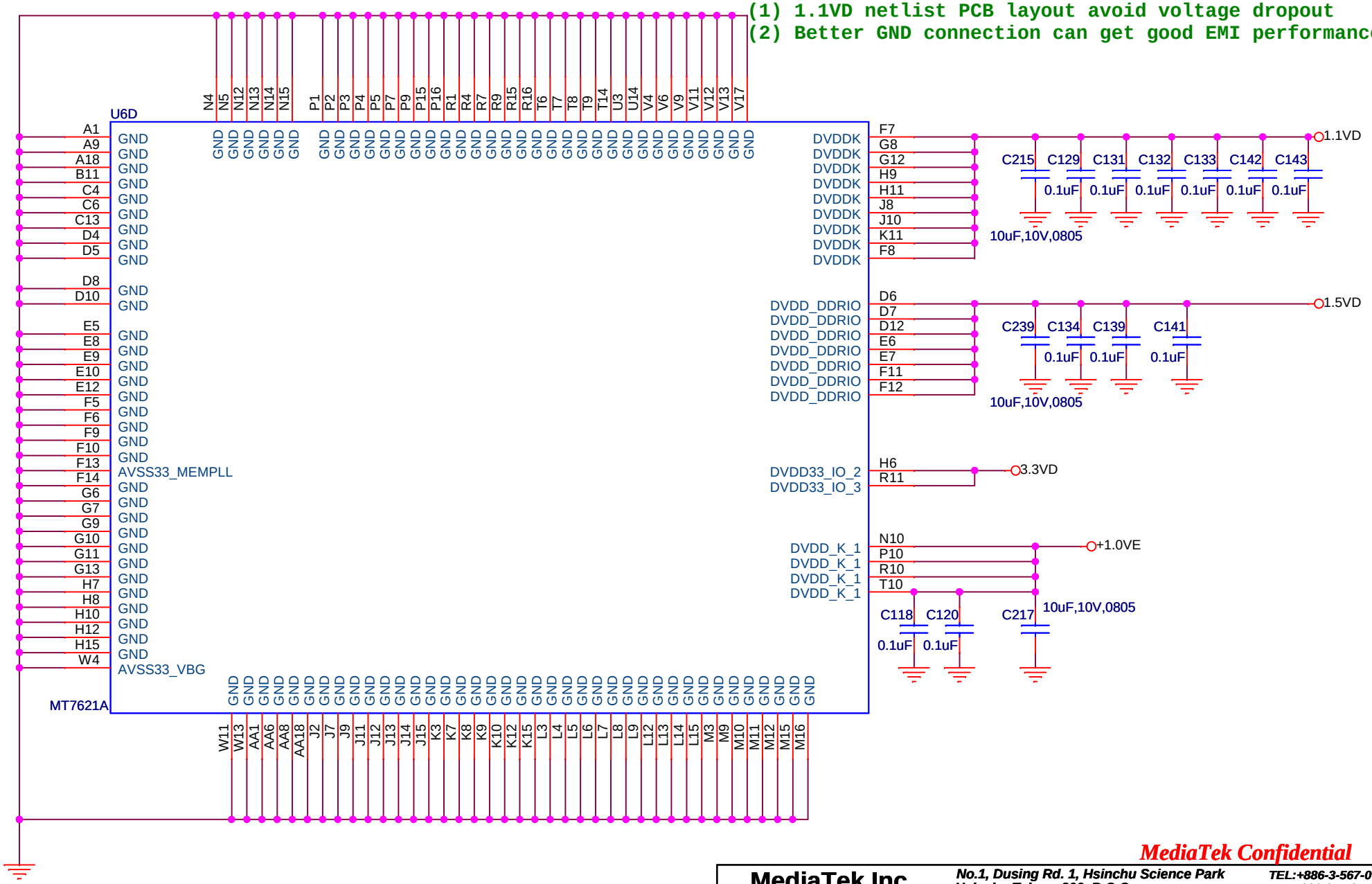
MT7621 Power

Please notice
Power and GND PCB layout is very important
(1) 1.1VD netlist PCB layout avoid voltage dropout
(2) Better GND connection can get good EMI performance



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Size: A	Document Number: MT7621A	Drawn: *Henrych.chen*	Rev: V41
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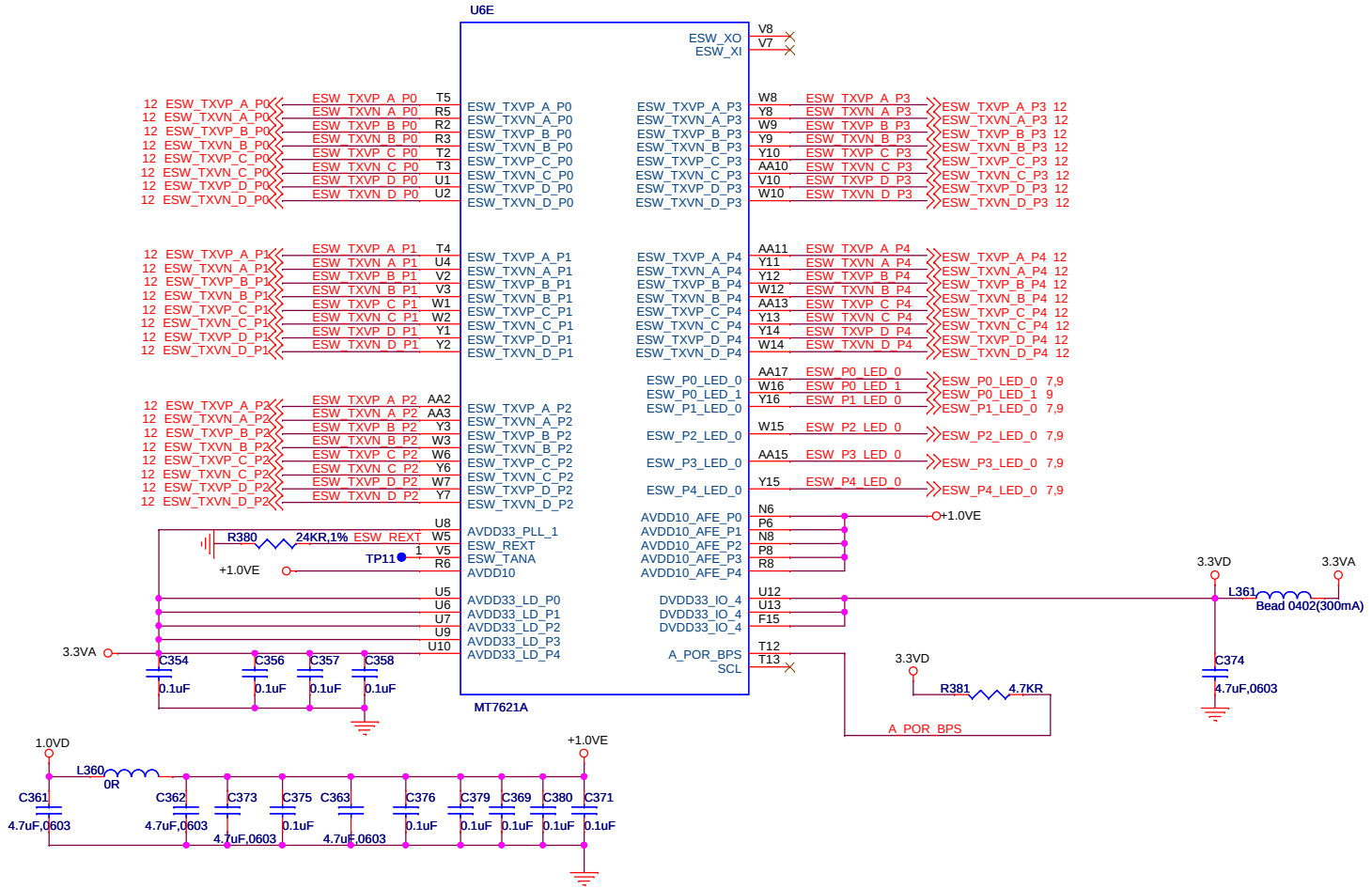
Giga SW



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	Size: B	Document Number: MT7621A	Drawn: Henrych.chen / Rev: V41
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Giga Phy

Close to IP1001

3.3V to 1.2V

3.3V to 2.1V

PHY address setting 00101b

Select either pull-high resistor or pull-low resistor for Tx/Rx phase delay.
Reserve these resistors on PCB for phase adjustment.
RXCLK output delay 2ns in 1000Base-T
TXCLK input delay 0ns in 1000Base-T

Pull low for RGMII interface
Pull high for GMII/MII interface

LED Mode 0

Closed to X'FML

2.5V or 2.1V (Use 2.1V)

Transformer :
FUN-JIN->GT24-03S,GT24-03SM
Pulse->H5004, H5007, H5062, H5091NL
Bothhand->24HST1041A-2,GST5009

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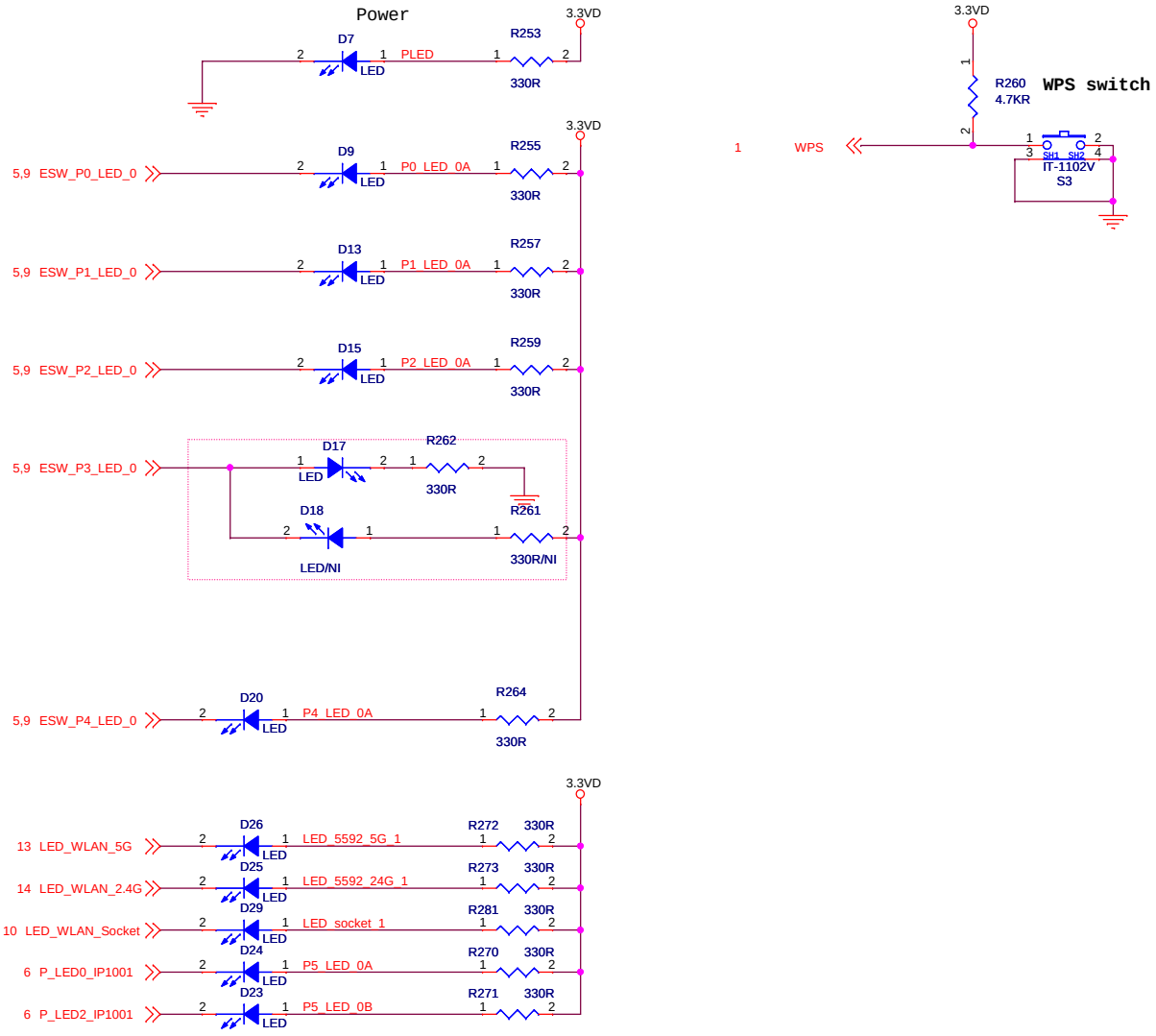
LED



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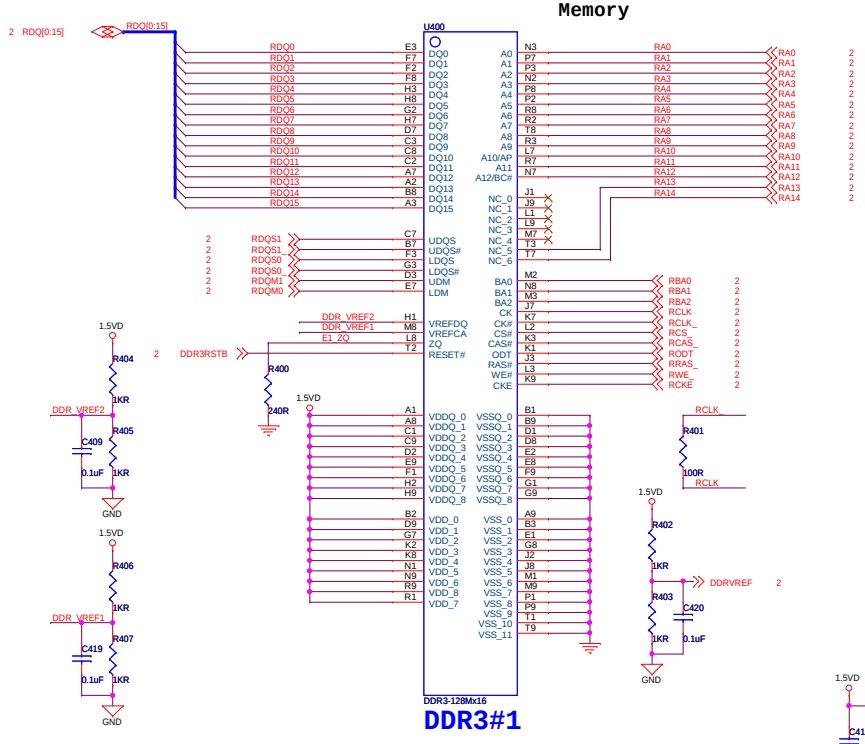
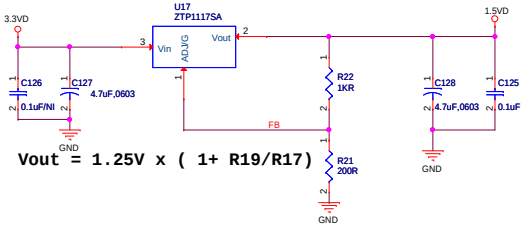
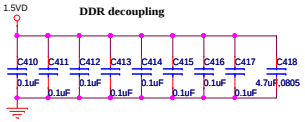
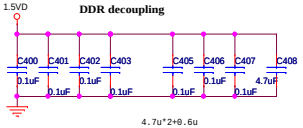
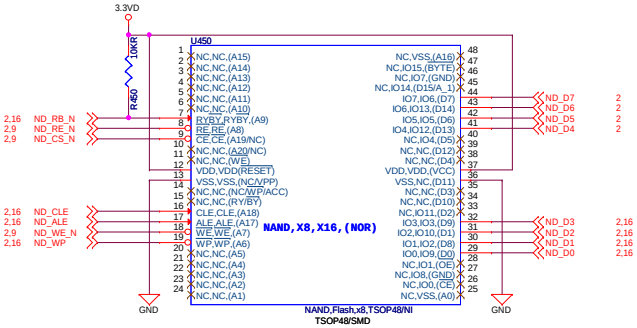
Memory

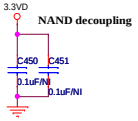












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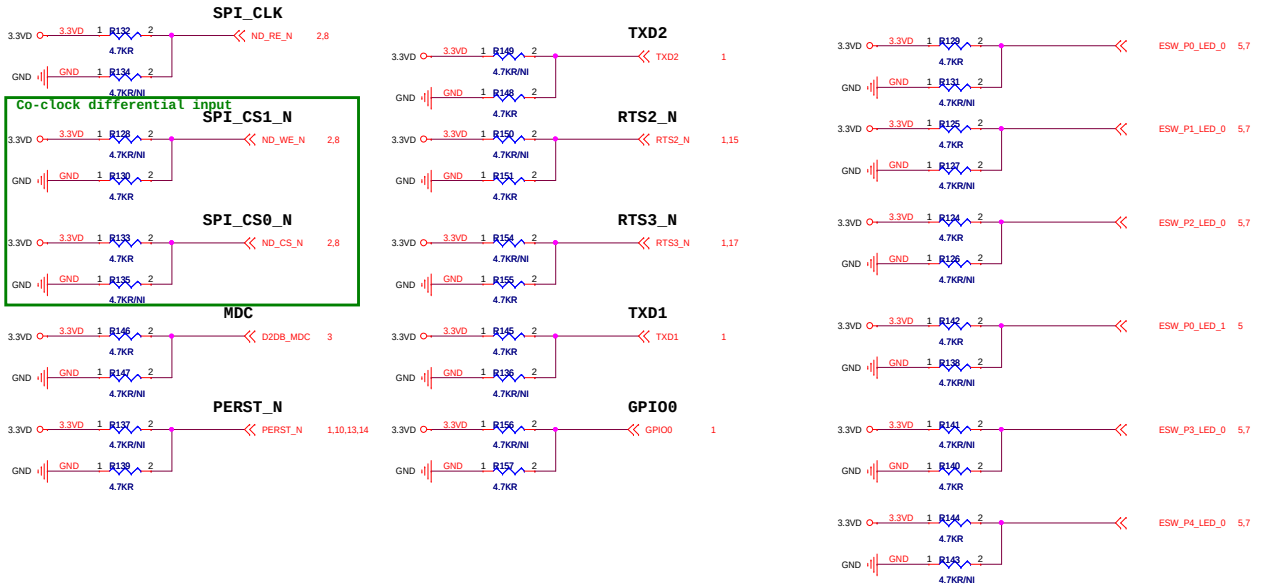
Boot Strapping

Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	**011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input **101: 40 MHz, differential input** 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) **0010: Normal / Boot from SPI 3-byte address** 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

Giga Switch Hardware Trap

Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		



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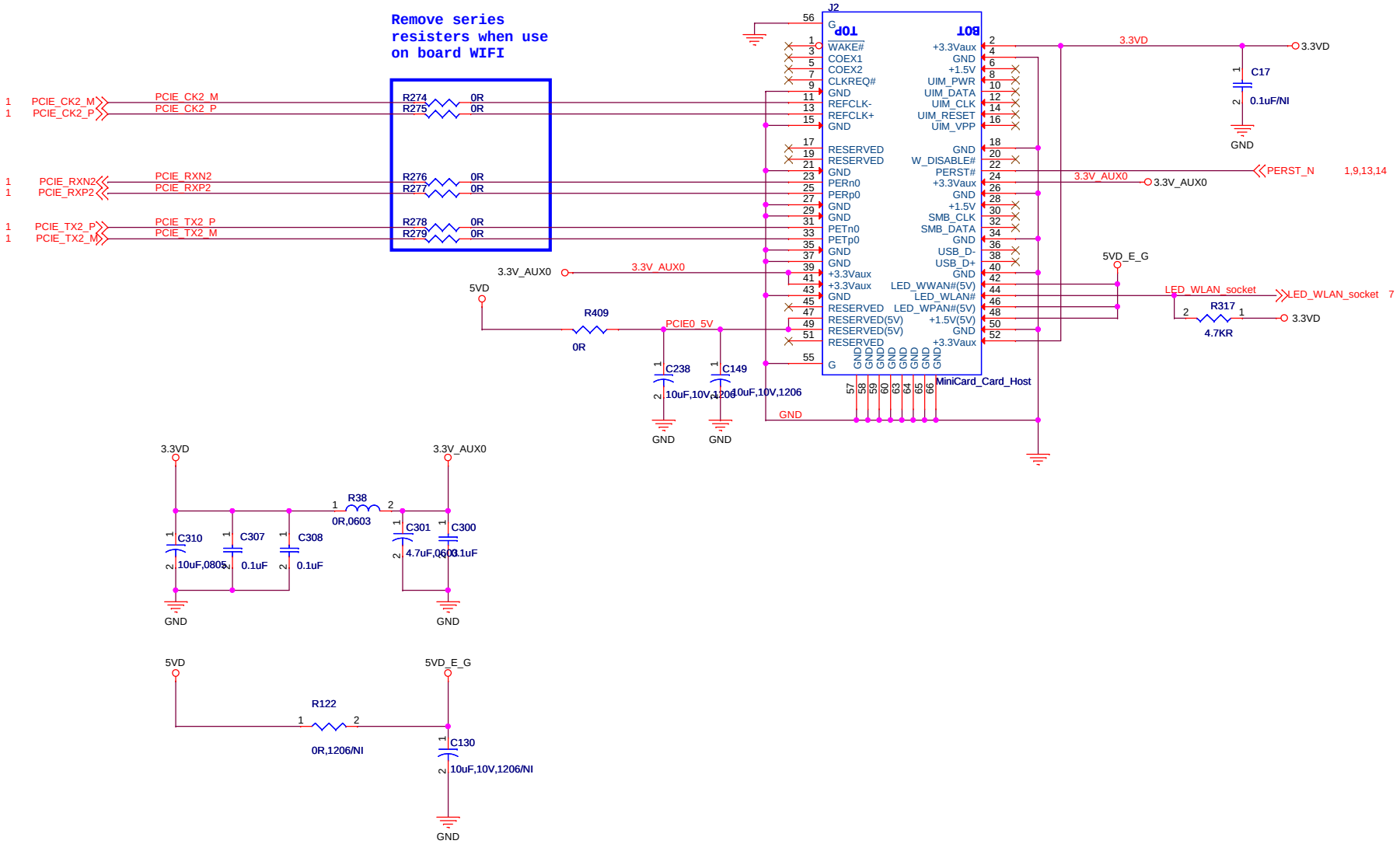
PCIe Slot #2



Reserve pin 42, 46, 47, 48, 49 for 5V input

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MEDIATEK	Title: MT7621A		
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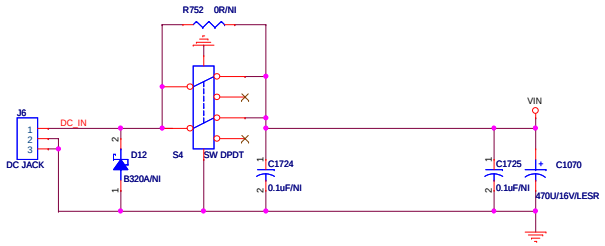
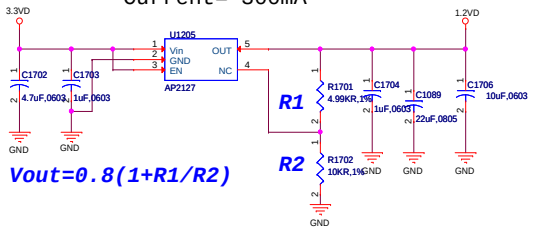
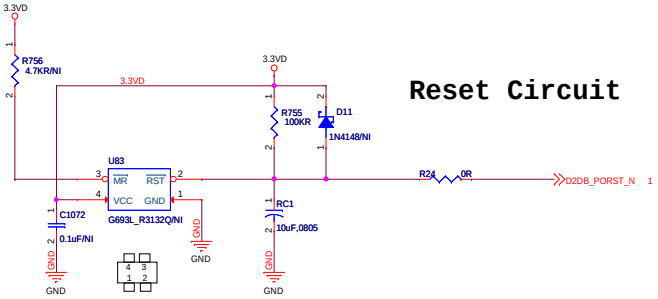
System Power



For USB/PCIe PHY Power (1.2V)
Current= 300mA

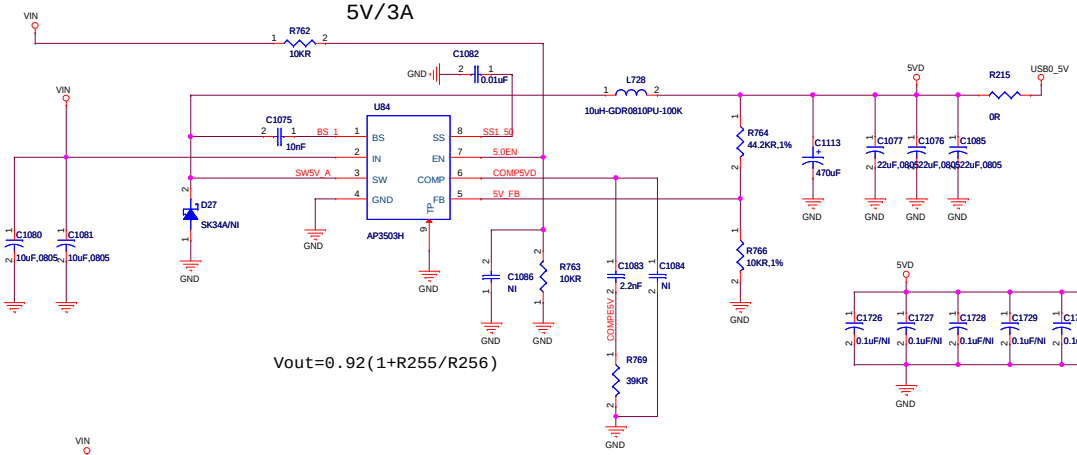


Vout=0.8(1+R1/R2)



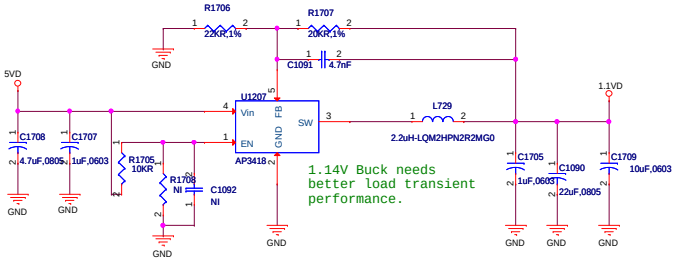
Reset Circuit

5V/3A

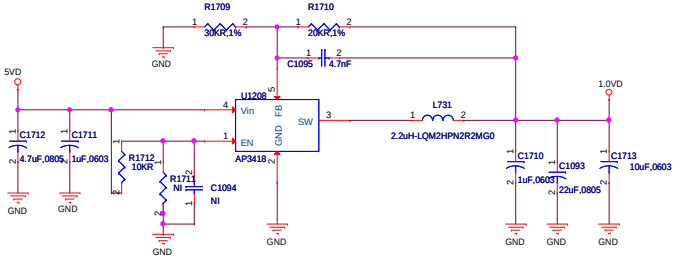


Vout=0.92(1+R255/R256)

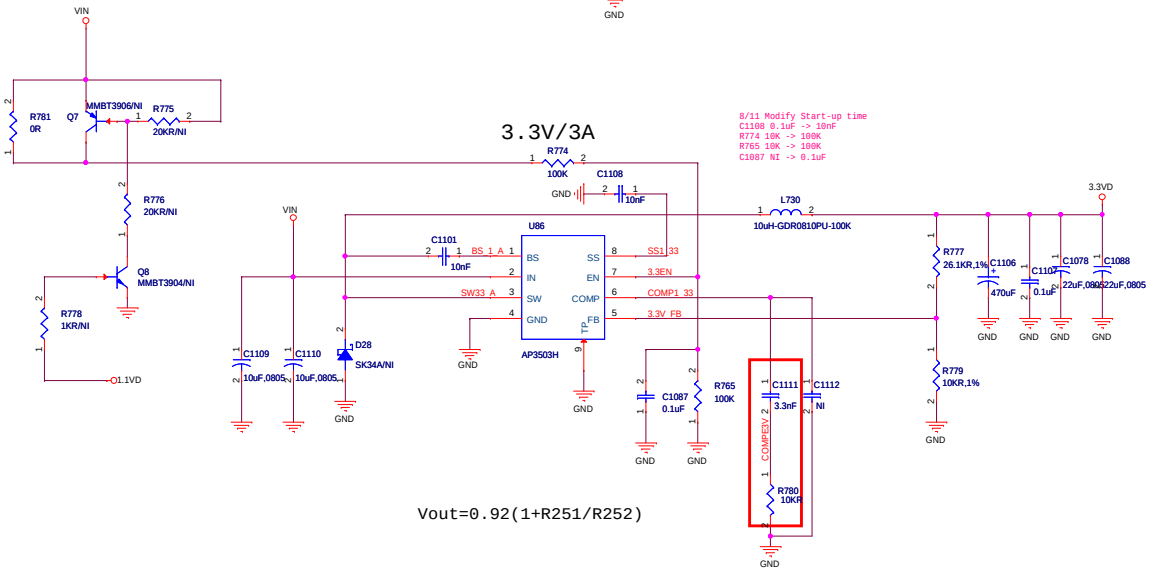
1.14V/1.5A



1.0V/1.5A



3.3V/3A



8/11 Modify Start-up time
C1108 0.1uF -> 10nF
R774 10K -> 100K
R765 10K -> 100K
C1087 NI -> 0.1uF

Vout=0.92(1+R251/R252)

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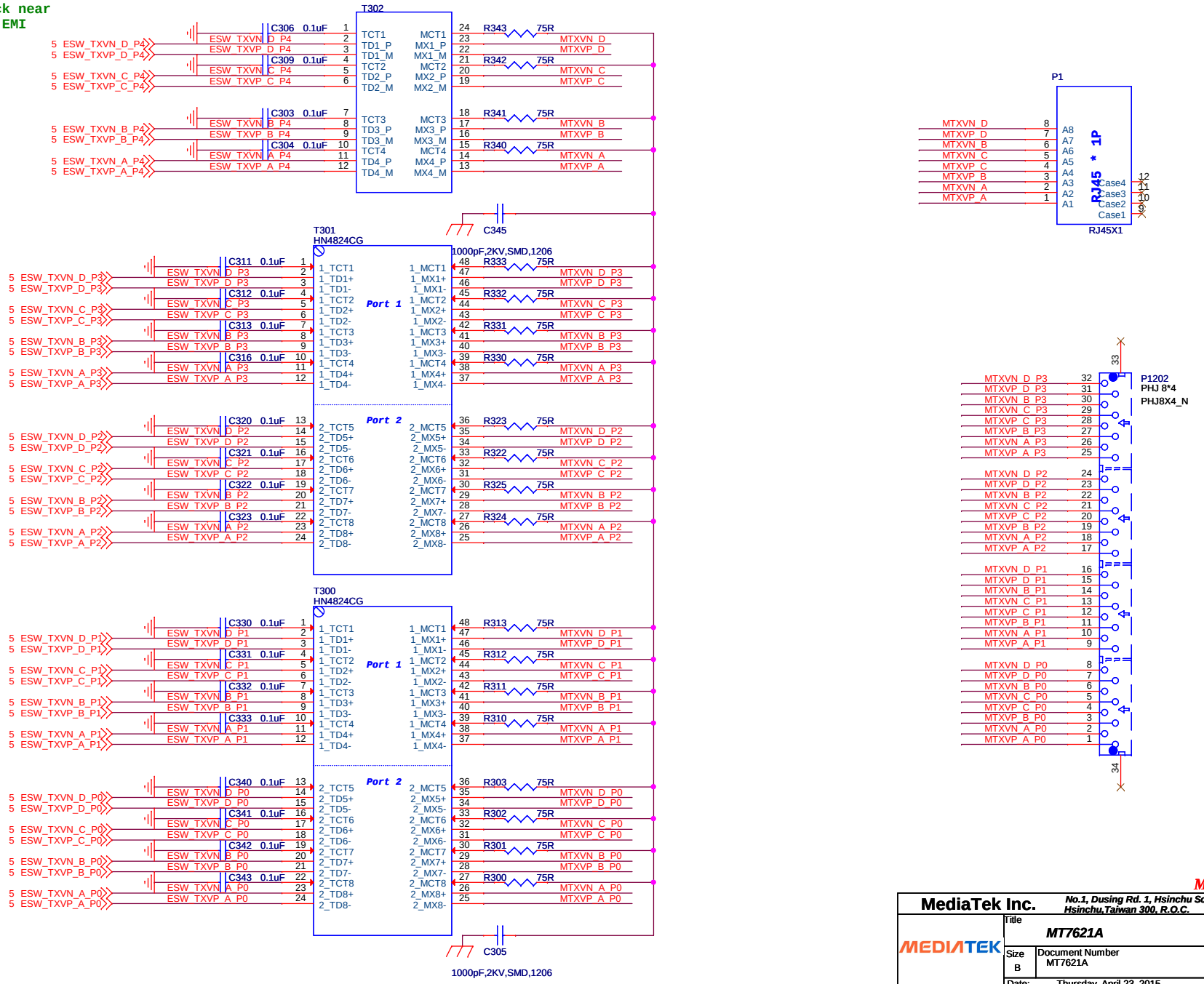
XMER choose common chock near
MT7621 side for better EMI



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RF port is more sensitive to ESD for advanced silicon process.
The design of ESD protection must take into consideration since sample pilot run stage.
For detail, please contact with MTK technical contact window.

Place DC block capacitor near MT7612 RX pin. (red circle 1)

* If FEM has DC-block-capacitor inside design, system could use FEM component as ESD discharging path directly. For example, use C207,C242 0R instead of 10pF in SKY85601 case.(red circle 2)

* Place MT7612E , DC block capacitor and FEM insides shielding case to avoid human touching.

Placement Note
C85 and C88 DC coupling capacitor should place in shielding case, and near MT7612E pin out

WF0_RF_5G_TRX

WF0_RF_5G_RX_AUXIN

WF1_RF_5G_RX_AUXIN

WF1_RF_5G_TRX

Please check part number in BOM list

MT7612E

WIFI先暫放0.47uF 0402 電容,但會視PCB空間退縮成0.1uF 0201電容.

1.6V Buck Output (800 mA)

Internal LDO Input (1.6V轉1.2V)

Internal 1.2V LDO Output

5G External SW/LNA Circuit (WF0)

5G External SW/LNA Circuit (WF1)

Boot Strapping (Internal Pull High/Low)

EE_CLK	0 : 40MHz Xtal (default) 1 : 20MHz Xtal
MOSI	0 : E-Fuse (default) 1 : EEPROM
GPIO [14:12]	Chip mode [2:0] => GPIO [14:12] 001:Boot from ROM (default)

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Size	Document Number: MT7621A	Drawn: Jimmy	Rev: V01
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	Normal Mode	Test Mode
0: Normal Mode 1: Test Mode	TEST_MODE R1719 1K/NI GND	
0: EFUSE 1: EEPROM	3V3 ANTSEL6 R1720 1K/NI R1721 1K GND	
00: 20MHz SMD 01: 20MHz DIP 10: 25MHz DIP 11: 40MHz SMD	3V3 ANTSEL4 XTAL_SEL0 R1722 1K R1723 1K/NI GND 3V3 ANTSEL5 XTAL_SEL1 R1724 1K R1725 1K/NI GND	
Co-clock mode 0: Current Mode 1: Voltage Mode Set current mode to MT7621	3V3 GPIO0_03 R1726 1K/NI R1727 1K GND	

Default : Co-Clock Mode from MT7612E

Please check part number in BOM list

MT7603E

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Title: MT7603E iPA/iLNA			
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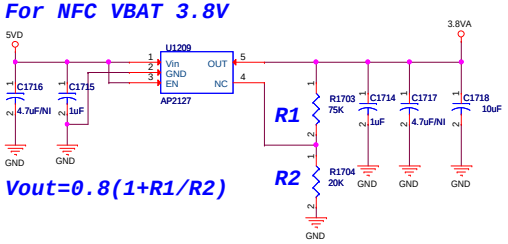
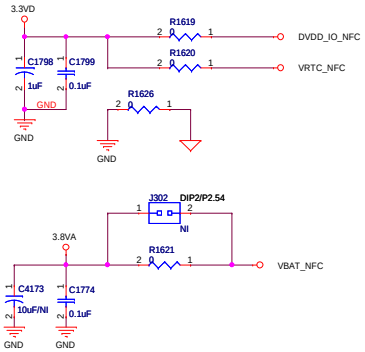
5/20 Change NFC power plan

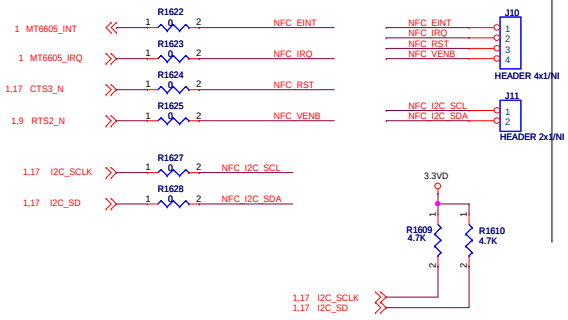
For NFC VBAT 3.8V

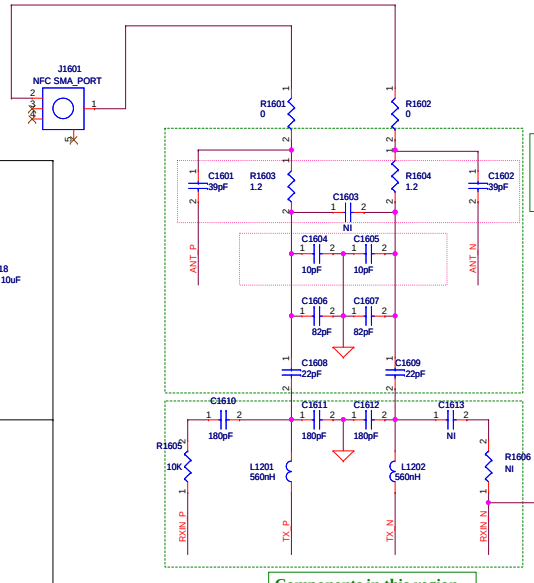


Vout=0.8(1+R1/R2)

For DVDD_IO_NFC(3.3V)
For VRTC Power (3.3V)







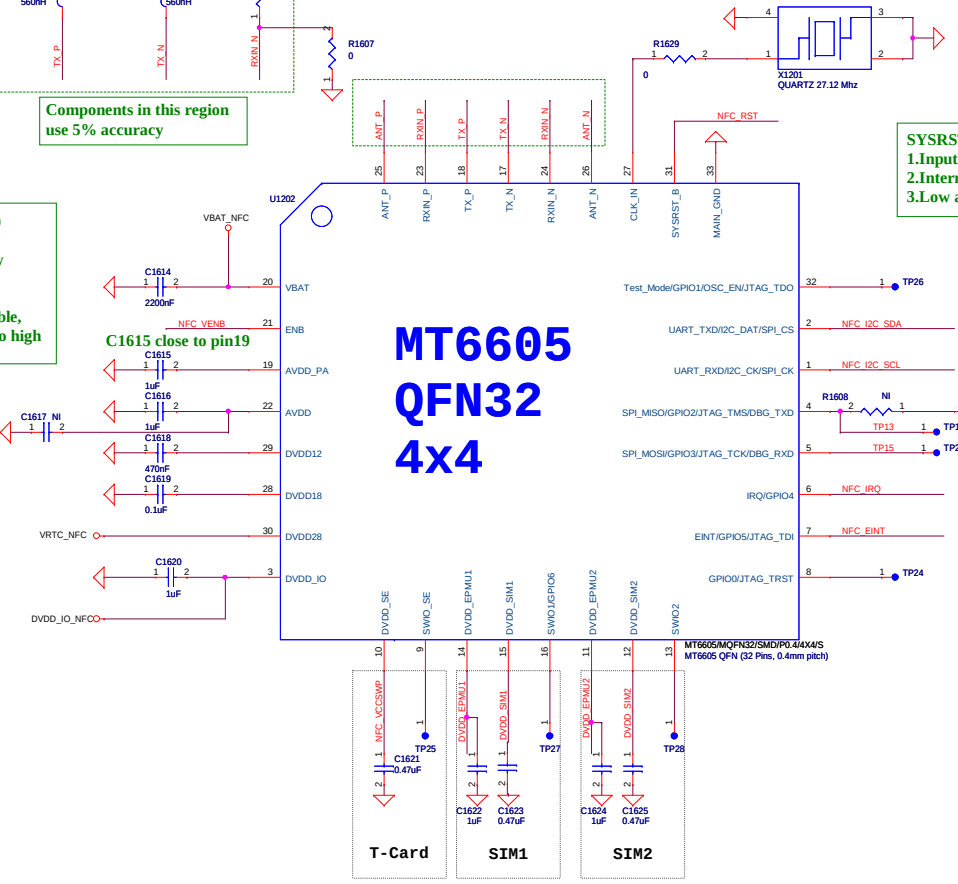
C1601,C1602,C1603,C1604,C1605,C1606,C1607, C1608, C1609 need to use 2% accuracy and 50V tolerance capacitor
PS: 0201 cap can't tolerance 50V

10/9 Fine tune
C1604,C1605 15pF->10pF
R1603,R1604 6.8ohm->1.2ohm
C1601,C1602 56pF->39pF

Components in this region use 5% accuracy

POWER MODE[1:0]=[NFC_RST:NFC_VENB]

Power Mode	NFC_RST	NFC_VENB
NFC enable (configure, R/W, card, polling loop, polling loop card listening)	1	0
NFC disable (HPD)	0	1
Hign battery card listening	1	1
Reset	0	0



ENB (NFC_VEN)
1.Input pin
2.Internal pull low
3.Low active
4.If default NFC would like to disable, please configure to high

C1615 close to pin19

SYSRST_B (NFC_RST)
1.Input pin
2.Internal pull high
3.Low active

Only can use HW I2C.
SW I2C is not allowed.

R1608 NC : XTAL MODE
R1608 10K : Co-Clock

IRQ(NFC_IRQ) , OSC_EN(NFC_OSC_EN) are output pin, and both are high active

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Title: MT7621A			
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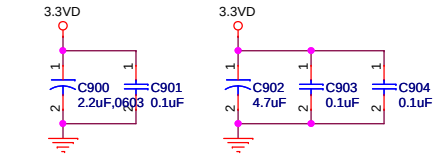
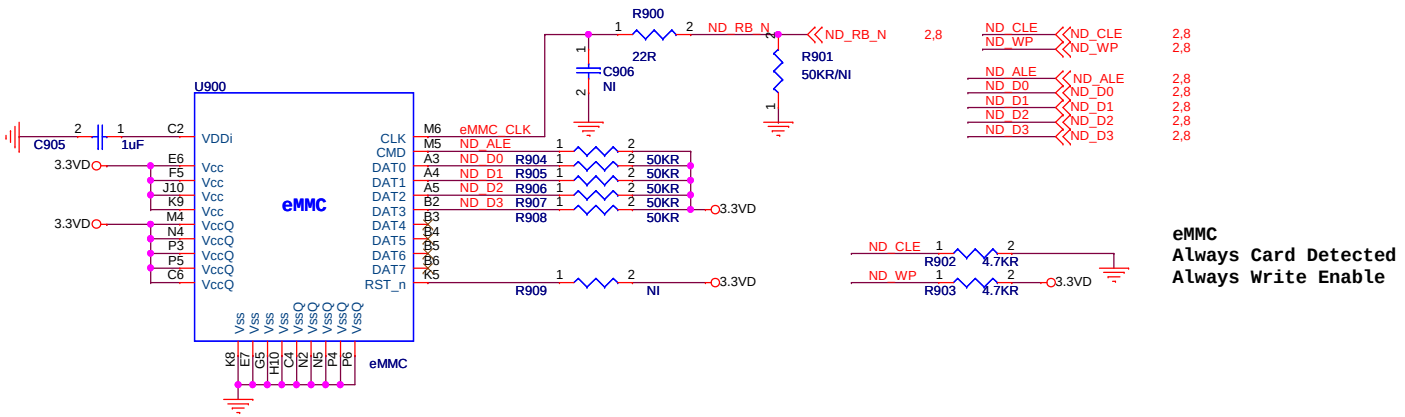


Near VCC (eMMC) Near VCCQ (eMMC)



eMMC
Always Card Detected
Always Write Enable

sd_wp (I)	nd_wp (O)
sd_clk (I/O)	nd_rb_n (I)
sd_cd (I)	nd_cle (O)
sd_cmd (I/O)	nd_ale (O)
sd_data[0] (I/O)	nd_d[0] (I/O)
sd_data[1] (I/O)	nd_d[1] (I/O)
sd_data[2] (I/O)	nd_d[2] (I/O)
sd_data[3] (I/O)	nd_d[3] (I/O)

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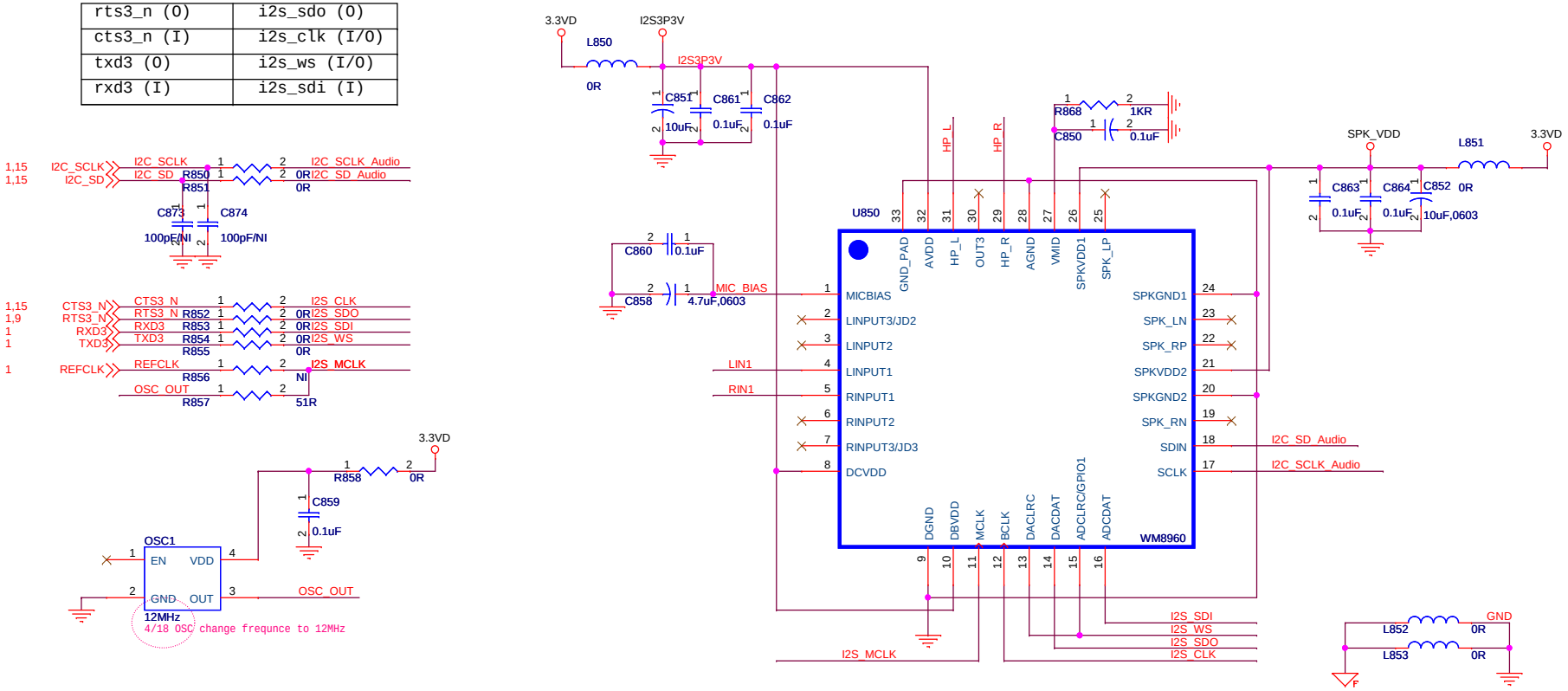
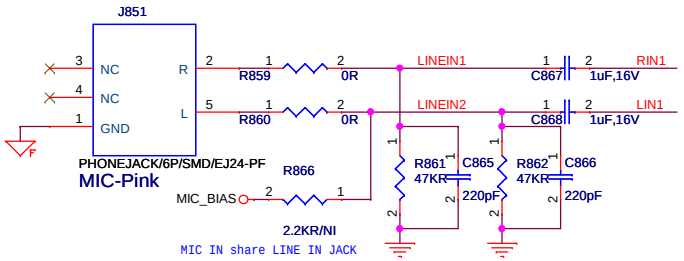
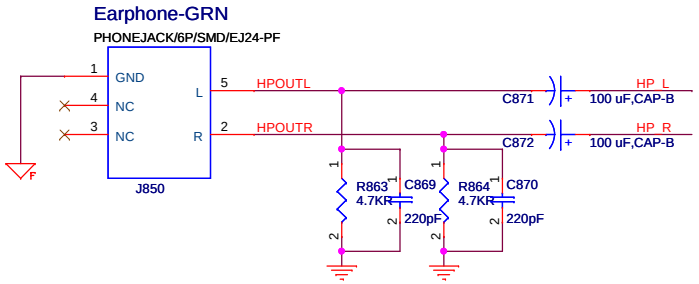
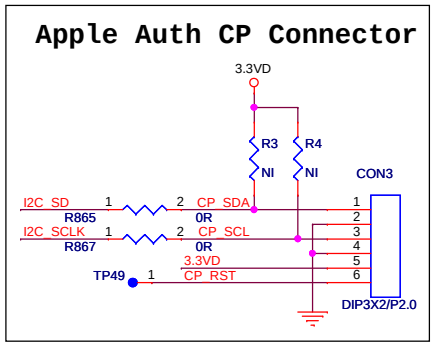
rts3_n (O)	i2s_sdo (O)
cts3_n (I)	i2s_clk (I/O)
txd3 (O)	i2s_ws (I/O)
rxd3 (I)	i2s_sdi (I)









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MEDIATEK	Title: Audio Codec WM8960		
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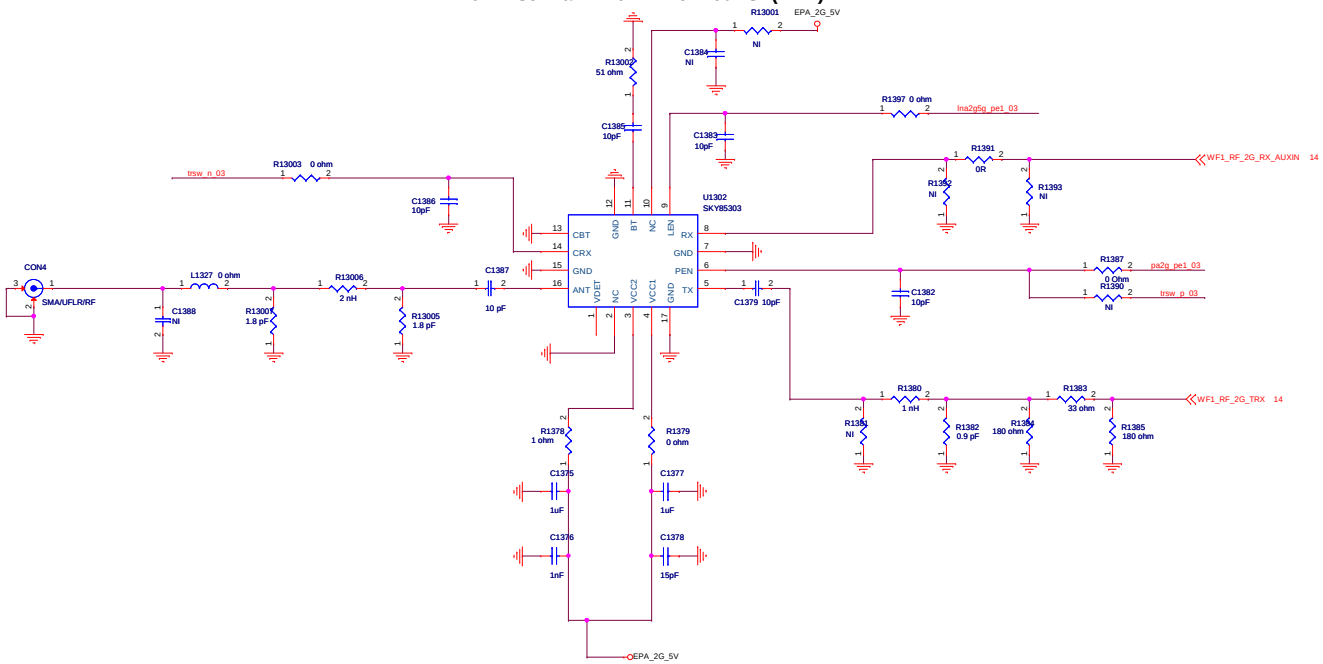
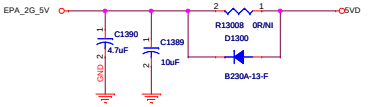
2G External PA/LNA Circuit (WF1)

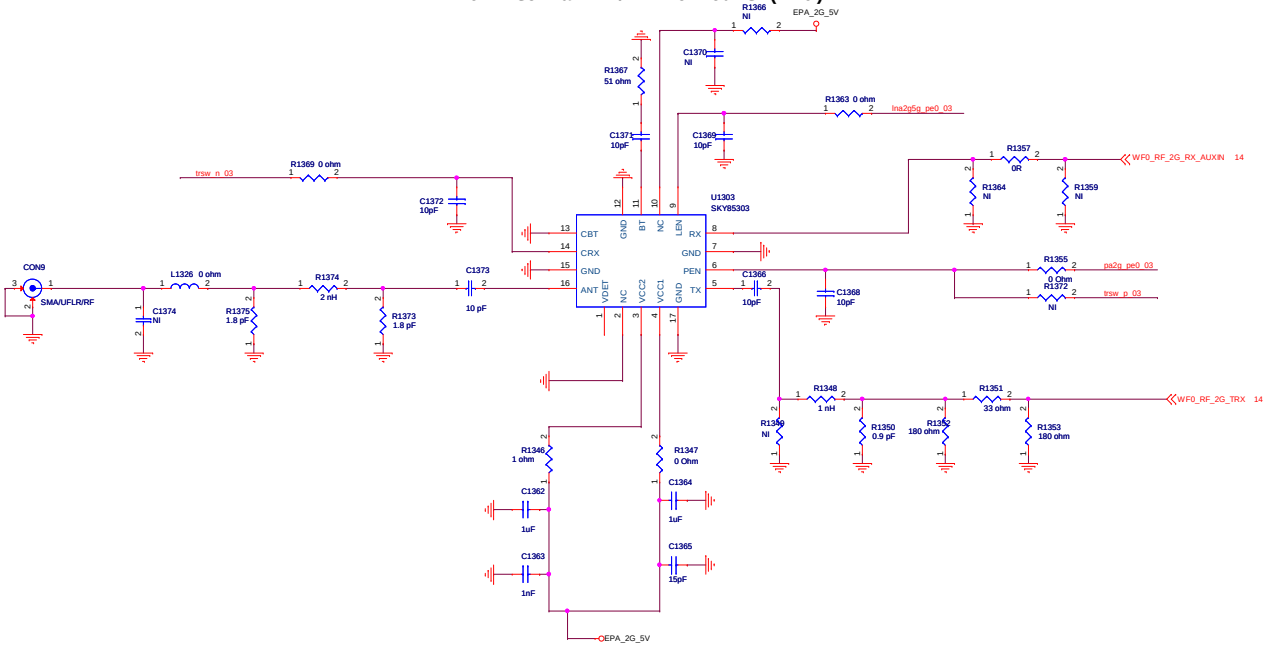




14 trsw_p_03 — trsw_p_03
14 trsw_n_03 — trsw_n_03
14 lna2g5g_pe0_03 — lna2g5g_pe0_03
14 lna2g5g_pe1_03 — lna2g5g_pe1_03
14 pa2g_pe0_03 — pa2g_pe0_03
14 pa2g_pe1_03 — pa2g_pe1_03

14 WF1_RF_2G_TRX — WF1_RF_2G_TRX
14 WF0_RF_2G_TRX — WF0_RF_2G_TRX
14 WF1_RF_2G_RX_AUXIN — WF1_RF_2G_RX_AUXIN
14 WF0_RF_2G_RX_AUXIN — WF0_RF_2G_RX_AUXIN

2G External PA/LNA Circuit (WF0)



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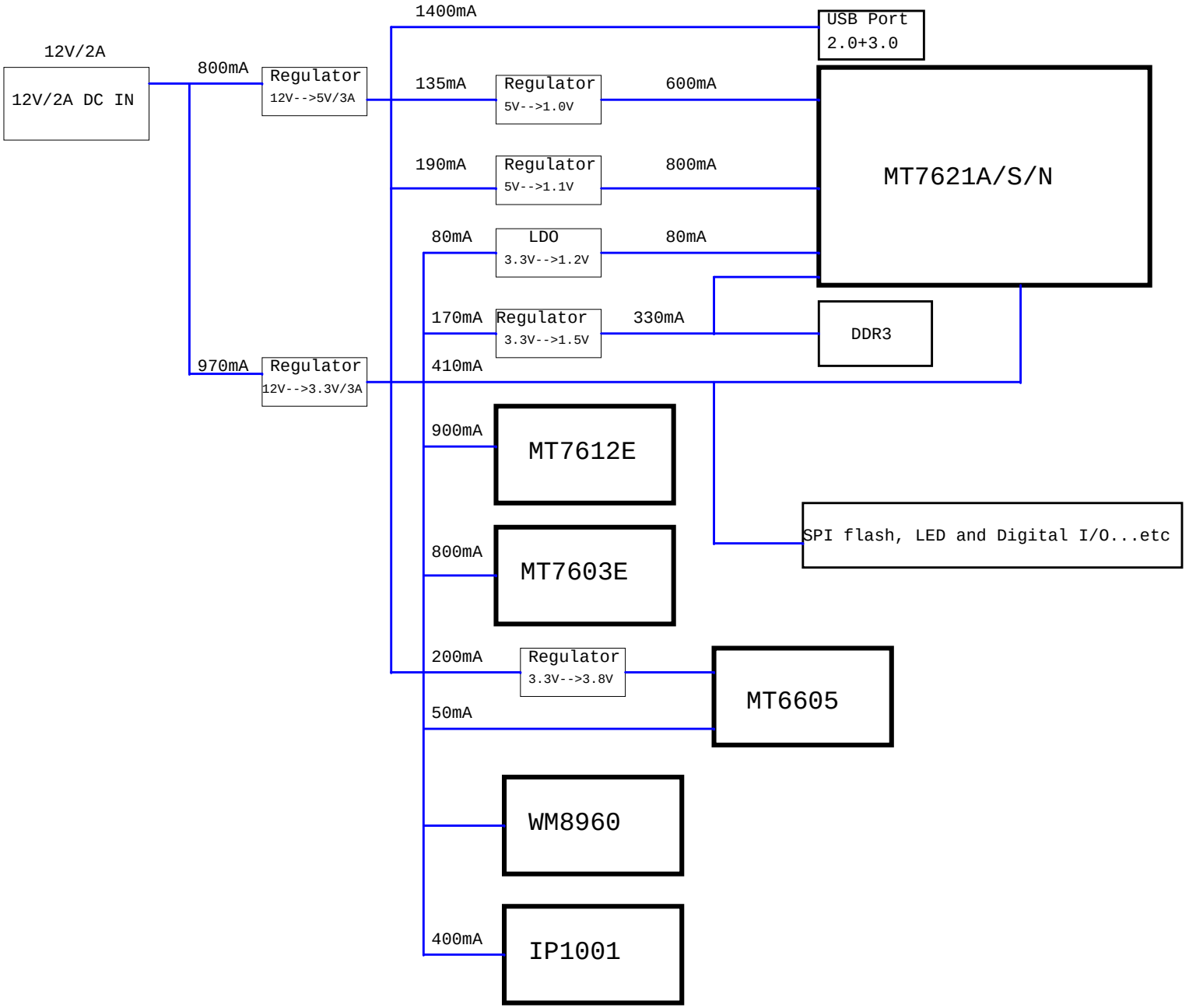

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