SONY

Diagonal 8.000 mm (Type 1/2.0) 48Mega-Pixel CMOS Image Sensor with Square Pixel for Color Cameras

IMX586-AAJH5-C

General description and application

IMX586 is a diagonal 8.000 mm (Type 1/2.0) 48 Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Sony's back-illuminated and stacked CMOS image sensor to achieve high speed image capturing by column parallel A/D converter circuits and high sensitivity and low noise image (comparing with conventional CMOS image sensor) through the backside illuminated imaging pixel structure. R, G, and B pigment primary color mosaic filter is employed. It operates with five power supply voltages: analog 2.8 V and 1.8V, digital 1.1 V, PLL-PHY 1.1V and 1.8 V for input/output interface and achieves low power consumption.
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Functions and Features

- ◆ Back-illuminated and stacked CMOS image sensor
- ◆ Quad Bayer Coding color filter arrangement
- ◆ Phase Detection Auto Focus (PDAF)
- ◆ High Frame Rate 30fps@Full resolution (QBC Re-mosaic) / 30fps@QBC-HDR / 120fps@2x2 Adjacent Pixel Binning (16:9) / 240fps@2x2 Adjacent Pixel Binning V2H2(16:9)
- ◆ High signal to noise ratio(SNR)
- ◆ Dual sensor synchronization operation
- ◆ Built-in 2D Dynamic Defect Pixel Correction
- ◆ Lens Shading Correction (LSC)
- ◆ Built-in temperature sensor
- ◆ Output video format of RAW10/8, COMP8
- ◆ QBC Re-mosaic function
- ◆ QBC HDR function
- ◆ Two PLLs for independent clock generation for pixel control and data output interface
- ◆ CSI-2 serial data output
  MIPI D-PHY 2lane/4lane, Max. 2.5Gbps/lane, D-PHY spec. ver. 1.2 compliant
  MIPI C-PHY 1/2/3trio, Max 2.5Gsps/Trio, C-PHY spec ver. 1.0 compliant
- ◆ 2-wire serial communication (Supports I^2C "Fast mode" and "Fast-mode Plus")
- ◆ 28K bit of OTP ROM for users

Device Structure

◆ CMOS image sensor
◆ Image size : Diagonal 8.000 mm (Type 1/2.0)
◆ Total number of pixels : 8032 (H) × 6248 (V) approx. 50.18 M pixels
◆ Number of effective pixels : 8032 (H) × 6088 (V) approx. 48.89 M pixels
◆ Number of active pixels : 8000 (H) × 6000 (V) approx. 48.00 M pixels
◆ Chip size : 7.504 mm (H) × 5.659 mm (V)
◆ Unit cell size : 0.80 μm (H) × 0.80 μm (V)
◆ Substrate material : Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog1)	VANA1	-0.3 to +4.2	V	refer to VSS level
Supply voltage (analog2)	VANA2	-0.3 to +2.52	V	
Supply voltage (digital1, digital2(PLL-PHY))	VDIG1,2	-0.3 to +1.54	V	
Supply voltage (interface)	VIF	-0.3 to +2.52	V	
Input voltage (digital)	VI	-0.3 to +2.52	V	
Output voltage (digital)	VO	-0.3 to +2.52	V	
Guaranteed Operating temperature	TOPR	-20 to +70	˚C	
Guaranteed storage temperature	TSTG	-30 to +80	˚C	
Guaranteed performance temperature	TSPEC	-20 to +60	˚C	

Recommended Operating Voltage

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog1)	VANA1	2.8 ± 0.1	V	refer to VSS level
Supply voltage (analog2)	VANA2	1.8 ± 0.1	V	
Supply voltage (digital1, digital2(PLL-PHY))	VDIG1,2	1.1 ± 0.1	V	
Supply voltage (interface)	VIF	1.8 ± 0.1	V	

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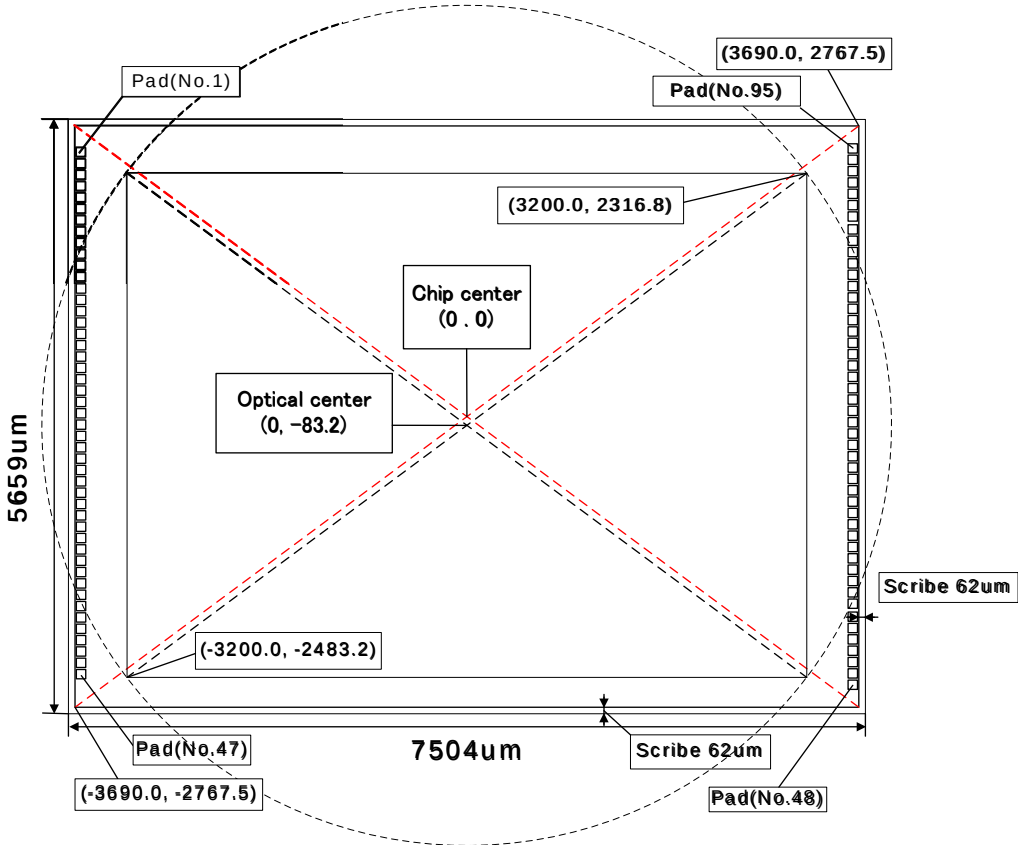
General-0.0.9

Contents

1. Chip Center and Optical Center



*1 Actual size of a chip will be smaller than indicated when dicing (scribe) is taken into account.

*2 Some PADs are located in image circle.

Figure 1 Chip Center and Optical Center (x and y coordinates in µm)

2. Pin Coordinates

Table 1 Pin Coordinates

No.	Symbol	X	Y
1	VDDHSN1	-3633.25	2515.50
2	VSSHSN1	-3633.25	2407.50
3	VDDMCM1	-3633.25	2299.50
4	VSSLCB1	-3633.25	2191.50
5	VSSLCN1	-3633.25	2083.50
6	VDDLCN1	-3633.25	1975.50
7	VSSLSC1	-3633.25	1867.50
8	VDDLSC1	-3633.25	1759.50
9	VSSLPL1	-3633.25	1651.50
10	VDDLPL1	-3633.25	1543.50
11	VSSSUB	-3633.25	1435.50
12	VSSLSC2	-3633.25	1327.50
13	VDDLSC2	-3633.25	1219.50
14	VSSLSC3	-3633.25	1111.50
15	VDDLSC3	-3633.25	1003.50
16	VSSLPL2	-3633.25	895.50
17	VDDLPL2	-3633.25	787.50
18	ZTRM	-3633.25	679.50
19	VDDLIF1	-3633.25	571.50
20	VSSLIF1	-3633.25	463.50
21	D3P0A	-3633.25	355.50
22	D3N0B	-3633.25	247.50
23	D1P0C	-3633.25	139.50
24	D1N1A	-3633.25	31.50
25	CKP1B	-3633.25	-76.50
26	CKN1C	-3633.25	-184.50
27	VSSLIF2	-3633.25	-292.50
28	VDDLIF2	-3633.25	-400.50
29	VSSLSC4	-3633.25	-508.50
30	VDDLSC4	-3633.25	-616.50
31	D2P2A	-3633.25	-724.50
32	D2N2B	-3633.25	-832.50
33	D4P2C	-3633.25	-940.50
34	D4N	-3633.25	-1048.50
35	VSSLIF3	-3633.25	-1156.50
36	VDDLIF3	-3633.25	-1264.50
37	VDDMIF	-3633.25	-1372.50
38	VSSMIF	-3633.25	-1480.50
39	VSSLSC5	-3633.25	-1588.50
40	VDDLSC5	-3633.25	-1696.50
41	VDDLCN2	-3633.25	-1804.50
42	VSSLCN2	-3633.25	-1912.50
43	VSSLCB2	-3633.25	-2020.50
44	VDDMCM2	-3633.25	-2128.50
45	VSSHSN2	-3633.25	-2236.50
46	VDDHSN2	-3633.25	-2344.50
47	VDDSUB	-3633.25	-2452.50
48	VDDHSN3	3633.25	-2553.30
49	VSSHSN3	3633.25	-2445.30
50	VDDMCM3	3633.25	-2337.30

No.	Symbol	X	Y
51	TESTOUT	3633.25	-2229.30
52	TENABLE	3633.25	-2121.30
53	SLASEL	3633.25	-2013.30
54	GPO	3633.25	-1905.30
55	VSSLCB3	3633.25	-1781.55
56	VSSLCN3	3633.25	-1673.55
57	VDDLCN3	3633.25	-1565.55
58	VDDMIO1	3633.25	-1457.55
59	VDDLSC6	3633.25	-1349.55
60	VSSLSC6	3633.25	-1241.55
61	VDDLSC7	3633.25	-1133.55
62	VSSLSC7	3633.25	-1025.55
63	VDDMIO2	3633.25	-917.55
64	INCK	3633.25	-809.55
65	SCL	3633.25	-701.55
66	SDA	3633.25	-593.55
67	SWDIO	3633.25	-485.55
68	SWTCK	3633.25	-377.55
69	VSSHSN4	3633.25	-269.55
70	VDDHSN4	3633.25	-161.55
71	VDDMCM4	3633.25	-53.55
72	VDDHDA	3633.25	54.45
73	VDDHAN	3633.25	162.45
74	VSSHAN	3633.25	270.45
75	TVMON	3633.25	378.45
76	VSSHCP	3633.25	486.45
77	VDDHCP	3633.25	594.45
78	VPI	3633.25	702.45
79	VRL	3633.25	810.45
80	VRLRD	3633.25	918.45
81	VDDLSC8	3633.25	1026.45
82	VSSLSC8	3633.25	1134.45
83	VDDLSC9	3633.25	1242.45
84	VSSLSC9	3633.25	1350.45
85	VDDMIO3	3633.25	1458.45
86	VDDLCN4	3633.25	1566.45
87	VSSLCN4	3633.25	1674.45
88	VSSLCB4	3633.25	1782.45
89	XVS	3633.25	1905.30
90	FSTROBE	3633.25	2013.30
91	POREN	3633.25	2121.30
92	XCLR	3633.25	2229.30
93	VDDMCM5	3633.25	2337.30
94	VSSHSN5	3633.25	2445.30
95	VDDHSN5	3633.25	2553.30

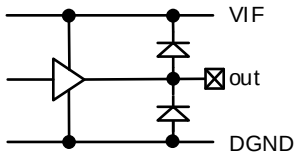
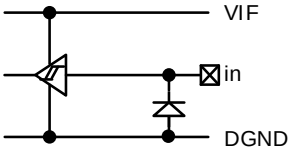
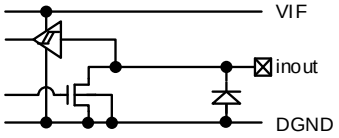
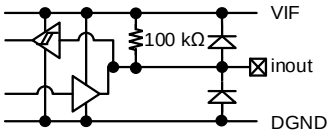
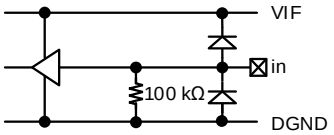
3. Pin Description

Table 2 Pin Description

No.	Symbol	I/O	A/D	Description	Remarks
1	VDDHSN1	Power	A	VANA1 power supply	
2	VSSHSN1	GND	A	VANA GND	
3	VDDMCM1	Power	A	VANA2 power supply	
4	VSSLCB1	GND	D	VDIG1 GND	
5	VSSLCN1	GND	D	VDIG1 GND	
6	VDDLCN1	Power	D	VDIG1 power supply	
7	VSSLSC1	GND	D	VDIG1 GND	
8	VDDLSC1	Power	D	VDIG1 power supply	
9	VSSLPL1	GND	D	VDIG2 GND	
10	VDDLPL1	Power	D	VDIG2 power supply	
11	VSSSUB	GND	D	VDIG1 GND	
12	VSSLSC2	GND	D	VDIG1 GND	
13	VDDLSC2	Power	D	VDIG1 power supply	
14	VSSLSC3	GND	D	VDIG1 GND	
15	VDDLSC3	Power	D	VDIG1 power supply	
16	VSSLPL2	GND	D	VDIG2 GND	
17	VDDLPL2	Power	D	VDIG2 power supply	
18	ZTRM	I	A	Analog input	NC
19	VDDLIF1	Power	D	VDIG2 power supply	
20	VSSLIF1	GND	D	VDIG2 GND	
21	D3P0A	O	D	Digital output	MIPI output (D-PHY:DATA3+/C-PHY:Trio0A)
22	D3N0B	O	D	Digital output	MIPI output (D-PHY:DATA3-/C-PHY:Trio0B)
23	D1P0C	O	D	Digital output	MIPI output (D-PHY:DATA1+/C-PHY:Trio0C)
24	D1N1A	O	D	Digital output	MIPI output (D-PHY:DATA1-/C-PHY:Trio1A)
25	CKP1B	O	D	Digital output	MIPI output (D-PHY:CLK+/C-PHY:Trio1B)
26	CKN1C	O	D	Digital output	MIPI output (D-PHY:CLK -/C-PHY:Trio1C)
27	VSSLIF2	GND	D	VDIG2 GND	
28	VDDLIF2	Power	D	VDIG2 power supply	
29	VSSLSC4	GND	D	VDIG1 GND	
30	VDDLSC4	Power	D	VDIG1 power supply	
31	D2P2A	O	D	Digital output	MIPI output (D-PHY:DATA2+/C-PHY:Trio2A)
32	D2N2B	O	D	Digital output	MIPI output (D-PHY:DATA2-/C-PHY:Trio2B)
33	D4P2C	O	D	Digital output	MIPI output (D-PHY:DATA4+/C-PHY:Trio2C)
34	D4N	O	D	Digital output	MIPI output (D-PHY:DATA4-/C-PHY:NC)
35	VSSLIF3	GND	D	VDIG2 GND	
36	VDDLIF3	Power	D	VDIG2 power supply	
37	VDDMIF	Power	D	VIF power supply	
38	VSSMIF	GND	D	VDIG1 GND	
39	VSSLSC5	GND	D	VDIG1 GND	
40	VDDLSC5	Power	D	VDIG1 power supply	
41	VSSHSN1	Power	D	VDIG1 power supply	
42	VSSLCN2	GND	D	VDIG1 GND	
43	VSSLCB2	GND	D	VDIG1 GND	
44	VDDMCM2	Power	A	VANA2 power supply	
45	VSSHSN2	GND	A	VANA GND	
46	VDDHSN2	Power	A	VANA1 power supply	

No.	Symbol	I/O	A/D	Description	Remarks
47	VDDSUB	Power	A	VANA1 power supply	
48	VDDHSN3	Power	A	VANA1 power supply	
49	VSSHSN3	GND	A	VANA GND	
50	VDDMCM3	Power	A	VANA2 power supply	
51	TESTOUT	O	D	Digital output	NC (for monitor signal output)
52	TENABLE	I	D	Digital input	NC(pull-down internal)
53	SLASEL	I	D	Digital input	I^2C slave address select Pull down(pull-down internal)
54	GPO	O	D	Digital output	NC (for monitor signal output)
55	VSSLCB3	GND	D	VDIG1 GND	
56	VSSLCN3	GND	D	VDIG1 GND	
57	VDDLCN3	Power	D	VDIG1 power supply	
58	VDDMIO1	Power	D	VIF power supply	
59	VDDLSC6	Power	D	VDIG1 power supply	
60	VSSLSC6	GND	D	VDIG1 GND	
61	VDDLSC7	Power	D	VDIG1 power supply	
62	VSSLSC7	GND	D	VDIG1 GND	
63	VDDMIO2	Power	D	VIF power supply	
64	INCK	I	D	Digital input	Clock input
65	SCL	I/O	D	Digital I/O	I^2C pin
66	SDA	I/O	D	Digital I/O	I^2C pin
67	SWDIO	I/O	D	Digital I/O	NC(pull-up internal)
68	SWTCK	I	D	Digital input	NC(pull-down internal)
69	VSSHSN4	GND	A	VANA GND	
70	VDDHSN4	Power	A	VANA1 power supply	
71	VDDMCM4	Power	A	VANA2 power supply	
72	VDDHDA	Power	A	VANA1 power supply	
73	VDDHAN	Power	A	VANA1 power supply	
74	VSSHAN	GND	A	VANA GND	
75	TVMON	O	A	Analog output	NC
76	VSSHCP	GND	A	VANA GND	
77	VDDHCP	Power	A	VANA1 power supply	
78	VPI	Power	A	Analog input	
79	VRL	Minus	A	Analog input	
80	VRLRD	Minus	A	Analog input	
81	VDDLSC8	Power	D	VDIG1 power supply	
82	VSSLSC8	GND	D	VDIG1 GND	
83	VDDLSC9	Power	D	VDIG1 power supply	
84	VSSLSC9	GND	D	VDIG1 GND	
85	VDDMIO3	Power	D	VIF power supply	
86	VDDLCN4	Power	D	VDIG1 power supply	
87	VSSLCN4	GND	D	VDIG1 GND	
88	VSSLCB4	GND	D	VDIG1 GND	
89	XVS	I/O	D	Digital I/O	for dual sync(pull-up internal)
90	FSTROBE	O	D	Digital output	Flash strobe
91	POREN	I	D	Digital input	NC(pull-up internal)
92	XCLR	I	D	Digital input	Chip clear(pull-down internal)
93	VDDMCM5	Power	A	VANA2 power supply	
94	VSSHSN5	GND	A	VANA GND	
95	VDDHSN5	Power	A	VANA1 power supply	

4. Input / Output Equivalent Circuit

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
FSTROBE GPO TESTOUT		INCK	
SCL SDA		XVS	
SLASEL XCLR			

VIF : 1.8 V power supply
DGND : VDIG1 GND

Figure 2 Input / Output Equivalent Circuit

5. Peripheral Circuit Diagram

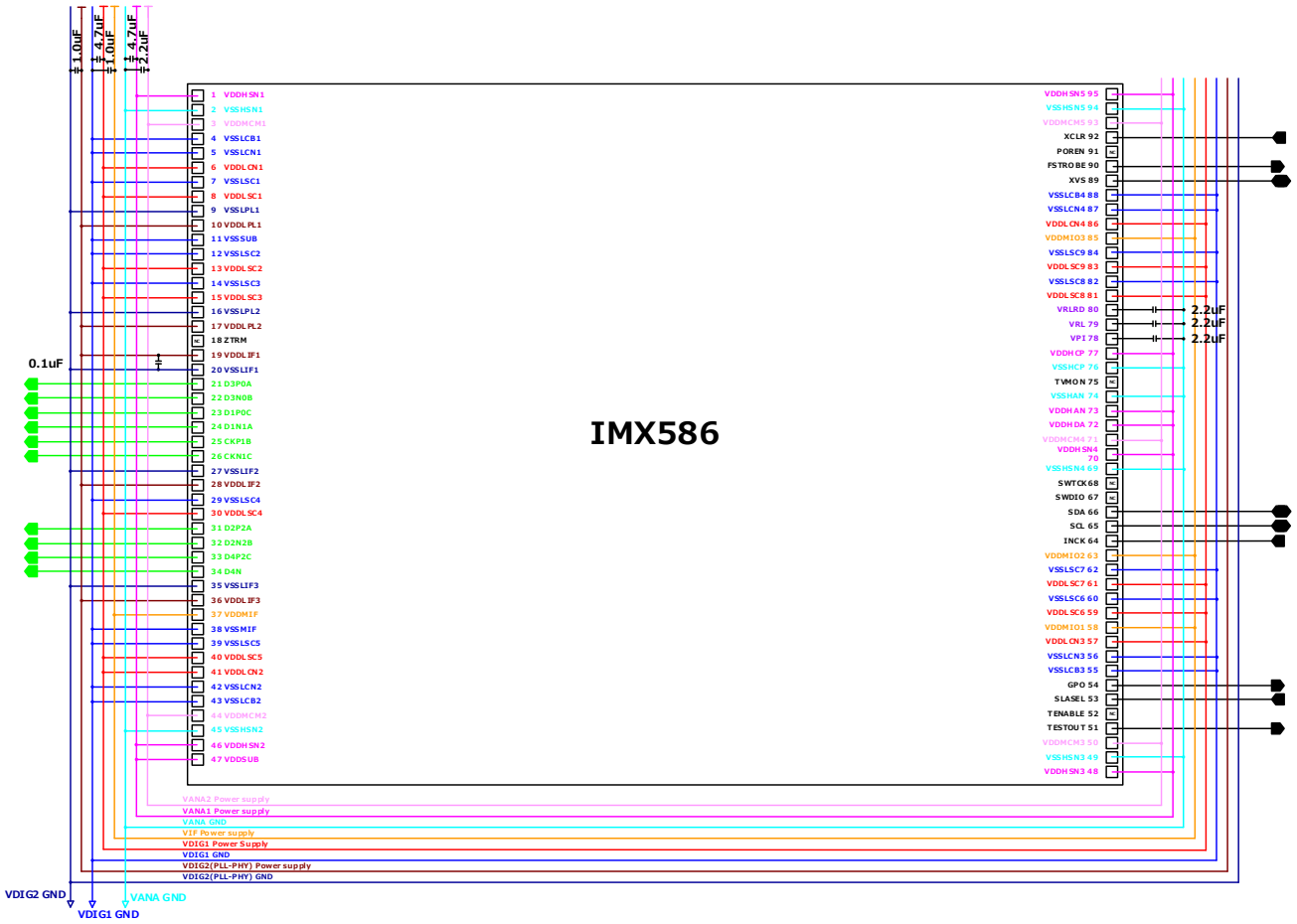


Figure 3 Peripheral Circuit (Recommended schematics)

Note1: The capacitor of 0.1µF is located as close as possible near VDDLIF1/VSSLIF1 pins.

Note2: Sony recommends separating the PLL-PHY Power & PLL-PHY GND from Digital Power Supply and Digital GND to satisfy the high-speed specification which is required by CPHY and DPHY v1.2. If the PLL-PHY Power and PLL-PHY GND could not to separate from Digital Power Supply and Digital GND, power noise interference will be increase and there is possibility to worse the signal jitter.

Note3: I^2C Slave Address can be changed by SLASEL pin.

Table 3 I^2C Slave Address

SLASEL	I^2C Slave Address
L or NC	0x34(write), 0x35(read)
H	0x20(write), 0x21(read)

Note4: In case of using MIPI C-PHY mode, D4N pin is no need to connect(NC). (Even in the case of CPHY, D4N pin is required a connection when you want to connect an evaluation board Sony Semiconductor Solutions Corporation for debug purpose.

Note5: Relationships between functions and status of the terminals are shown in Table 4.

Table 4 Relationships between functions and status of the terminals

Function	Relative pin	Status of the terminal in the schematic above
OTP	VDDHSN	use (VANA1)
I^2C Slave Address change	SLASEL	use(optional)
HWSTB Trigger	XCLR	use
Dual Sensor Synchronization	XVS	use(optional)
Flash Strobe	FSTROBE	use(optional)
Test monitor	GPO, TESTOUT	use(optional)

Note6: Back side or substrate of the sensor chip has a contact with Digital GND (VSSLSC) internally by following the above schematics. No other additional or intentional electrical contact is necessary.

Note7: The capacitor values and parts count used for decoupling of power supply lines in this diagram are determined only with Sony's testing environment. The capacitor values and/or parts count for power line decoupling may have to be reviewed and optimized by each manufacture depending on their design.

6. Functional Description

6-1 System Outline

IMX586 is a CMOS active pixel type image sensor which adopts Sony's back-illuminated and stacked CMOS image sensor to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions. Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.
A onetime programmable memory is embedded in the chip for storing the user data. It has 28 K-bit for user, 64 K-bit as a whole.

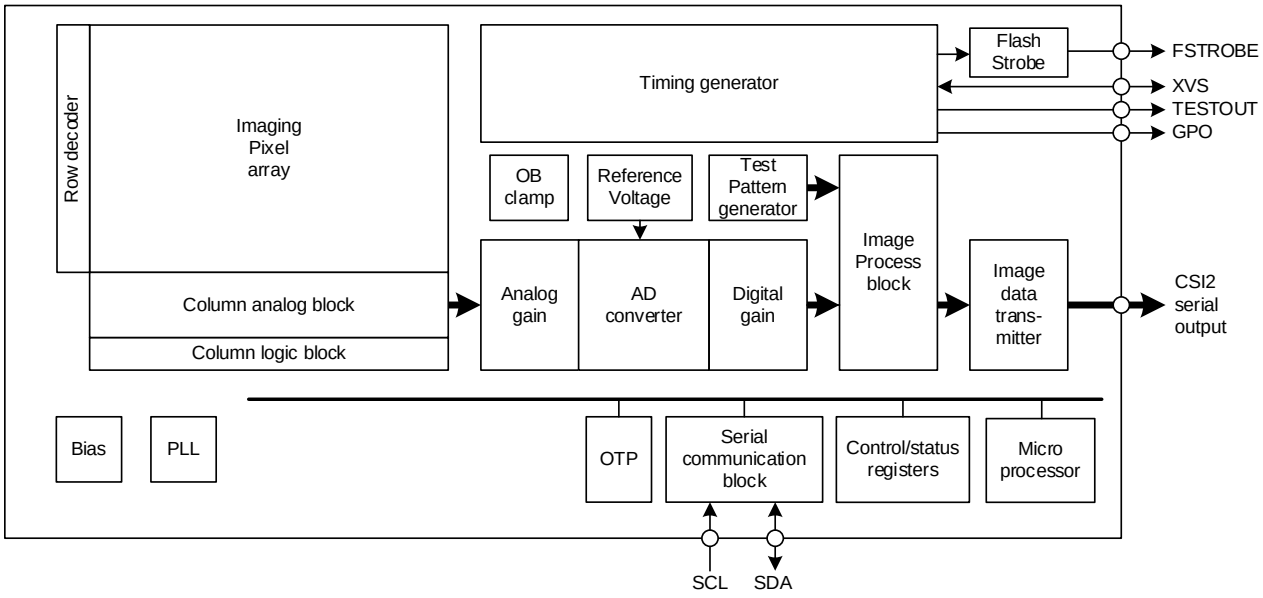


Figure 4 Overview of functional block diagram

6-2 Control register setting by the serial communication

The IMX586 can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows. See Application Notes for more details of each function beyond the following description.

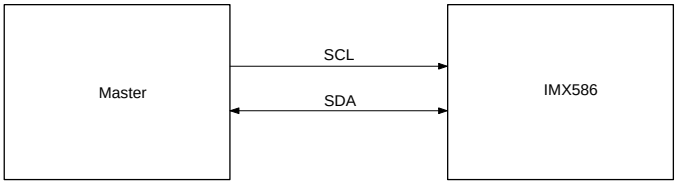


Figure 5 2-wire serial communication

6-2-1 2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I^2C fast-mode compatible interface, and the data transfer protocol is I^2C standard. IMX586 supports two transfer speed mode (Fast-mode ≤400 kHz, Fast-mode Plus* ≤1 MHz).
This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX586.
*only available with INCK ≥ 12.9 MHz

Table 5 Description of 2-wire Serial Communication Pins

pin name	description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of IMX586 are mapped on the 16-bit address space and the register categories shown as below. Detail register information is shown in Register Map.

Table 6 Specification of register address map for 2-wire serial communication

	address range	description
I^2C register	0x0000 - 0x0fff	Configuration register Read Only and Read/Write Dynamic register
	0x1000 - 0x1fff	Parameter limit register Read only static register
	0x2000 - 0x2fff	Reserved
	0x3000 - 0xffff	Manufacture specific register

6-2-2 Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

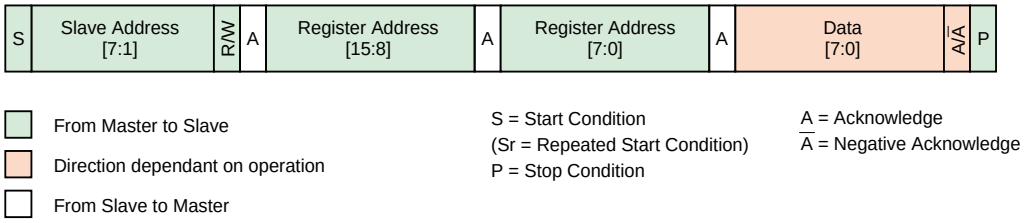
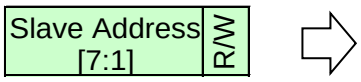


Figure 6 2-wire serial communication protocol

IMX586 has a default slave address shown as below.
The slave address is selectable by pin connection of SLASEL.
When called by the selected slave address, serial communication interface is activated.
Duplication of the address on the same bus must be prevented.
*For other slave address options, refer to Application Note.



Slave Address (Read or Write) * See Table 5 for R/W bit	SLASEL (pin#70)
MSB LSB 0 0 1 1 0 1 0 R/W	L or NC
MSB LSB 0 0 1 0 0 0 0 R/W	H

R/W shows the direction of communication.

Figure 7 Slave address

Table 7 R/W bit

R/W bit	direction of communication
0	Write (Master → Sensor)
1	Read (Sensor → Master)

6-3 Clock generation and PLL

IMX586 equips embedded PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation condition. See Application Notes for more details of each function.

6-3-1 Clock System Diagram

IMX586 is equipped with two PLLs, One outputs IVTCK for image processing, the other is IOPSYCK for MIPI output.
The IVTCK PLL can output at 1250 to 2160 MHz, and the IOPCK PLL can output at 1250 to 2500MHz(C-PHY/DPHY), based on a clock input with the 6 to 27 MHz range.

The IVTCK PLL could be configured with divider of up to 1/1 to 1/4 range, and multiply in the 104 to 360 range.

The IOPCK PLL could be configured with divider of up to 1/1 to 1/15 range, and multiply in the 47 to 2500(C-PHY/DPHY) range.

This sensor normally recommend to make it operate in single PLL mode by driving just one PLL (IOPCK PLL), however can also operate in dual PLL mode by driving both PLLs from parameter setting flexibility point of view.

In PLL single mode, IVT_PREPLLCK _DIV and IVT_PLL _MPY are applied to IOPCK PLL, and IOP_PREPLLCK _DIV and IOP_PLL _MPY are ignored.

.

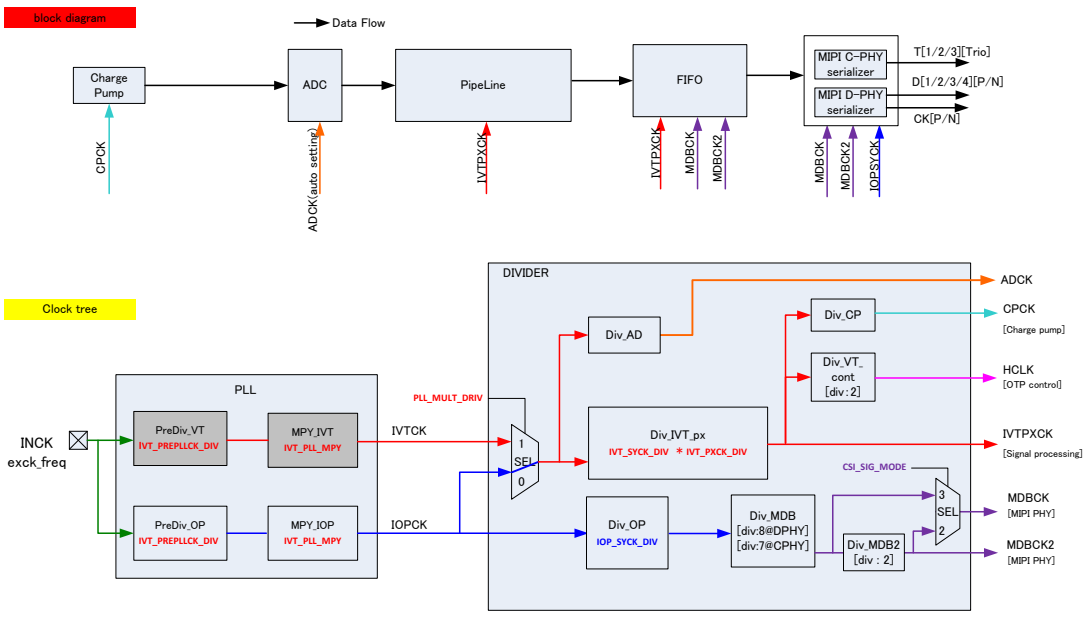


Figure 8 Clock System Diagram (PLL single mode)

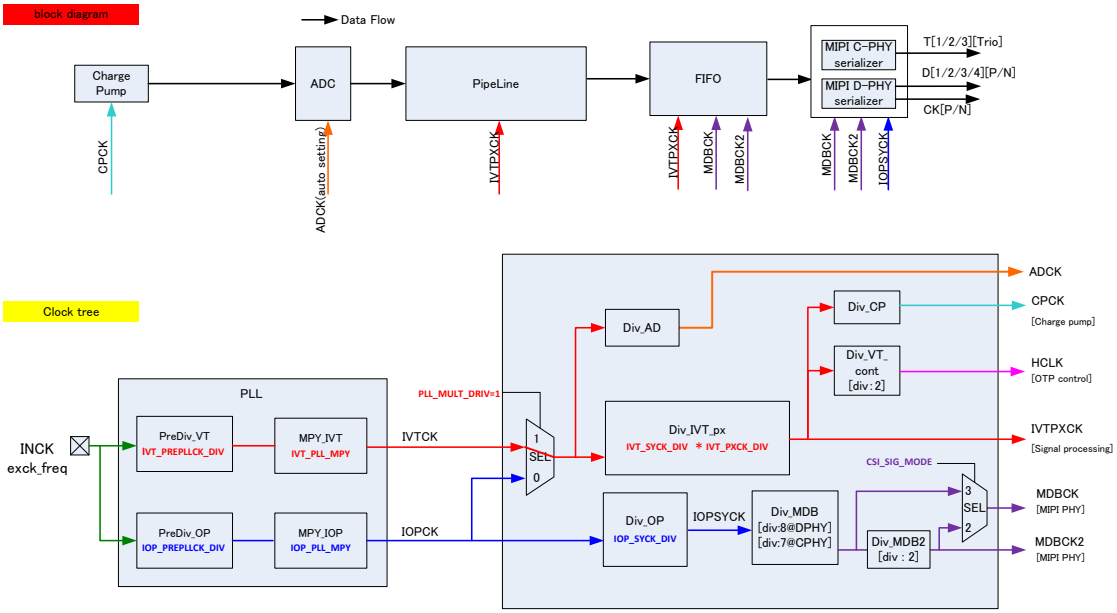


Figure 9 Clock System Diagram (PLL dual mode)

6-4 Description of operation clocks

The followings are general descriptions for each clock. See Application Note for more detail.

6-4-1 INCK

INCK is an external input clock (6 to 27MHz). See “AC characteristics” for electrical requirements to INCK.

6-4-2 IVTCK, IOPCK(PLL output)

These clocks are the root of all the operation clocks in IMX586 and it designates the data rate.
DCKP/DCKN; CSI2 interface clock is generated from IOPCK by dividing into 1/2 frequency since the interface is operated in double data rate format.

6-4-3 IVTPXCK Clock

The clock for internal image processing is used as the base of integration time, frame rate, and etc.

6-4-4 IOPSYCK Clock

The clock for internal image processing is designating the pixel rate and etc.

6-5 Image Readout Operation

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, IMX586 outputs the image data.

See Application Notes for more details of each function.

6-5-1 Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with pin #1 located at the upper left corner.

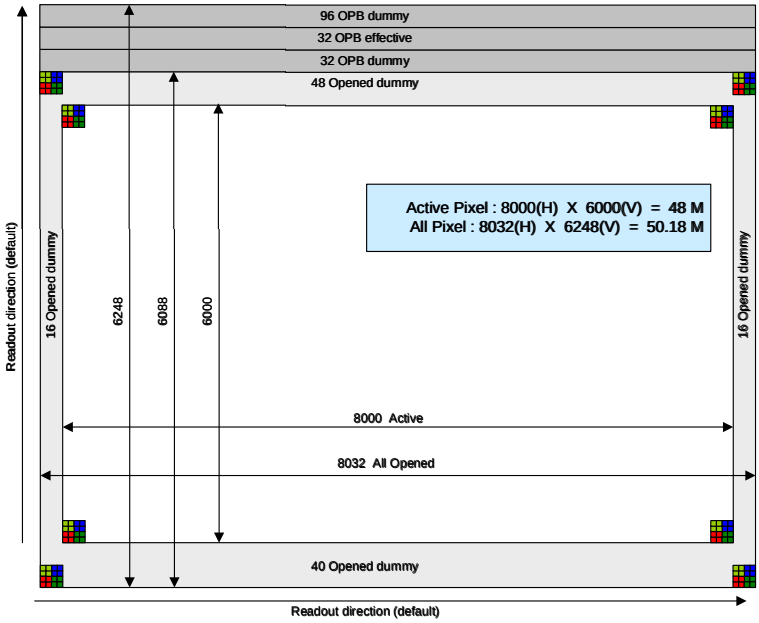


Figure 10 physical alignment of the imaging pixel array

6-5-2 Color coding and order of reading image date

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals respectively. The line with R & Gr signals and the line with Gb & B signals are output alternating one after the other.

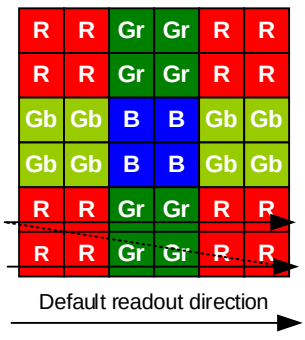


Figure 11 Color coding alignment (Quad Bayer Coding)

6-6 Output Image Format

This is the output image diagram of full pixel output mode(after Re-mosaic), Image data is output from the upper left corner of the diagram.

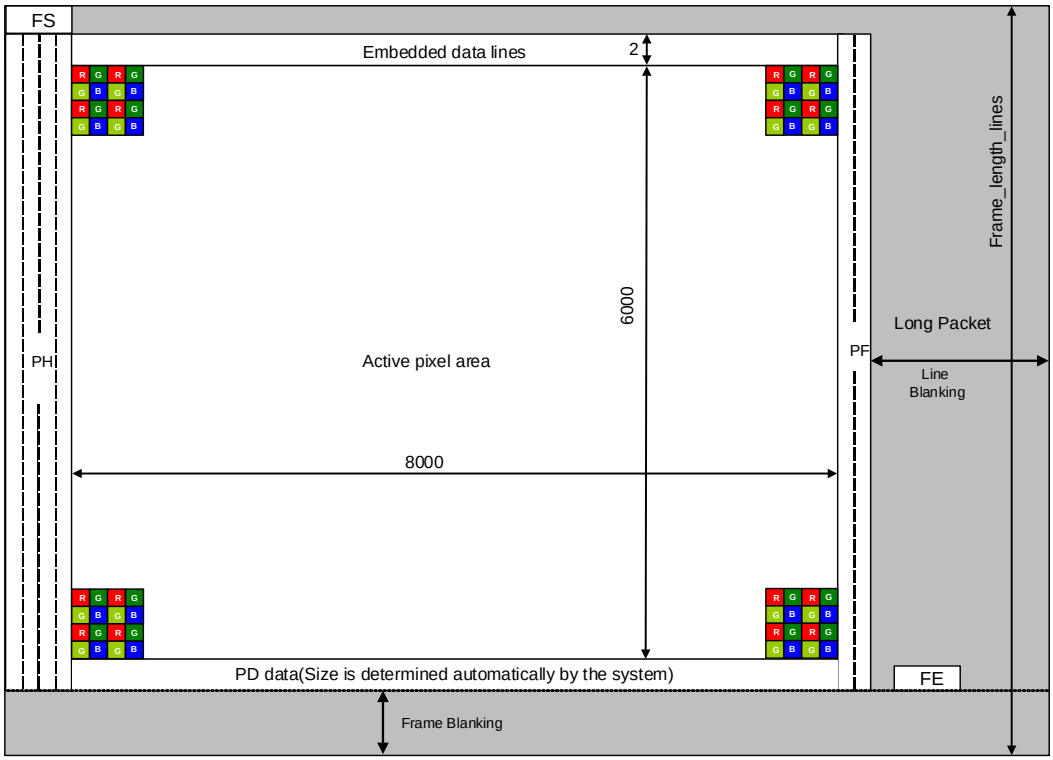


Figure 12 Full pixel output mode data structure

6-6-1 Embedded Data Line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame. The corresponding registers are indicated by “EDL” column of the Register Map.
An unfixed value is output when not outputting embedded data.

See Application Notes for contents and output sequence of Embedded Data Lines.

6-6-2 Image size of mode

IMX586 can capture and output full size(after Re-mosaic), cropped/scaled image in combination with the normal mode. Examples are shown in the table below. Definitions of each parameter are shown in the below figure.

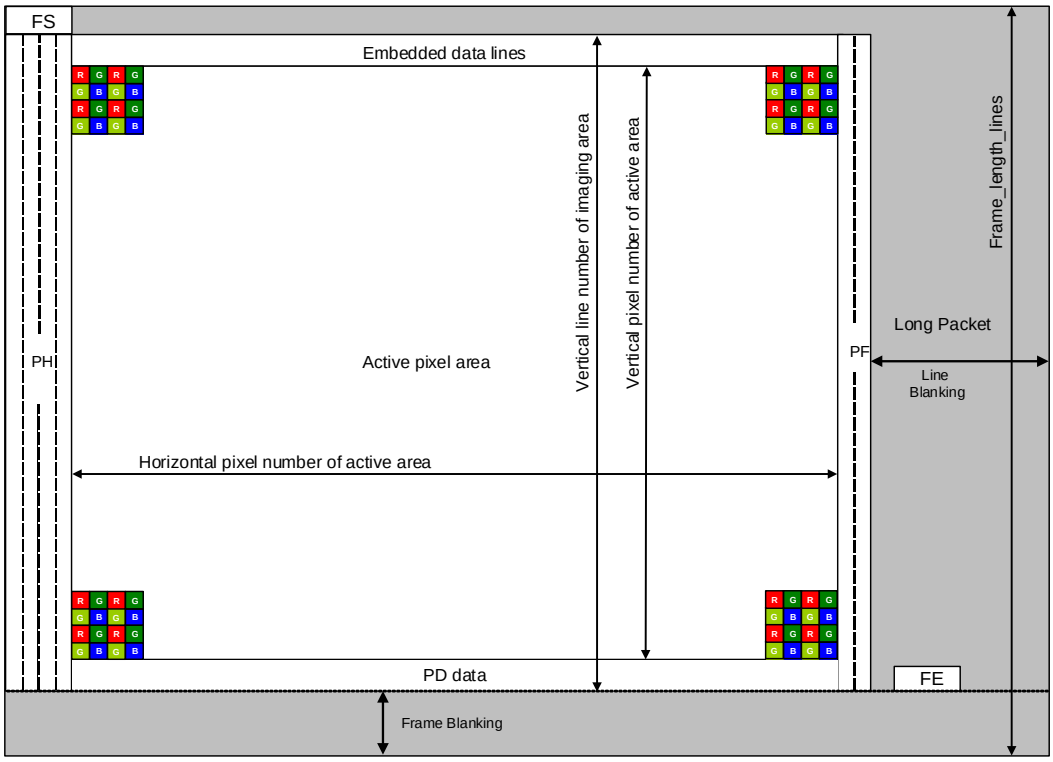


Figure 13 Image size parameter definition

Table 8 modes and image sizes

	Modes						
	Full-pixel	2x2 Adjacent Pixel Binning	2x2 Adjacent Pixel Binning	2x2 Adjacent Pixel Binning	2x2 Adjacent Pixel Binning V2H2	2x2 Adjacent Pixel Binning V2H2 (720p)	QBC HDR
Cropping	Non(4:3)	Non(4:3)	Non(4:3)	Vcrop(16:9)	Vcrop(16:9)	Vcrop(16:9) 720 Crop	Non(4:3)
Binning	Non	H/V	H/V	H/V	H/V	H/V	Non
Scaling	Non	Non	Non	Non	Non	Non	Non
H Pixels	8000	4000	4000	4000	2000	1296	4000*1
V Pixels	6000	3000	3000	2256	1128	736	3000*1
Frame Rate	30fps/19fps*2	100fps	60fps	120fps	240fps	480fps	30fps
PDAF	Support	Not Support	Support	Not Support	Not Support	Not Support	Support
Max Analog Gain	24dB	36dB	36dB	36dB	36dB	30dB	24dB
FOV							
Output							

*1: QBC HDR image is made from 4 same color pixels with different exposure, so the resolution of QBC HDR capture image is half from that of normal capture image.
*2: Notation is frame rate of C-PHY/D-PHY.

6-6-3 Available operation mode

IMX586 have four modes that All-pixel, 2x2 Adjacent Pixel Binning(H:1/2,V:1/2), 2x2 Adjacent Pixel Binning V2H2 (H:1/4, V:1/4), and Quad Bayer Coding HDR(H:1/2,V:1/2).

6-6-4 Image area control capabilities

As control function for image's viewing area and /or image size, IMX586 has capability of vertical analog crop, digital crop, scaling and output crop. In IMX586, horizontal analog cropping is prohibited. The relation of image output size and the resister is shown below.

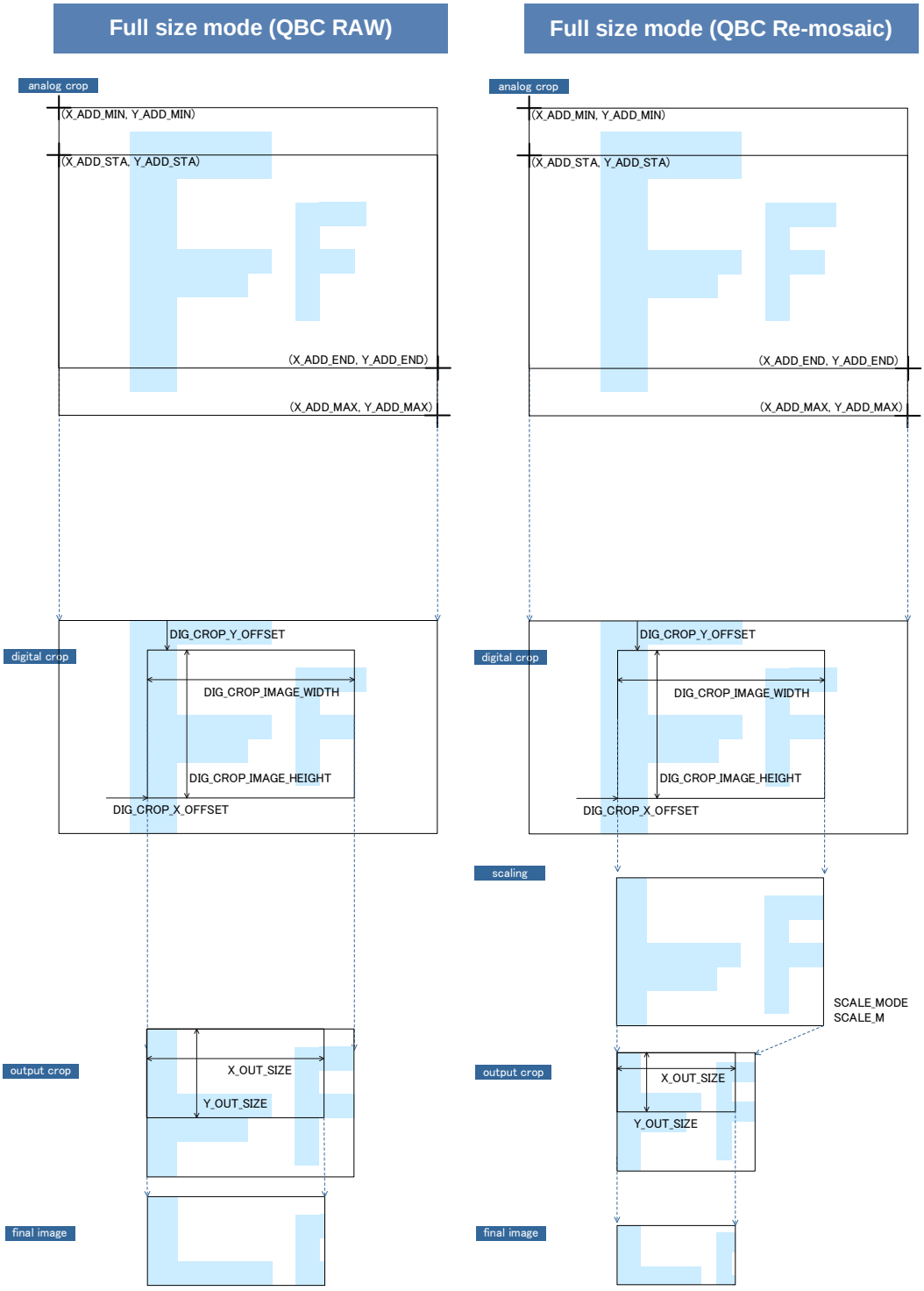


Figure 14 image area control capabilities for full size mode

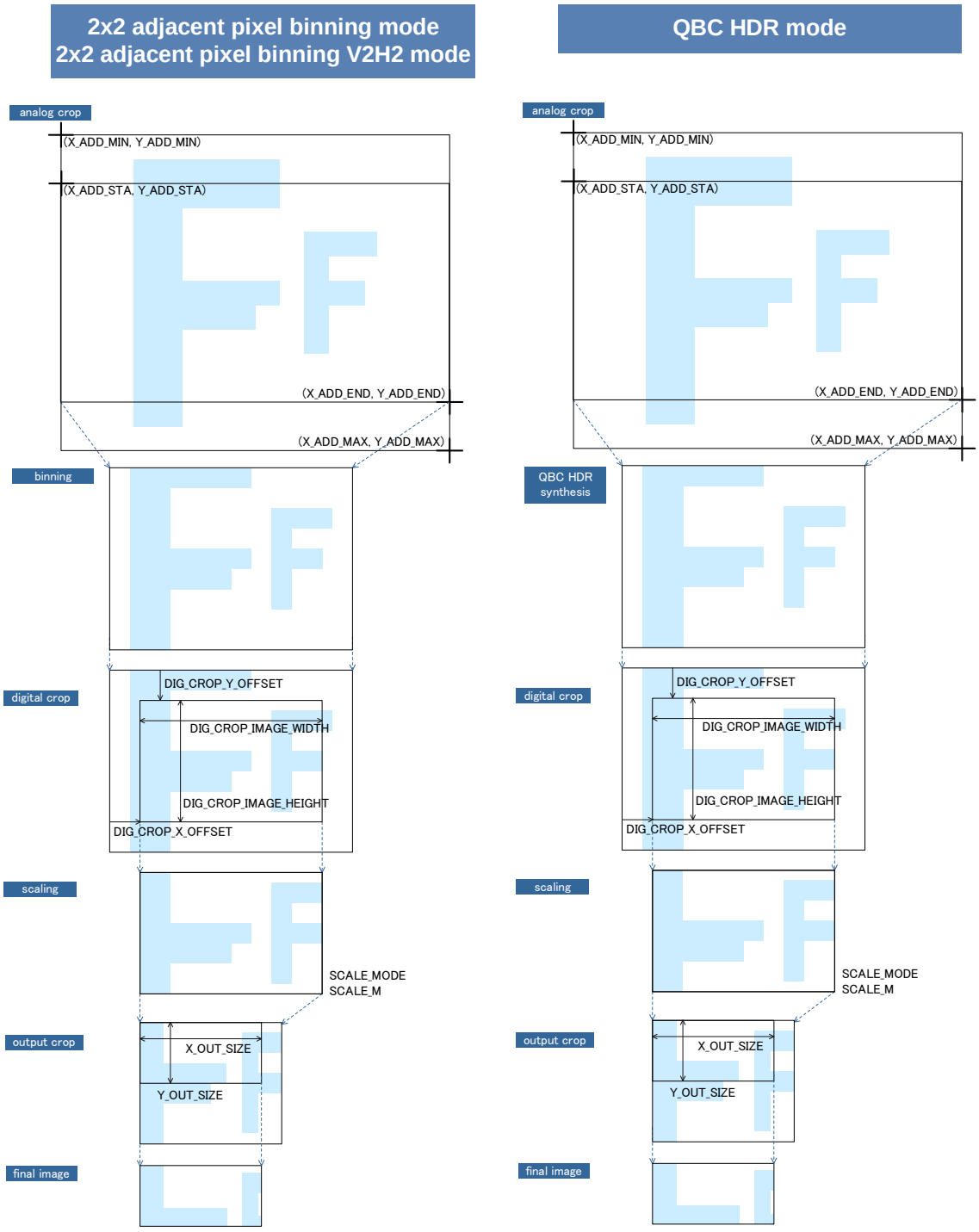


Figure 15 image area control capabilities for 2x2 adjacent pixel binning mode, 2x2 adjacent pixel binning V2H2 mode and QBC HDR mode

Readout Start Position

Default readout position of IMX586 starts from the lower left when PIN1 is placed at the upper left corner. Because the lens will invert the image both vertically and horizontally, the proper image can be archived when PIN1 is placed at the upper left corner.

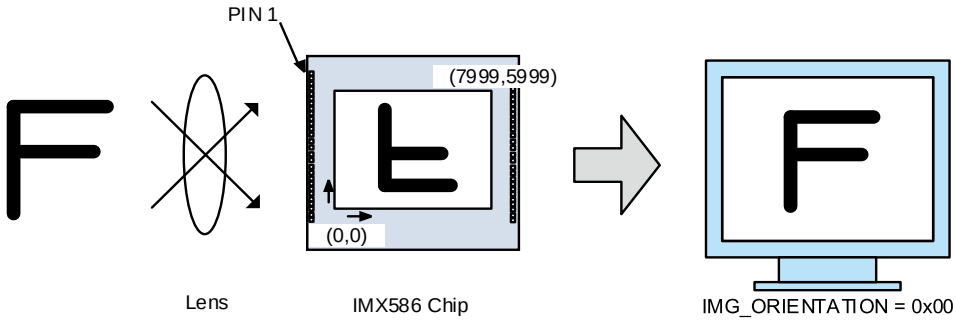


Figure 16 Readout start position

Vertical flip and horizontal mirror readout modes can be specified by the register below. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image. When changing the readout direction, the color of first readout pixel (R/Gr/Gb/B) also changes with it.

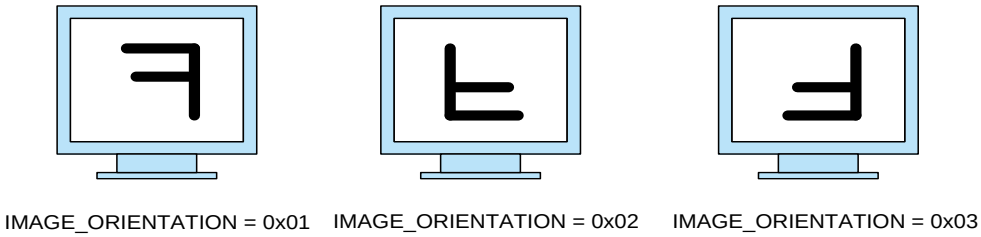


Figure 17 Read out image for each combination of flip and mirror

6-7 Gain setting

IMX586 can apply analog gain on photo-electron signal and digital gain on digital signal after ADC. Range of settable range is as follows.

Table 9 Range of Gains

	Min	Max.	Note
Analog Gain	0dB	24dB	Full-pixel, QBC HDR
	0dB	36dB	2x2 Adjacent Pixel Binning, 2x2 Adjacent Pixel Binning V2H2
	0dB	30dB	2x2 Adjacent Pixel Binning V2H2 720p mode (High speed ADC mode)*
Digital Gain	0dB	24dB	Functionally Settable

* See software reference manual for details.

6-8 Image compensation function

In IMX586 only defect pixel correction is available. Use-case may be chosen in terms of trade-off for power consumption and image quality for example.

See Application Notes for more details of each function.

6-8-1 Defect Pixel Correction

The defect correction function includes static defect correction and dynamic defect correction.

The static defect correction is to correct the defective pixels according to address data stored in OTP. There is only area for Sony Semiconductor Solutions Corporation's factory area.
The dynamic defect correction eliminates any critical defects detected on RGB array by estimating from surrounding adjacent pixels value.

6-8-2 Lens Shading Correction (LSC)

Lens Shading Correction (LSC) is a function to compensate degraded illumination toward the edge of an image.

6-9 Miscellaneous functions

IMX586 has the following additional functions to be used for various final products' features.
See Application Notes for more details of each function.

6-9-1 Phase Detection Auto Focus(PDAF)

Phase Detection Auto Focus (PDAF) function realizes the fast auto focus by using the Phase Difference based on the partially masked sensor pixels. Phase Difference is proportional to the lens defocus value, thus user can move the lens to In-Focus Position directly.

6-9-2 2x1OCL Pixel Correction

2x1OCL pixels have smaller signal value than normal green pixels because a part of the light is blocked off by their shield. 2x1OCL pixels are required to have some gain such that the signal level of each 2x1OCL pixel will be equivalent to a normal pixel. This is called "L/R Correction" (LRC).
For more details, refer to the software reference manual.

6-9-3 Thermal Meter

This function is to measure the thermal data from internal sensor then average it. Measurement results could be read via I^2C or EBD data.

6-9-4 Test pattern output

IMX586 can output the following test pattern by build-in pattern generator.
Test patterns of Solid Color, 100% Color Bar, Fade to Gray Color Bar, PN9 are available.
For Solid Color mode, each value of R, Gr, Gb and B is adjustable.

6-9-5 Long Exposure Setting

IMX586 can achieve a very long exposure time (up to 128 times of 1 vertical period) by simply expanding the vertical blanking time setting.

6-9-6 OTP (One Time Programmable Read Only Memory)

Total of 28 K bit of OTP is available for users.
The area available for the user is total of 56 pages. Among these pages, 64 Byte (address 0 to 63) can be used at the user's discretion, but other pages are reserved as the area for LSC (Lens Shading Correction), QSC (Quad Bayer Coding Sensitivity Correction),
LRC (L/R sensitivity Correction), model ID, unique CCI address and also partially write prohibited.
See OTP manual for details.

6-9-7 Dual sensor synchronization operation

IMX586 supports synchronized shooting operation of two image sensors by implementing both slave and master mode for each sensor. To enable this feature, master/slave must be set for each sensor by software control method. XVS is dedicated output for the synchronization.

6-9-8 Flash light control sequence

IMX586 can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins (FSTROBE).

6-9-9 Monitor terminal settings

IMX586 can output 3 internal signals (H Sync/V Sync/OIS pulse) via monitor terminals.
The monitor terminals mean the following two terminals, such as GPO and TESTOUT.

6-10 Image signal interface

6-10-1 MIPI transmitter

IMX586 outputs image signal by CSI2 high speed serial interface consisted of one pair of clock line and four pairs of data line. See MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) version 1.3 and MIPI Alliance Specification for D-PHY version 1.2 and C-PHY version 1.0 for details.

Because signal is transmitted by differential pair, impedance (generally 100 Ω) between differential pair near the receiver side during HS mode is required. Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

As C-PHY signals are output over 3 lines as a single connection, the recommended signal impedance for a single line is 50 ohms. Make sure all 3 lines wired to the receiving device are the same length for the C-PHY output signals. If all lines are not the same length, the differences in wire length cause jitter at the receiving device, which reduces the timing margin.

Refer to MIPI Alliance C-PHY Standard v1.0 for more detailed information on C-PHY standards.

7. How to operate IMX586

7-1 Power on Reset

IMX586 does not have the built in “Power On Reset” function.
The XCLR pin is set to “LOW” and the power supplies are brought up. Then the XCLR pin should be set to “High” after INCK supplied.

7-2 Power on sequence

7-2-1 Power on slew rate

Maximum slew rate (mV/us) is specified for each power supply to avoid oscillation during power on.

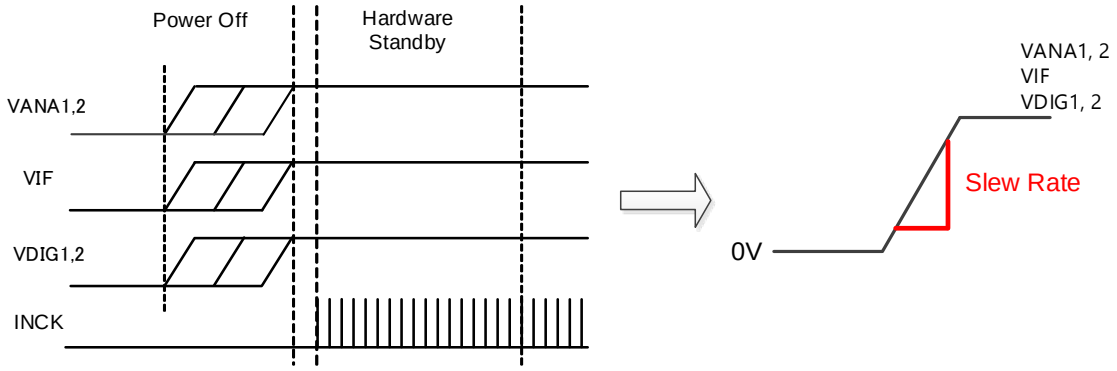


Figure 18 Power on slew rate

Table 10 Limitation on power-on slew rate

Power Supplies	Slew Rate			Comment
	Min	Max	Unit	
VANA1,2, VIF, VDIG1,2	-	100	mV/μs	Tentative

7-2-2 Startup sequence with 2-wire serial communication

Follow the power supply start up sequence as below.

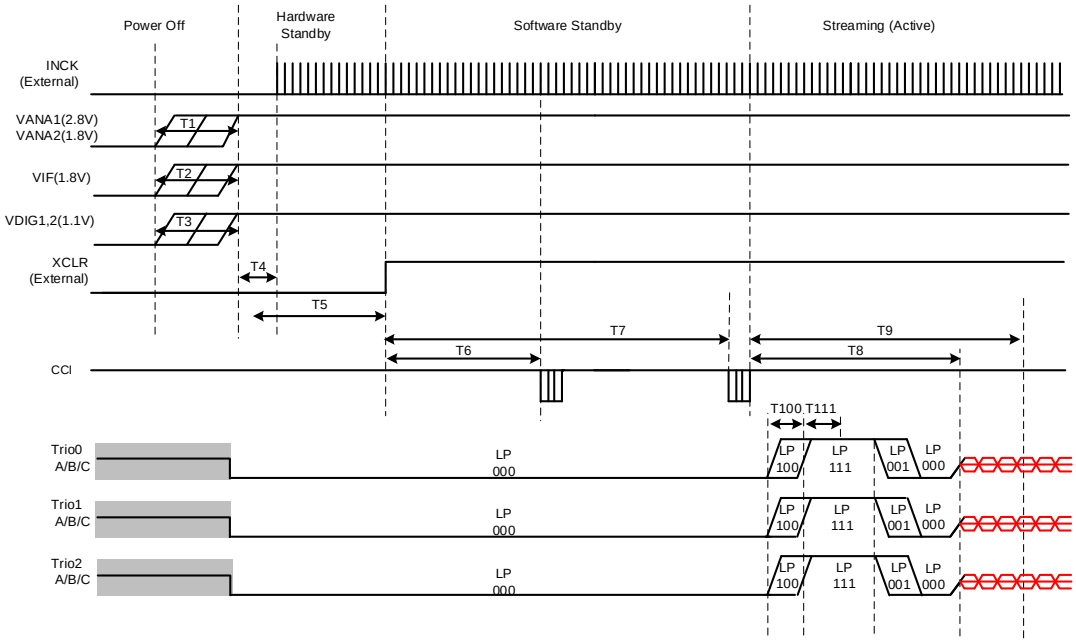


Figure 19 Startup sequence with 2-wire serial communication (C-PHY)

* Presence of INCK during Power Off is acceptable despite of above chart.

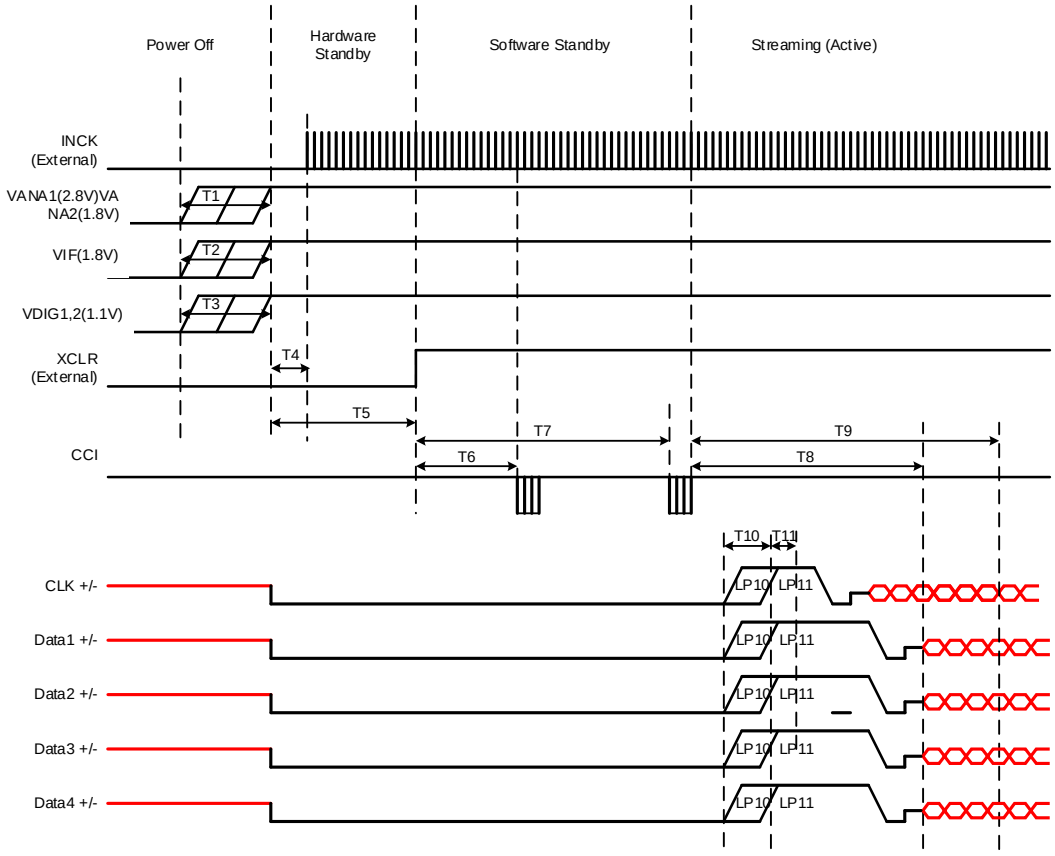


Figure 20 Startup sequence with 2-wire serial communication (D-PHY)

* Presence of INCK during Power Off is acceptable despite of above chart.

Table 11 Startup sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
VANA1,2 rising – VANA1,2 on	T1	VANA1, VANA2, VDIG1, VDIG2 and VIF may rise in any order.		µs	Slew rate of VANA1, VANA2, VDIG1, VDIG2 and VIF(0%-100%) :"refer to 7-2-1 Power on slew rate"
VDIG1,2 rising – VDIG1,2 on	T2			µs	
VIF rising – VIF on	T3			µs	
VANA1, VANA2, VDIG1, VDIG2 and VIF rising – INCK start	T4	0		µs	Later of T1, T2 and T3
VANA1, VANA2, VDIG1, VDIG2 and VIF rising – XCLR rising	T5	0		ms	
XCLR rising till CCI Read Version ID register wait time	T6	1		ms	
INCK rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	8		ms	VRL cap : 2.2µF
Start of first streaming from sending streaming command	T8		5.0 ms + The delay of the coarse integration time value + (Tline * 90[lines]) (tentative)		IVTPXCK = 216MHz INCK = 6MHz
			8.0 ms + The delay of the coarse integration time value + (Tline * 90[lines]) (tentative)		IVTPXCK = 62.5MHz INCK = 6MHz
Start of first streaming with stable frame from sending streaming command.	T9		T8 + 1Frame	Frames	
DPHY power up	T10	1	1.1	ms	
DPHY init	T11	100	110	µs	
CPHY power up	T100	1	1.1	ms	
CPHY init	T111	100	110	µs	

Note : XCLR needs to be Low until all power supplies complete power-on

7-3 Power down sequence

7-3-1 Power down sequence with 2-wire serial communication

Follow the power down sequence below.

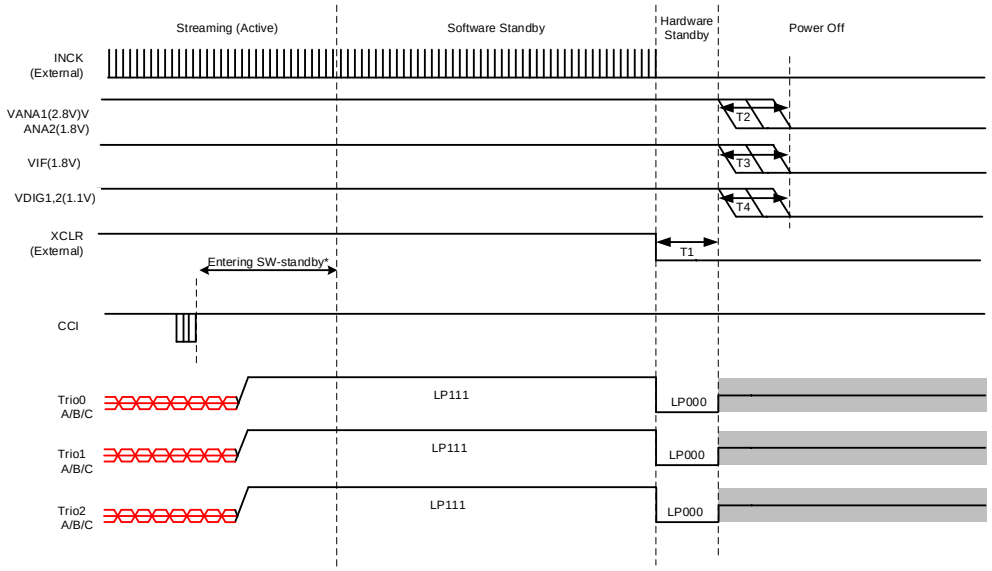


Figure 21 Power down sequence with 2-wire serial communication (C-PHY)

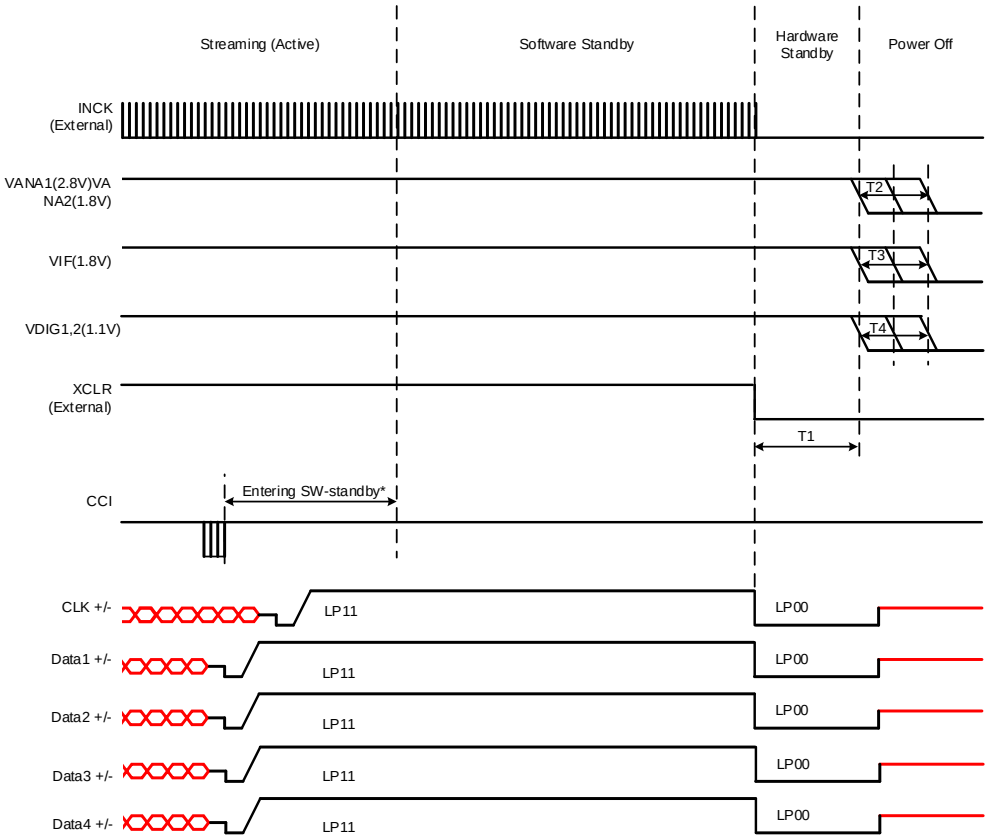


Figure 22 Power down sequence with 2-wire serial communication (D-PHY)

Table 12 Power down sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
XCLR Neg-edge – VANA1,2 (VDIG1,2 or VIF) fall	T1	0		µs	Presence of INCK during Power Off is acceptable.
Sequence free of VANA1,2 falling and VDIG1,2 falling and VIF falling	T2,T3, T4	VANA1,2 and VDIG1,2 and VIF may fall in any order.		µs	

7-4 Register Map

See Register Map.

8. Electrical Characteristics

The Electrical Characteristics of the IMX586 is shown below

8-1 DC characteristics

Table 13 DC Characteristics

Item	Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VDDSUB VDDHSN1 - 5 VDDHAN VDDHDA	VANA1		2.7	2.8	2.9	V
	VDDHCM1 - 5	VANA2		1.7	1.8	1.9	V
	VDDLCN1 - 4 VDDLSC1 - 9	VDIG1		1.0	1.1	1.2	V
	VDDLIF1,2,3 VDDLPL1,2	VDIG2		1.0	1.1	1.2	V
	VDDMIO1,2,3	VIF		1.7	1.8	1.9	V
Digital input voltage	SDA	VIH				2.9	V
	SCL	VIL		-0.3		0.3VIF	V
Digital input voltage	XCLR INCK	VIH		0.65VIF		VIF + 0.3	V
	SLASEL XVS	VIL		-0.3		0.35VIF	V
Digital output voltage	SDA	VOH		VIF-0.2			V
		VOL				0.2VIF	V
Digital output voltage	GPO, FSTROBE, XVS TESTOUT	VOH		VIF-0.2			V
		VOL				0.2	V

8-2 AC Characteristics

8-2-1 Master Clock Waveform Diagram

8-2-1-1 INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.

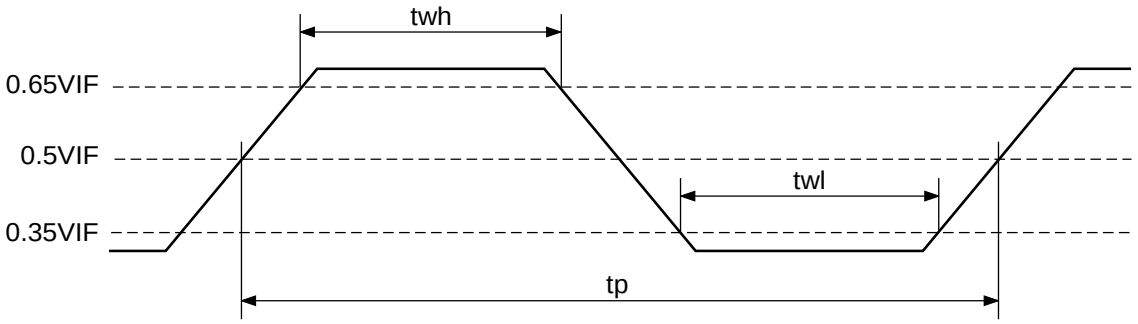


Figure 23 Master Clock Square Waveform Input Diagram

Table 14 Master Clock Square Waveform Input Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{SCK}	6		27	MHz
INCK clock period	t_p	37.0		166.7	ns
INCK low level width	t_{wl}	0.4tp		0.6tp	ns
INCK high level width	t_{wh}	0.4tp		0.6tp	ns
INCK jitter	Tjitter			600	ps

8-2-1-2 INCK Sine Waveform Input Specifications

IMX586 does not support the “AC coupled connection”.
Therefore, there is no description of AC characteristics

8-2-2 PLL block characteristics

Electrical characteristics of PLL block is shown below.

Table 15 PLL block characteristics (VT system)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	6.0		12.0	MHz	
VCO frequency range	1250		2160	MHz	
Output frequency range	1250		2160	MHz	
Settling time			1000	μs	

Table 16 PLL block characteristics (OP system)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	1.0		12.0	MHz	
VCO frequency range	1250		2500	MHz	C-PHY
			2500	MHz	D-PHY
Output frequency range	1250		2500	MHz	C-PHY
			2500	MHz	D-PHY
Settling time			1000	µs	

8-2-3 Definition of settling time of PLL block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

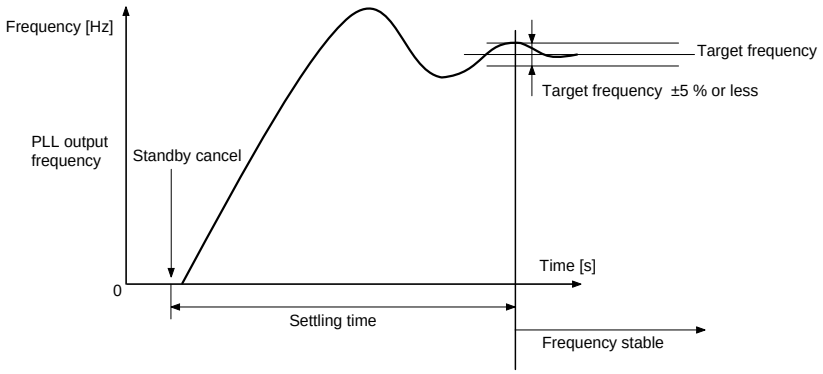


Figure 24 Definition of settling time

8-2-4 2-wire serial communication block characteristics

2-wire serial communication characteristics are shown below.

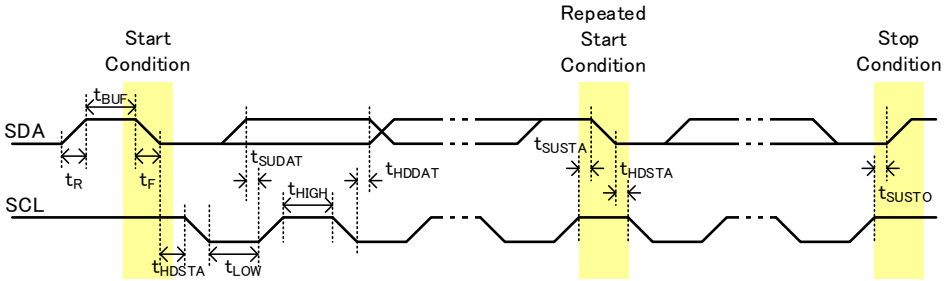


Figure 25 2-wire serial communication block specification

Table 17 2-wire serial communication block specification

Parameter	Symbol	Conditions	Min.	Max. (Fast-mode Plus)	Unit
Low level input voltage	V_{IL}		-0.5	$0.3V_{IF}$	V
High level input voltage	V_{IH}		$0.7V_{IF}$	2.9	V
Low level output voltage	V_{OL1}	VIF > 2 V, Sink 3 mA	0	0.4	V
	V_{OL2}	VIF < 2 V, Sink 3 mA	0	$0.2V_{IF}$	V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 VIF→0.3 VIF		250 (120)	ns
Input current	I_I	0.1 VIF→0.9 VIF	-10	10	μA
SDA I/O capacitance	$C_{I/O}$			10	pF
SCL Input capacitance	C_I			10	pF

Table 18 2-wire serial communication block AC specification

Fast-mode

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Rise time (SDA and SCL)	t_R	-	300	ns
Fall time (SDA and SCL)	t_F	-	300	ns
Hold time (start condition)	t_{HDSTA}	0.6	-	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.6	-	µs
Setup time (stop condition)	t_{SUSTO}	0.6	-	µs
Data setup time	t_{SUDAT}	100	-	ns
Data hold time	t_{HDDAT}	0	0.9	µs
Bus free time between Stop and Start condition	t_{BUF}	1.3		µs
Low period of the SCL clock	t_{LOW}	1.3		µs
High period of the SCL clock	t_{HIGH}	0.6		µs

Fast-mode Plus (Note: Only available with INCK ≥ 12.9 MHz; See module design reference manual for detail.)

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	1000	kHz
Rise time (SDA and SCL)	t_R	-	120	ns
Fall time (SDA and SCL)	t_F	-	120	ns
Hold time (start condition)	t_{HDSTA}	0.26	-	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.26	-	µs
Setup time (stop condition)	t_{SUSTO}	0.26	-	µs
Data setup time	t_{SUDAT}	50	-	ns
Data hold time	t_{HDDAT}	0	-	µs
Bus free time between Stop and Start condition	t_{BUF}	0.5		µs
Low period of the SCL clock	t_{LOW}	0.5		µs
High period of the SCL clock	t_{HIGH}	0.26		µs

Note : Fast-mode Plus supports only available with INCK ≥ 12.9MHz;
See module design reference manual for detail.

8-2-5 Current consumption and standby current

Table 19 Current consumption and standby current

(Full size@30 frame/s, V_{ANA1} = 2.8V, V_{ANA2} = 1.8V, $V_{DIG1,2}$ = 1.1 V, V_{IF} = 1.8 V, Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (analog)	I_{ANA}		TBD	TBD	mA	
Current consumption (digital)	I_{DIG1}		TBD	TBD	mA	
Current consumption (digital)	I_{DIG2}		TBD	TBD	mA	
Current consumption (IF)	I_{IF}		TBD	TBD	mA	
Standby current (analog)	I_{STBANA}			TBD	μA	XCLR : Low fixed INCK :stop
Standby current (digital)	$I_{STBDIG1}$			TBD	μA	XCLR : Low fixed INCK :stop
Standby current (digital)	$I_{STBDIG2}$			TBD	μA	XCLR : Low fixed INCK :stop
Standby current (IF)	I_{STBIF}			TBD	μA	XCLR : Low fixed INCK :stop

9. Spectral Sensitivity Characteristic

(Includes neither lens characteristics nor light source characteristics.)

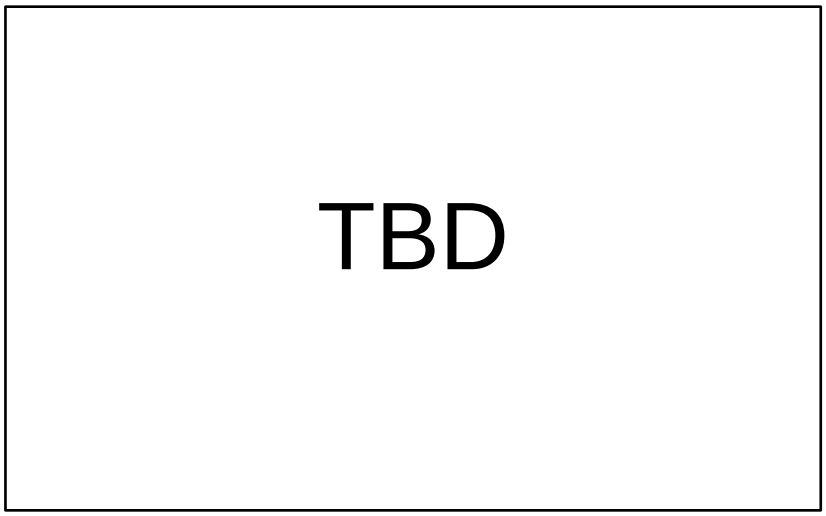


Figure 26 Spectral sensitivity characteristics

10. Image Sensor Characteristics

10-1 Image Sensor Characteristics

Table 20 Image Sensor Characteristics

(Full size@30 frame/s, V_{ANA1}= 2.8V, V_{ANA2}= 1.8V, $V_{DIG1,2}$ = 1.1 V, V_{IF} = 1.8 V, Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Range	Measurement method	Remarks
Sensitivity	S	TBD			LSB	Center	1(*1)	
Sensitivity ratio	RG	TBD	TBD	TBD		Center	2(*1)	
	BG	TBD	TBD	TBD				
Saturation signal	Vsat	1023			LSB	Zone1	3(*1)	Include OB level (*2)
Video signal shading	SH			TBD	%	Zone2D	4(*1)	Design assurance
Dark signal	Vdt			TBD	LSB	Zone2D	5(*1)	When operation at 15 frame/s

The data described at this image sensor characteristics are the measurement standard without base gain setting, and indicates the results evaluated with OB as a reference.

Note 1) These refer to the descriptions of the Measurement Methods on Page 42.

Note 2) LSB is the abbreviation of Least Significant Bit. 10 bits = 1023 digital is the maximum output code for the output unit. The gain setting (base gain setting) in which the saturation signal output matches with 1023 LSB requires 0[dB] when the OB level is 64 LSB (standard recommended value).

10-2 Zone Definition used for specifying image sensor characteristics

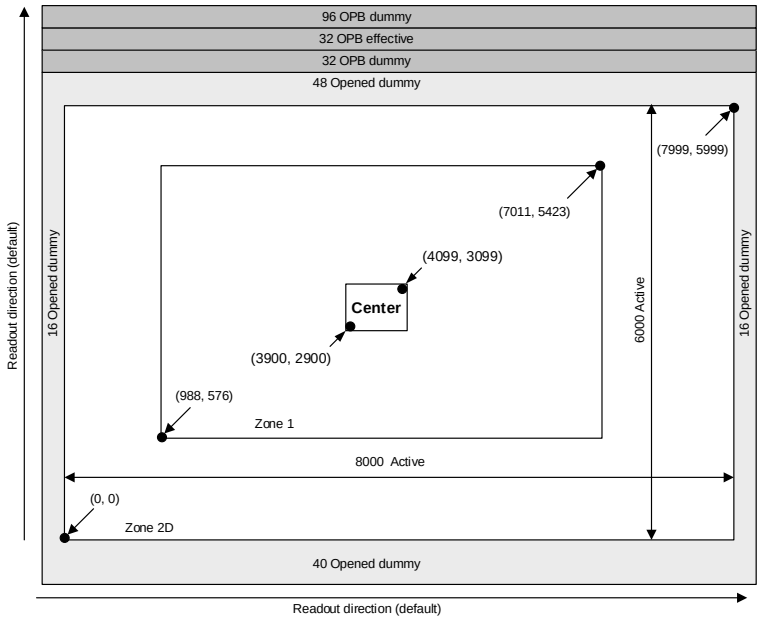


Figure 27 Zone Definition Diagram

11. Measurement Method for Image Sensor Characteristics

11-1 Measurement conditions

The device operation conditions are at the typical values of the bias and clock voltage.

Table 21 Measurement Conditions

Supply voltage	VANA1 2.8V, VANA2 1.8V, VDIG1, 2 1.1V, VIF 1.8V
Clock	INCK 18 MHz

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr, Gb, R and B digital signal outputs of the measurement system.

11-2 Pixel position of This Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.

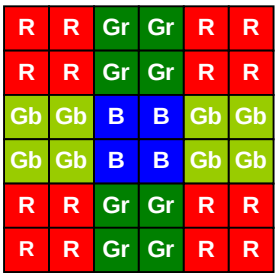


Figure 28 Coding alignment

11-3 Definition of Standard Imaging Conditions

11-3-1 Standard imaging condition I

Use a pattern box (luminance: 706 cd/m2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

11-3-2 Standard imaging condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.

11-4 Measurement method

11-4-1 Sensitivity

Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/75 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of imaging area, and substitute the values into the following formula.

S = {((VGr + VGb) /2) × (75/120)} [LSB]

11-4-2 Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting so that the average value of the Gr and Gb signal output is TBD [LSB], measure the R signal output (VR [LSB]), the Gr and Gb signal outputs (VGr, VGb [LSB]) and the B signal output (VB [LSB]) at the imaging area Center in frame readout mode, and substitute the values into the following formulas.

VG = (VGr + VGb) /2

RG = VR/VG

RB = VB/VG

11-4-3 Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous Intensity to 20 times the intensity with the average value of the Gr, Gb signal outputs, TBD [LSB], measure the average value of the Gr, Gb, R and B signal outputs.

11-4-4 Video signal shading

Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is TBD [LSB]. Then measure the maximum value (Gmax [LSB]) and minimum value (Gmin [LSB]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

SH = ((Gmax –Gmin) /Gmax) × 100 [%]

11-4-5 Dark signal

Measure the output difference between 1/15 [s] signal output (Va) and 1/15000 or less [s] signal output (Vb) at the device ambient temperature of 60 ˚C and the device in the light-obstructed state, and calculate the signal output at 1/15 [s] storage by them using the following approximate formula. Then, this is Vdt [LSB].

Vdt = (Va – Vb) × (1/15) / (1/15) – (1/15000) ≈ (Va –Vb) [LSB]

12. Spot Pixel Specification(TENTATIVE)

Table 22 Spot Pixel Specifications

(Full size@30 frame/s, V_{ANA1} = 2.8V, V_{ANA2} = 1.8V, $V_{DIG1,2}$ = 1.1 V, V_{IF} = 1.8 V, Tj = 60 ˚C)

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone		Measurement method	Remarks
		Zone2D	Other		
Black or white pixels at high light	30 % ≤ D	TBD	No evaluation criteria applied	12-3-1	
White pixels in the dark	28 (LSB) ≤ D	TBD	No evaluation criteria applied	12-3-2	1/30 storage Note 2)

Note) 1. D...Spot pixel level.
2. Continuous same color pixels in the horizontal or vertical direction are NG.
3. Defect pixels are measured with all optional image processing features (DPC, LSC) disabled.
4. The maximum quantity pixel counts of 200 for Bright Pixels and 3040 for Dark Pixels are total of R + Gr + Gb + B individual pixels from any colour channels.
5. The analog gain for both the Illuminated and Dark defect conditions is 0dB.
7. The above chart (hereinafter referred to as the “Spot Pixel Specifications”) is the standard only for sorting image sensor products in this specification book (hereinafter referred to as the “PRODUCTS”) before shipment from a manufacturing factory. Sony Semiconductor Solutions Corporation and its distributors (collectively hereinafter referred to as the “Seller”) disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the Spot Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the “Program”), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.

12-1 Notice on White Pixels Specifications(TENTATIVE)

After shipment inspection of CMOS image sensors, pixels of CMOS image sensors may be distorted and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels.")
Particle radiation such as cosmic rays etc. is one of the causes of White Pixels.
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such distorted pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against White Pixels, such as adoption of automatic compensation systems for White Pixels and establishment of quality assurance standards.
White Pixels may be also caused by alpha radiation, which will be emitted in a process of decay of radioactive isotopes which inevitably exist in the air in minute amounts and may exist in materials or parts of CMOS image sensor devices (e.g. packaging materials, seal glass, wiring materials and IC chips). It is recommended that you should use materials or parts which do not include radioactive isotopes, which are sources of alpha radiation, and consider taking measures, such as adoption of vacuum packaging technologies in order to ensure that the PRODUCTS are not exposed to the air. As the density of radioactive isotopes in the air of the underground space may become thicker than that on the ground, it is highly recommended to ensure the PRODUCTS are not exposed to the air in using or storing the PRODUCTS at the underground space.

[For Your Reference]

The Annual number of White Pixels Occurrence Caused by Particle Radiation such as cosmic rays etc.

The data in the below chart shows the estimated annual number of White Pixels occurrence caused by particle radiation such as cosmic rays etc. in a single-story building in Tokyo at an altitude of 0 meters. The data shows estimated number of White Pixels based on records of past field tests calculated taking structures and electrical properties of each device into account. However, the data in the chart is for your reference purpose only, and shall not be construed as part of any CMOS image sensor product specifications which the Seller warrants.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
TBD LSB or higher	TBD pcs
TBD LSB or higher	TBD pcs
TBD LSB or higher	TBD pcs
TBD LSB or higher	TBD pcs
TBD LSB or higher	TBD pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the annual number of White Pixels occurrence.

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12-2 Measurement Method for Spot Pixels

Measure under the standard imaging condition II.

12-3 Spot Pixel Pattern Specifications

12-3-1 Black or white pixels at high light

After adjusting the average value of the Gr/Gb signal output to TBD LSB, measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the Gr/Gb/R/B signal output Vx (x = Gr/Gb/R/B), and substitute the values into the following formula.
The TBD LSB does not include the dark level offset of 64. The average value is calculated using the signal level output of Zone 2D.

$$D_K(\text{White Pixel level}) = (V_{XK} / \overline{V_X}) \times 100\ [\%]$$

$$D_B(\text{Black Pixel level}) = (V_{XB} / \overline{V_X}) \times 100\ [\%]$$

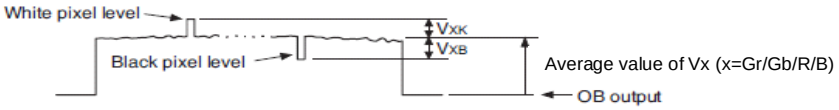

Figure 29 Measurement Method for Spot Pixels

12-3-2 White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

13. CRA Characteristics of Recommended Lens

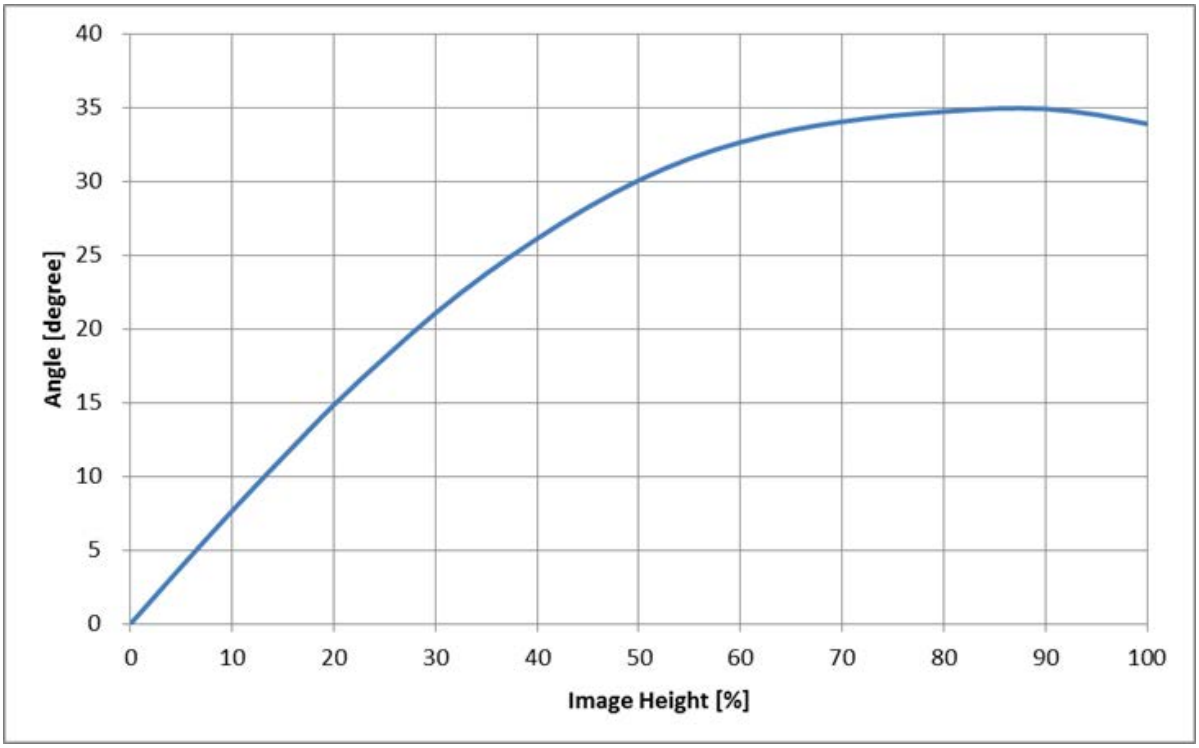

Figure 30 CRA characteristics

14. Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

(1) Perform all work in a clean environment.
(2) Do not touch the chip surface with hand and make any object contact with it.
(3) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

3. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Reliability assurance of this product should be ignored because it is a bare chip.
(5) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(6) Note that X-ray inspection may damage characteristics of the sensor.
(7) Note that the sensor may be damaged when using ultraviolet ray and infrared ray on mounting it.
(8) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

15. Notes on Handling (Additional items concerning bare chip mounting of stacked-type CMOS image sensors)

Collet contact is allowed in areas other than the pixel area, bonding pads, scribe area, and chip edge. Contact with areas other than the contact-allowed area may result in problems such as dust emission or electrostatic breakdown.

Collet contact-prohibited areas

- Pixel area: Abnormal images
- Bonding pad: Circuit electrostatic breakdown
  (Please note that this rule is not applicable for electrostatic breakdown prevention areas.)
- Scribe area: Dust emission due to chipping
- Chip edge: Dust emission due to chip breakage

Note: Ensure sufficient positional accuracy during the pickup work.
Separate the collet contact surfaces and contact-prohibited areas as much as possible.

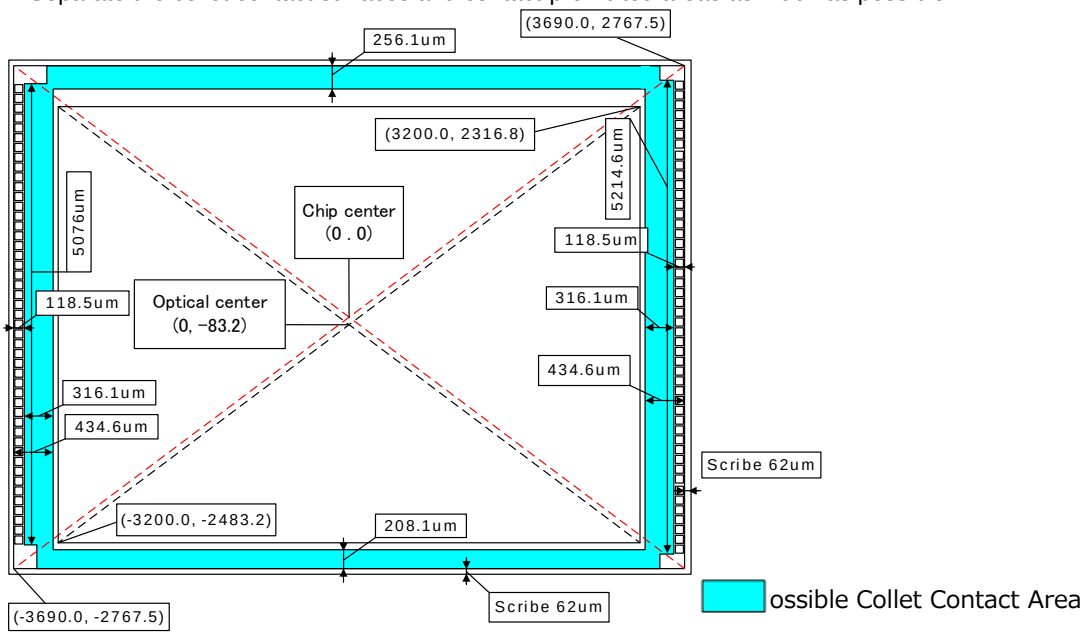

Figure 31 Prohibited Area

Ultrasonic chip cleaning is prohibited.
This may result in dust emission from cut surfaces.

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16. Open Source Software License