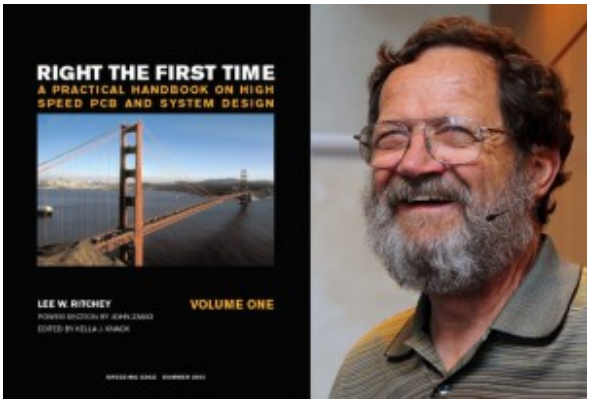
Copper Thieving Confusion

The good Lee Ritchey is spitting out a series of very useful posts on the SI-LIST (highly recommended mailing list if you are into signal integrity). Here is another one to clear up the confusion about copper thieving. To preserve it in this context, here is the important stuff:



> Thieving is copper added to outer layers of a PCB to create a uniform distribution of copper across the surface. The reason this is done is to make sure the copper plating in the holes is uniform. If the copper distribution in the artwork is not uniform, areas with little exposed copper will plate very heavy while areas with large amounts of copper, such as BGAs or connector pin fields will not plate properly. So, "thieving" steals some of the plating current that would otherwise concentrate on features that are sparse and be spread thin in areas with areas that are dense with features.
>
> Thieving is an **outer layer only process**. All of the discussions that mention doing things to inner layers are not thieving. They are signal layer fills to even out the resin flow from the prepreg. I have designed thousands of complex PCBs with many signal layers in each one and have never encountered a stackup that required inner layer signal layer fill to achieve a usable, flat PCB.
>
> When a fabricator is allowed to add thieving to outer layers, one only need to keep it away from other features on that layer to comply with

> typical spacing standards and away from traces enough that it does not adversely affect impedance. If the next layer down is a plane layer, that is all that is needed. If the next layer down is a signal layer (buried microstrip) thieving should not be placed over traces in the buried layer.

If you noticed it, the other common misconception that Lee clears up here is on "copper balancing" to avoid warped boards. **There is no need to balance copper on a PCB today**. Period.

Update 19/12-14:

I noticed someone having trouble understanding this and a friendly profile "Anne C" added this, which I find is a good supplementary explanation:

> The manufacturing process for PCBs will require a given type of plating. This is done by a a chemical process involving electric current to plate the bare copper traces. To help have a uniform current from your copper masses (trace, donuts, pads) to the plating solutions, it is better to have a uniform copper coverage, throughout your PCB. If this is not done, current will flow more in areas of your PCB that is busy with copper and less where it is not, throwing out of balance the migration of plating chemical to those copper features. The main problem it creates is a target quality of the plating on vias. When a PCB goes through the multistage oven to reflow the solder paste, bad quality vias may pop and fail. This failure mode occurs at the end of the assembly process and costs a lot in rework costs.

Thanks "Anne C" – whoever you are

Share this:

Email Print Facebook Twitter More

About Rolf Ostergaard

Rolf V. Ostergaard, M.Sc.EE. has worked with signal integrity in many different projects since working for 3Com in 1998 as a colleague to Lee Ritchey in Silicon Valley. While building a consulting business focused on advanced electronics and embedded software in Denmark, Rolf has been helping numerous companies with signal integrity and power integrity both as design, simulations, coaching, measurements and troubleshooting. He started conducting training in SI around 2004 and has trained hundreds of engineers, which lead to founding EE-Training to further expand this.
You can hire Rolf to do signal integrity training and consulting world wide and remote.

Comments

m.senthil says
March 13, 2014 at 17:42

Copper thieving is added for proper stability of board.

Reply

Rolf Ostergaard says
March 13, 2014 at 18:11

Mechanical reasons you say? Can you point to a source or reference for this information?

Reply