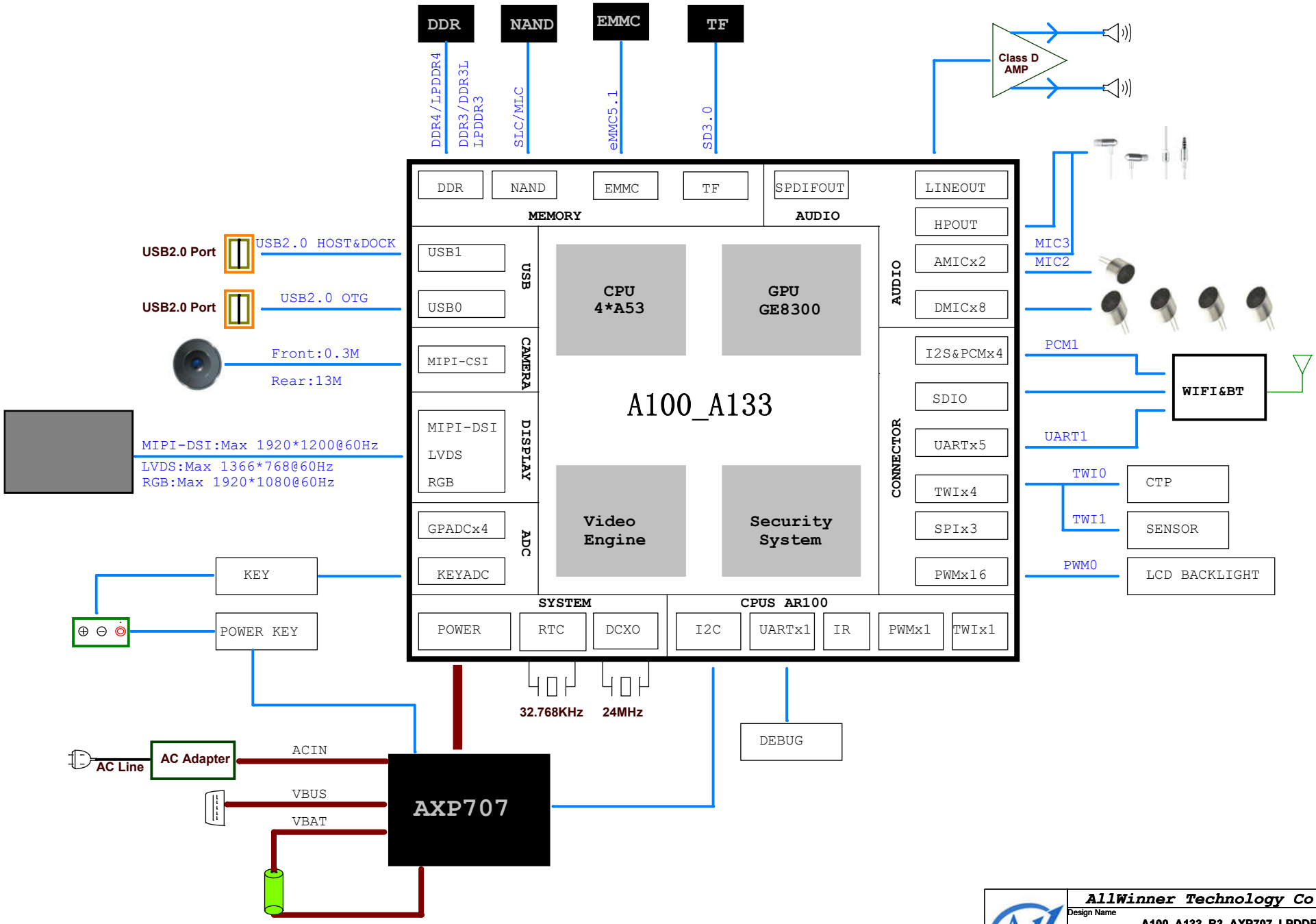
VERSION HISTORY

Index:

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Release version	2020-03-12			
Ver 1.1	1、P03 page , Instructions for modifying Power Tree. 2、Update A100 symbol,and modify A100 description as A100_A133. 3、P10 page, Modify the group value of power amplifier feedback resistors R22 and R24 to 100K. 4、P13 page ,Modify R53 resistance value to 1.8K. 5、Delete AC101 design,and delet R97/R108. 6、Delete the description of the camera module about the I2C design。	2020-06-28			

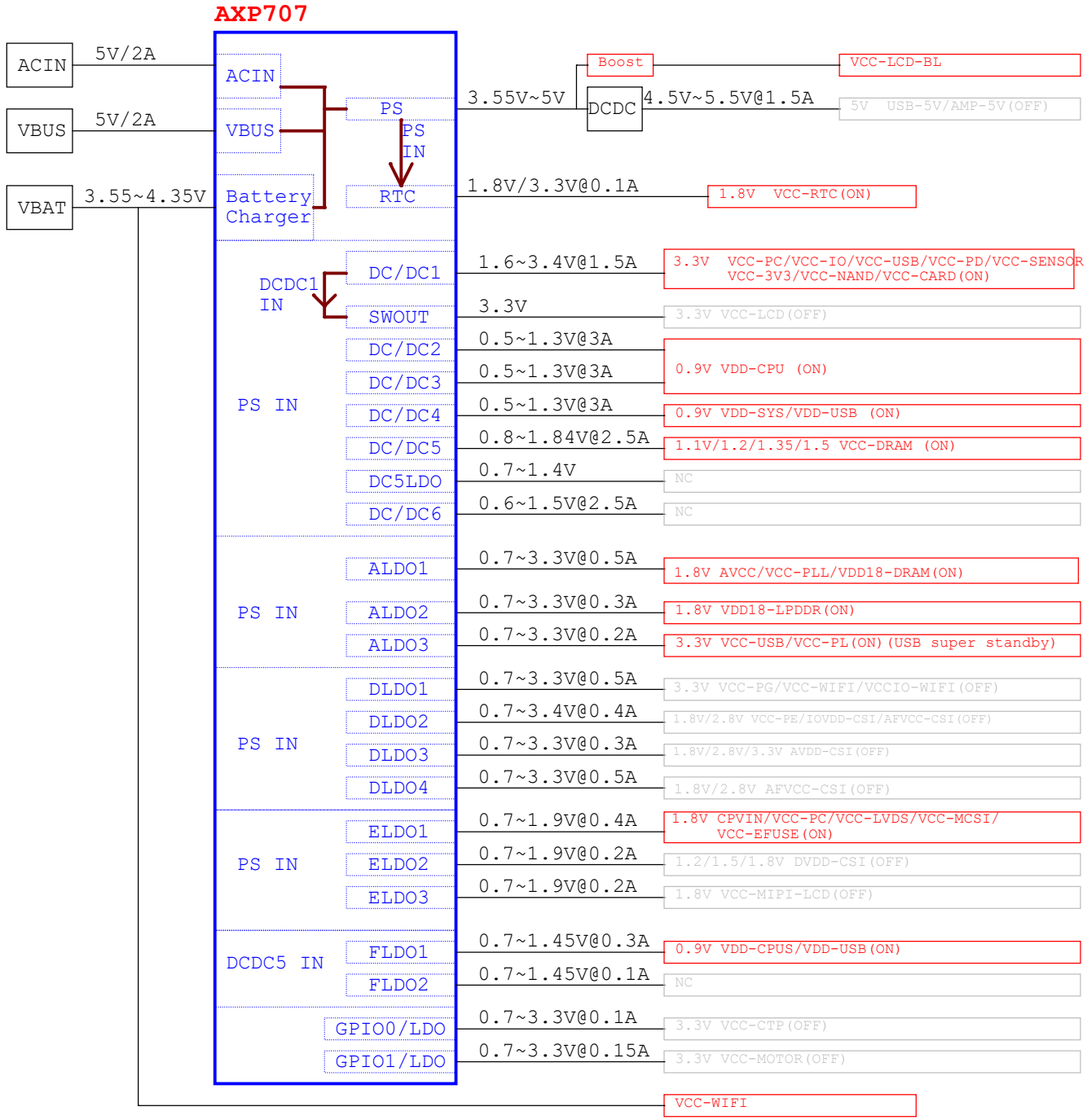
BLOCK



AllWinner Technology Co.,Ltd		
Design Name: A100_A133_B3_AXP707_LPDDR3		
Size: A3	Page Name: 02 BLOCK DIAGRAM	Rev
Date: Thursday, September 09, 2021	Sheet 2 of 18	

DEFAULT POWER ON

DEFAULT POWER OFF



AllWinner Technology Co.,Ltd			
Design Name: A100_A133_B3_AXP707_LPDDR3			
Size: A3	Page Name: 03 POWER TREE		Rev
Date: Thursday, September 09, 2021	Sheet 3 of 18		

GPIO ASSIGNMENT

PIN	Define	CFG	Function
PB0	CPUX_TMS	4	DEBUG
PB1	CPUX_TCK	4	
PB2	CPUX_TDO	4	
PB3	CPUX_TDI	4	
PB4		3	GPIO
PB5		3	
PB6		3	
PB7		3	
PB8	LCD-BL-EN	3	
PB9	CPUX_TX	2	DEBUG
PB10	CPUX_RX	2	

PIN	Define	CFG	Function
PE0	MCSI_MCLK	2	CSI
PE1	MCSI_SCK	2	
PE2	MCSI_SDA	2	
PE3			
PE4			
PE5			
PE6	MCSIB_STBY_F	1	
PE7	MCSIB_RST_F	1	
PE8	MCSIA_STBY_R	1	
PE9	MCSIA_RST_R	1	

PIN	Define	CFG	Function
PH0	TWI0_SCK	2	TWI
PH1	TWI0_SDA	2	
PH2	TWI1_SCK	2	
PH3	TWI1_SDA	2	
PH4	PS-EINT	1	GPIO
PH5			
PH6	PA_SHDN	0	
PH7			
PH8	USB0_ID_SOC	0	
PH9	CTP_INT	0	
PH10	CTP_RST	1	
PH11	GS-INT	0	
PH12			
PH13			
PH14			
PH15			
PH16			
PH17			
PH18			
PH19			

PIN	Define	CFG	Function
PC0	NAND_WE/SDC2_DS	2/3	NAND/eMMC
PC1	NAND_ALE/SDC2_RST	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE1	2	
PC4	NAND_CE0	2	
PC5	NAND_RE/SDC2_CLK	2/3	
PC6	NAND_RB0/SDC2_CMD	2/3	
PC7	NAND_RB1	2	
PC8	NAND_DQ7/SDC2_D3	2/3	
PC9	NAND_DQ6/SDC2_D4	2/3	
PC10	NAND_DQ5/SDC2_D0	2/3	
PC11	NAND_DQ4/SDC2_D5	2/3	
PC12	NAND_DQS	2	
PC13	NAND_DQ3/SDC2_D1	2/3	
PC14	NAND_DQ2/SDC2_D6	2/3	
PC15	NAND_DQ1/SDC2_D2	2/3	
PC16	NAND_DQ0/SDC2_D7	2/3	

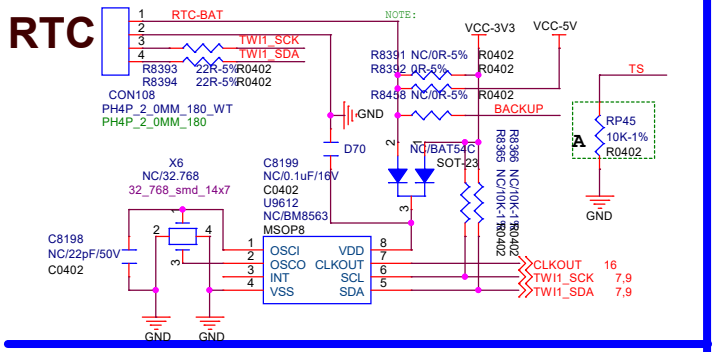
PIN	Define	CFG	Function
PF0	SDC0_D1	2	CARD
PF1	SDC0_D0	2	
PF2	SDC0_CLK	2	
PF3	SDC0_CMD	2	
PF4	SDC0_D3	2	
PF5	SDC0_D2	2	
PF6	SDC0_DET	0	

PIN	Define	CFG	Function
PL0	PMU_SCK	2	CPUS
PL1	PMU_SDA	2	
PL2	BT_RST_N	1	
PL3	BT_WAKE_AP	0	
PL4	AP_WAKE_BT	1	
PL5	WL_PMU_EN	1	
PL6	WL_WAKE_AP	0	
PL7	CPUS-TDI	2	
PL8	USB1-DRVVBUS	1	
PL9	EINT-HAL	0	
PL10	KD-EINT	0	
PL11	LED-EN	1	

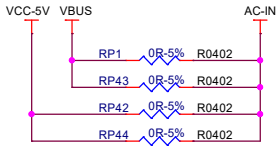
PIN	Define	CFG	Function
PD0	LCD_D2	2	LCD
PD1	LCD_D3	2	
PD2	LCD_D4	2	
PD3	LCD_D5	2	
PD4	LCD_D6	2	
PD5	LCD_D7	2	
PD6	LCD_D10	2	
PD7	LCD_D11	2	
PD8	LCD_D12	2	
PD9	LCD_D13	2	
PD10			
PD11			
PD12			
PD13			
PD14			
PD15			
PD16			
PD17			
PD18			
PD19			
PD20			
PD21			
PD22	LCD_RST	1	
PD23	LCD_PWM	3	

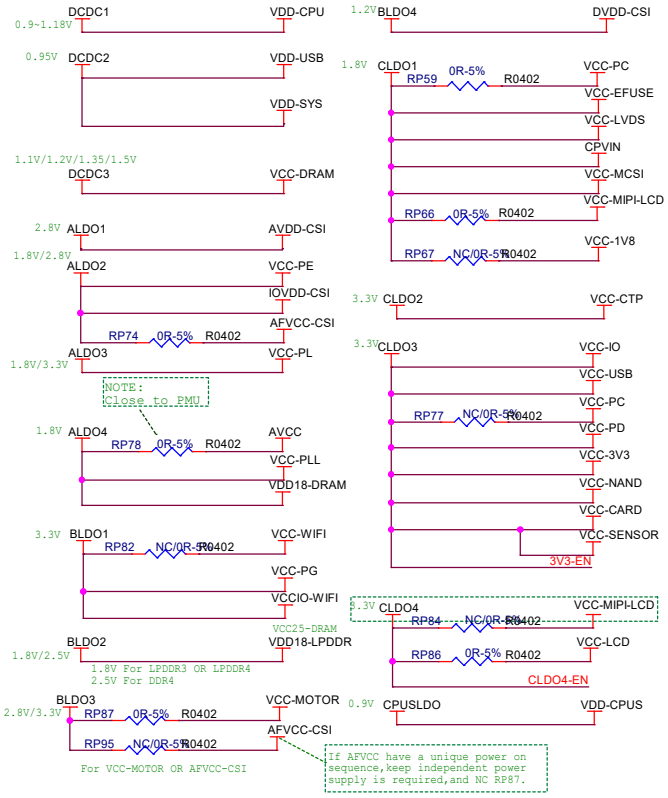
PIN	Define	CFG	Function
PG0	WL_SDIO_CLK	2	WIFI/BT
PG1	WL_SDIO_CMD	2	
PG2	WL_SDIO_D0	2	
PG3	WL_SDIO_D1	2	
PG4	WL_SDIO_D2	2	
PG5	WL_SDIO_D3	2	
PG6	BT_UART_RX	2	
PG7	BT_UART_TX	2	
PG8	BT_UART_CTS	2	
PG9	BT_UART_RTS	2	
PG10	BT_PCM_CLK	3	
PG11	BT_PCM_SYNC	3	
PG12	BT_PCM_DIN	3	
PG13	BT_PCM_DOUT	3	

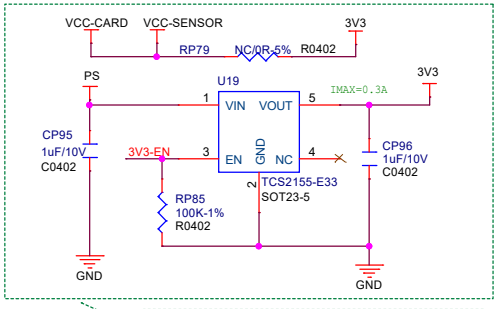
RTC

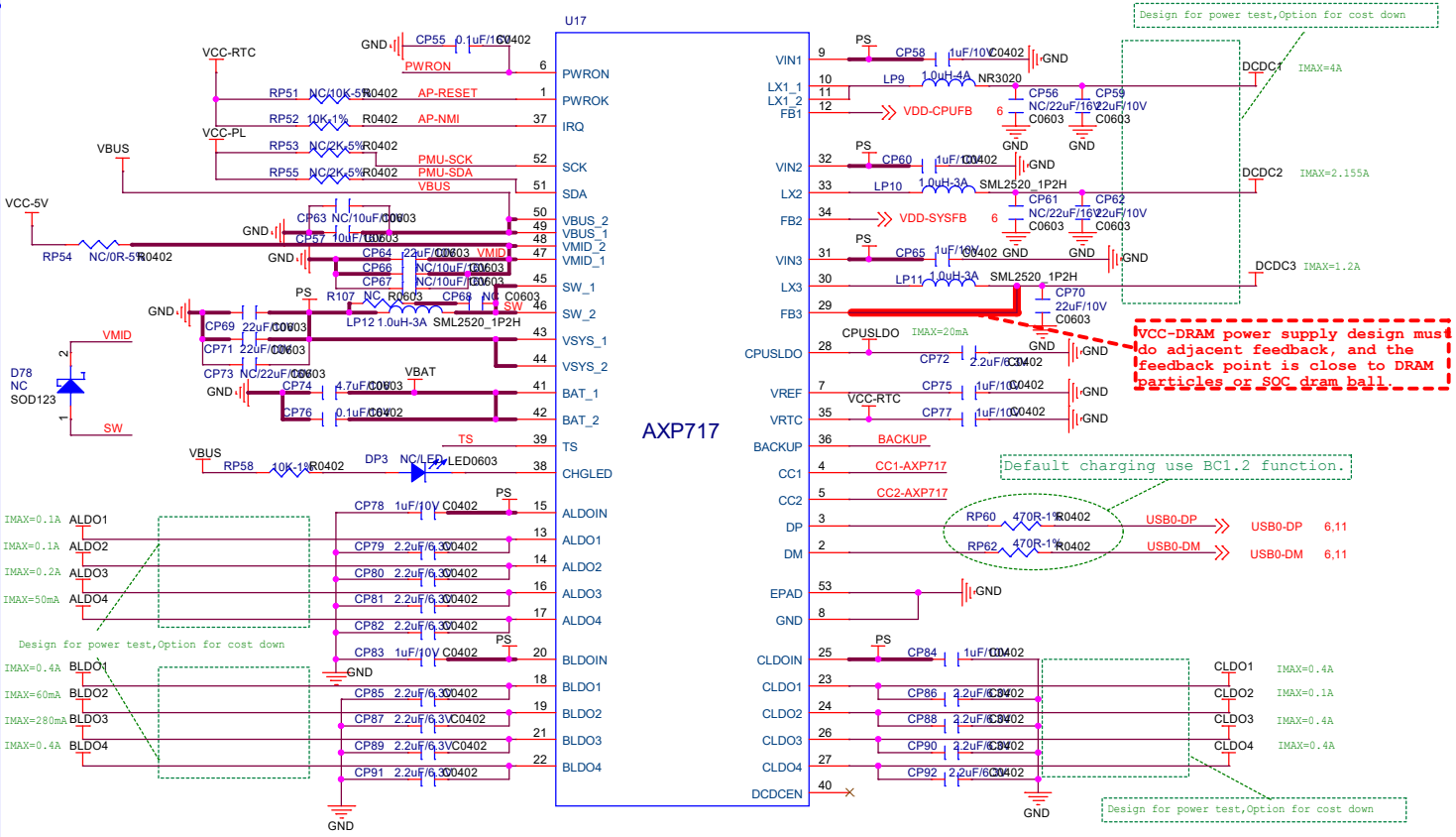


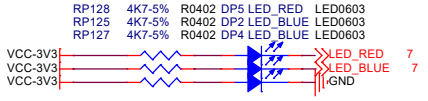
PMIC

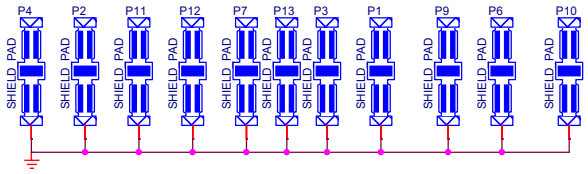




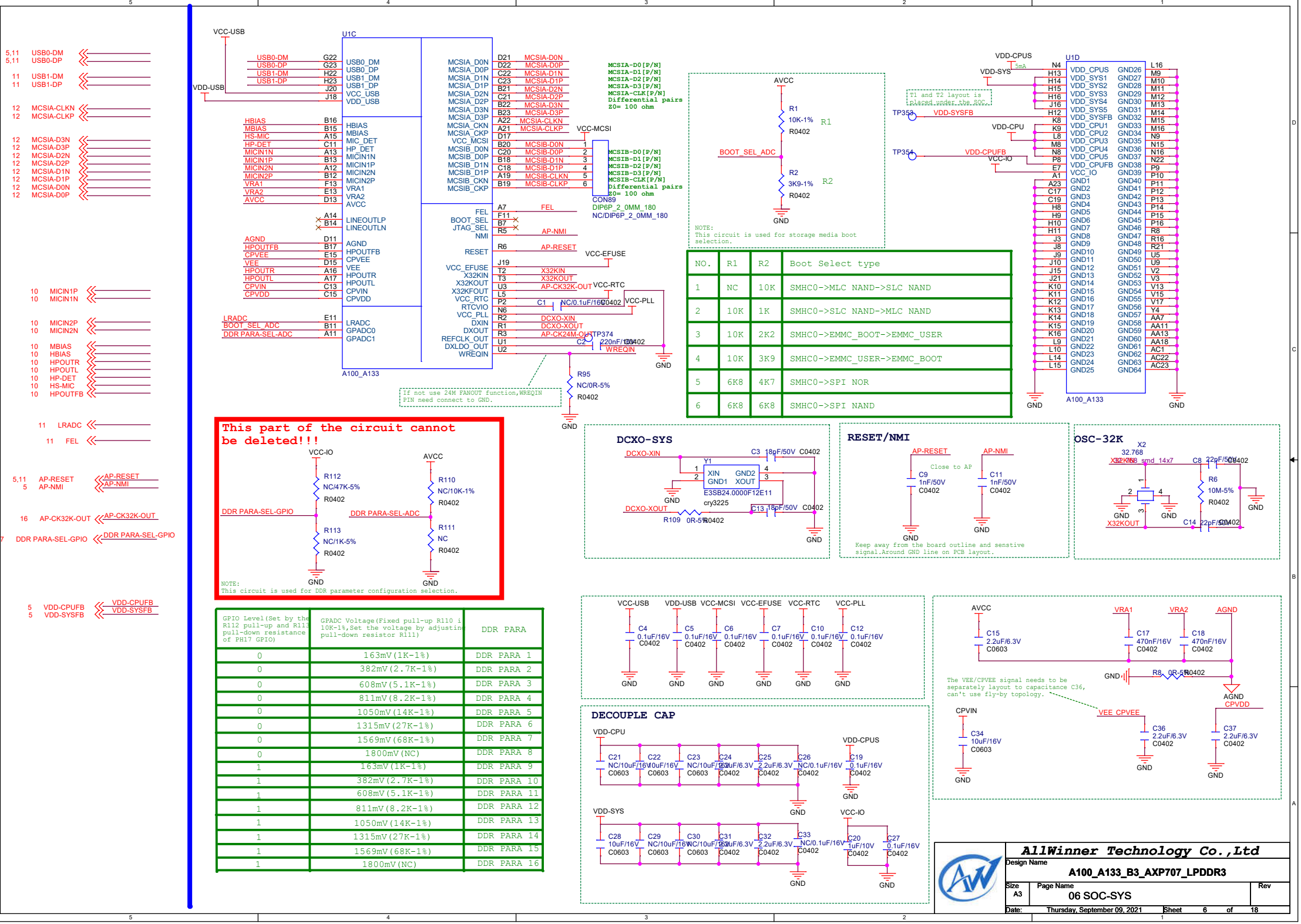








AllWinner Technology Co.,Ltd		
Design Name: A100_A133_B3_AXP707_LPDDR3		
Size: A3	Page Name: 05 AXP707	Rev
Date: Thursday, September 16, 2021	Sheet 5 of 18	



NO.	R1	R2	Boot Select type
1	NC	10K	SMHC0->MLC NAND->SLC NAND
2	10K	1K	SMHC0->SLC NAND->MLC NAND
3	10K	2K2	SMHC0->EMMC_BOOT->EMMC_USER
4	10K	3K9	SMHC0->EMMC_USER->EMMC_BOOT
5	6K8	4K7	SMHC0->SPI NOR
6	6K8	6K8	SMHC0->SPI NAND

This part of the circuit cannot be deleted!!!

GPIO Level(Set by the R112 pull-up and R113 pull-down resistance of PH17 GPIO)	GPADC Voltage(Fixed pull-up R110 is 10K-1%,Set the voltage by adjusting pull-down resistor R111)	DDR PARA
0	163mV(1K-1%)	DDR PARA 1
0	382mV(2.7K-1%)	DDR PARA 2
0	608mV(5.1K-1%)	DDR PARA 3
0	811mV(8.2K-1%)	DDR PARA 4
0	1050mV(14K-1%)	DDR PARA 5
0	1315mV(27K-1%)	DDR PARA 6
0	1569mV(68K-1%)	DDR PARA 7
0	1800mV(NC)	DDR PARA 8
1	163mV(1K-1%)	DDR PARA 9
1	382mV(2.7K-1%)	DDR PARA 10
1	608mV(5.1K-1%)	DDR PARA 11
1	811mV(8.2K-1%)	DDR PARA 12
1	1050mV(14K-1%)	DDR PARA 13
1	1315mV(27K-1%)	DDR PARA 14
1	1569mV(68K-1%)	DDR PARA 15
1	1800mV(NC)	DDR PARA 16

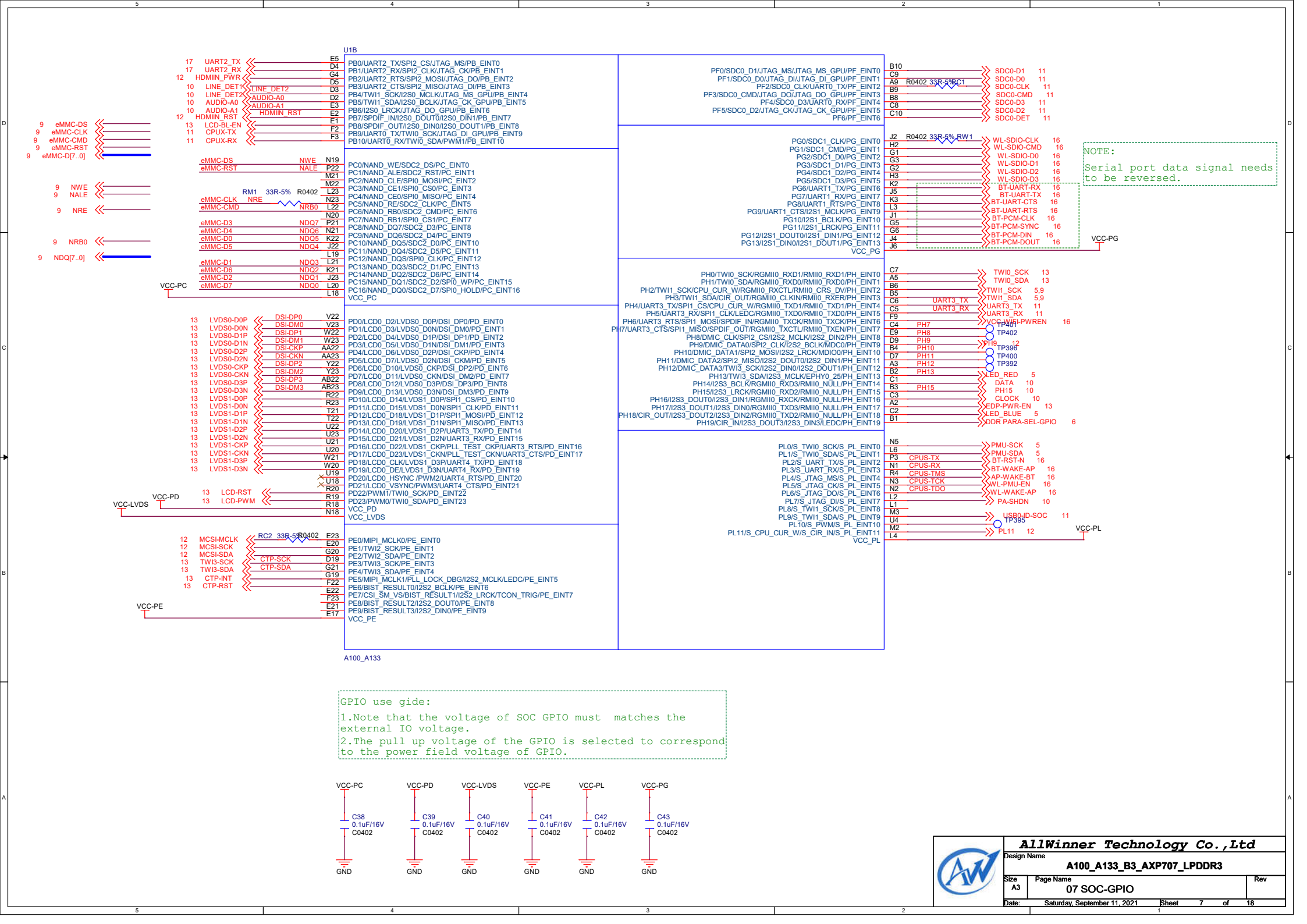
DCXO-SYS

RESET/NMI

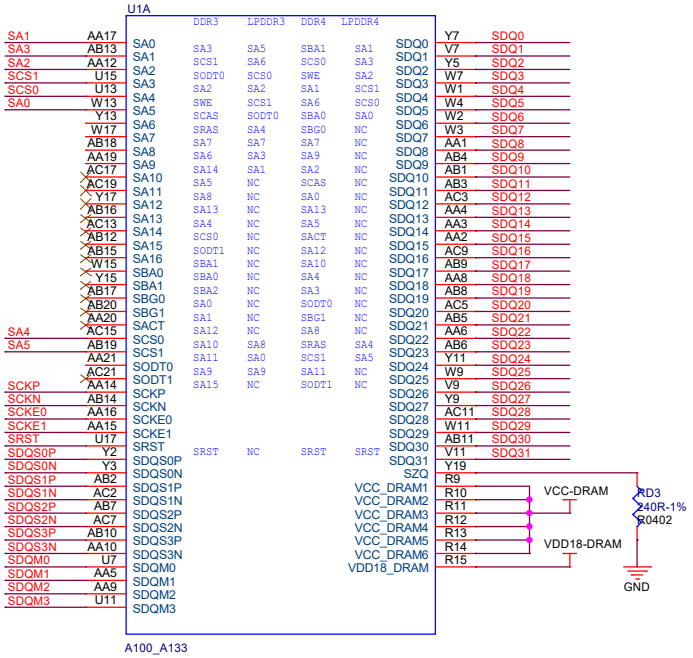
OSC-32K

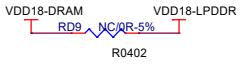
DECOUPLE CAP

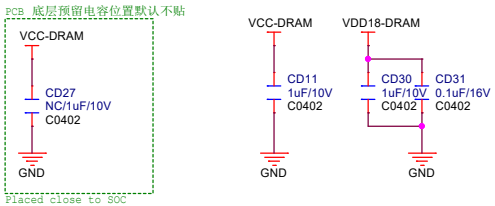
Company	AllWinner Technology Co.,Ltd
Design Name	A100_A133_B3_AXP707_LPDDR3
Size	A3
Page Name	06 SOC-SYS
Rev	
Date:	Thursday, September 09, 2021
Sheet	6 of 18

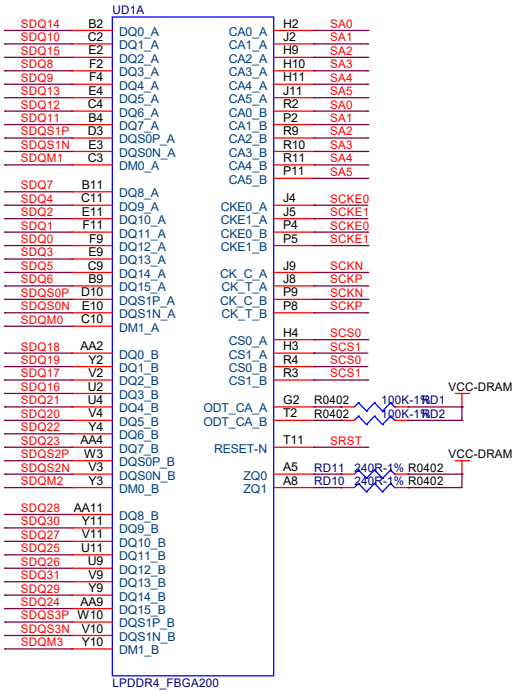

U1B
PB0/UART2_TX/SPI2_CS/JTAG_MS/PB_EINT0
PB1/UART2_RX/SPI2_CLK/JTAG_CK/PB_EINT1
PB2/UART2_RTS/SPI2_MOSI/JTAG_DO/PB_EINT2
PB3/UART2_CTS/SPI2_MISO/JTAG_DI/PB_EINT3
PB4/TWI1_SCK/I2S0_MCLK/JTAG_MS_GPU/PB_EINT4
PB5/TWI1_SDA/I2S0_BCLK/JTAG_CK_GPU/PB_EINT5
PB6/I2S0_LRCK/JTAG_DO_GPU/PB_EINT6
PB7/SPDIF_IN/I2S0_DOUT0/I2S0_DIN1/PB_EINT7
PB8/SPDIF_OUT/I2S0_DIN0/I2S0_DOUT1/PB_EINT8
PB9/UART0_TX/TWI0_SCK/JTAG_DI_GPU/PB_EINT9
PB10/UART0_RX/TWI0_SDA/PWM1/PB_EINT10
PC0/NAND_WE/SDC2_DS/PC_EINT0
PC1/NAND_ALE/SDC2_RST/PC_EINT1
PC2/NAND_CLE/SPI0_MOSI/PC_EINT2
PC3/NAND_CE1/SPI0_CS0/PC_EINT3
PC4/NAND_CE0/SPI0_MISO/PC_EINT4
PC5/NAND_RE/SDC2_CLK/PC_EINT5
PC6/NAND_RB0/SDC2_CMD/PC_EINT6
PC7/NAND_RB1/SPI0_CS1/PC_EINT7
PC8/NAND_DQ7/SDC2_D3/PC_EINT8
PC9/NAND_DQ6/SDC2_D4/PC_EINT9
PC10/NAND_DQ5/SDC2_D0/PC_EINT10
PC11/NAND_DQ4/SDC2_D5/PC_EINT11
PC12/NAND_DQS/SPI0_CLK/PC_EINT12
PC13/NAND_DQ3/SDC2_D1/PC_EINT13
PC14/NAND_DQ2/SDC2_D6/PC_EINT14
PC15/NAND_DQ1/SDC2_D2/SPI0_WP/PC_EINT15
PC16/NAND_DQ0/SDC2_D7/SPI0_HOLD/PC_EINT16
VCC_PC
PD0/LCD0_D2/LVDS0_D0P/DSI_DP0/PD_EINT0
PD1/LCD0_D3/LVDS0_D0N/DSI_DM0/PD_EINT1
PD2/LCD0_D4/LVDS0_D1P/DSI_DP1/PD_EINT2
PD3/LCD0_D5/LVDS0_D1N/DSI_DM1/PD_EINT3
PD4/LCD0_D6/LVDS0_D2P/DSI_CKP/PD_EINT4
PD5/LCD0_D7/LVDS0_D2N/DSI_CKM/PD_EINT5
PD6/LCD0_D10/LVDS0_CKP/DSI_DP2/PD_EINT6
PD7/LCD0_D11/LVDS0_CKN/DSI_DM2/PD_EINT7
PD8/LCD0_D12/LVDS0_D3P/DSI_DP3/PD_EINT8
PD9/LCD0_D13/LVDS0_D3N/DSI_DM3/PD_EINT9
PD10/LCD0_D14/LVDS1_D0P/SPI1_CS/PD_EINT10
PD11/LCD0_D15/LVDS1_D0N/SPI1_CLK/PD_EINT11
PD12/LCD0_D18/LVDS1_D1P/SPI1_MOSI/PD_EINT12
PD13/LCD0_D19/LVDS1_D1N/SPI1_MISO/PD_EINT13
PD14/LCD0_D20/LVDS1_D2P/UART3_TX/PD_EINT14
PD15/LCD0_D21/LVDS1_D2N/UART3_RX/PD_EINT15
PD16/LCD0_D22/LVDS1_CKP/PLL_TEST_CKP/UART3_RTS/PD_EINT16
PD17/LCD0_D23/LVDS1_CKN/PLL_TEST_CKN/UART3_CTS/PD_EINT17
PD18/LCD0_CLK/LVDS1_D3P/UART4_TX/PD_EINT18
PD19/LCD0_DE/LVDS1_D3N/UART4_RX/PD_EINT19
PD20/LCD0_HSYNC /PWM2/UART4_RTS/PD_EINT20
PD21/LCD0_VSYNC/PWM3/UART4_CTS/PD_EINT21
PD22/PWM1/TWI0_SCK/PD_EINT22
PD23/PWM0/TWI0_SDA/PD_EINT23
VCC_PD
VCC_LVDS
PE0/MIPI_MCLK0/PE_EINT0
PE1/TWI2_SCK/PE_EINT1
PE2/TWI2_SDA/PE_EINT2
PE3/TWI3_SCK/PE_EINT3
PE4/TWI3_SDA/PE_EINT4
PE5/MIPI_MCLK1/PLL_LOCK_DBG/I2S2_MCLK/LEDC/PE_EINT5
PE6/BIST_RESULT0/I2S2_BCLK/PE_EINT6
PE7/CSI_SM_VS/BIST_RESULT1/I2S2_LRCK/TCON_TRIG/PE_EINT7
PE8/BIST_RESULT2/I2S2_DOUT0/PE_EINT8
PE9/BIST_RESULT3/I2S2_DIN0/PE_EINT9
VCC_PE
A100_A133
PF0/SDC0_D1/JTAG_MS/JTAG_MS_GPU/PF_EINT0
PF1/SDC0_D0/JTAG_DI/JTAG_DI_GPU/PF_EINT1
PF2/SDC0_CLK/UART0_TX/PF_EINT2
PF3/SDC0_CMD/JTAG_DO/JTAG_DO_GPU/PF_EINT3
PF4/SDC0_D3/UART0_RX/PF_EINT4
PF5/SDC0_D2/JTAG_CK/JTAG_CK_GPU/PF_EINT5
PF6/PF_EINT6
PG0/SDC1_CLK/PG_EINT0
PG1/SDC1_CMD/PG_EINT1
PG2/SDC1_D0/PG_EINT2
PG3/SDC1_D1/PG_EINT3
PG4/SDC1_D2/PG_EINT4
PG5/SDC1_D3/PG_EINT5
PG6/UART1_TX/PG_EINT6
PG7/UART1_RX/PG_EINT7
PG8/UART1_RTS/PG_EINT8
PG9/UART1_CTS/I2S1_MCLK/PG_EINT9
PG10/I2S1_BCLK/PG_EINT10
PG11/I2S1_LRCK/PG_EINT11
PG12/I2S1_DOUT0/I2S1_DIN1/PG_EINT12
PG13/I2S1_DIN0/I2S1_DOUT1/PG_EINT13
VCC_PG
PH0/TWI0_SCK/RGMII0_RXD1/RMII0_RXD1/PH_EINT0
PH1/TWI0_SDA/RGMII0_RXD0/RMII0_RXD0/PH_EINT1
PH2/TWI1_SCK/CPU_CUR_W/RGMII0_RXCTL/RMII0_CRS_DV/PH_EINT2
PH3/TWI1_SDA/CIR_OUT/RGMII0_CLKIN/RMII0_RXER/PH_EINT3
PH4/UART3_TX/SPI1_CS/CPU_CUR_W/RGMII0_TXD1/RMII0_TXD1/PH_EINT4
PH5/UART3_RX/SPI1_CLK/LEDC/RGMII0_TXD0/RMII0_TXD0/PH_EINT5
PH6/UART3_RTS/SPI1_MOSI/SPDIF_IN/RGMII0_TXCK/RMII0_TXCK/PH_EINT6
PH7/UART3_CTS/SPI1_MISO/SPDIF_OUT/RGMII0_TXCTL/RMII0_TXEN/PH_EINT7
PH8/DMIC_CLK/SPI2_CS/I2S2_MCLK/I2S2_DIN2/PH_EINT8
PH9/DMIC_DATA0/SPI2_CLK/I2S2_BCLK/MDC0/PH_EINT9
PH10/DMIC_DATA1/SPI2_MOSI/I2S2_LRCK/MDIO0/PH_EINT10
PH11/DMIC_DATA2/SPI2_MISO/I2S2_DOUT0/I2S2_DIN1/PH_EINT11
PH12/DMIC_DATA3/TWI3_SCK/I2S2_DIN0/I2S2_DOUT1/PH_EINT12
PH13/TWI3_SDA/I2S3_MCLK/EPHY0_25/PH_EINT13
PH14/I2S3_BCLK/RGMII0_RXD3/RMII0_NULL/PH_EINT14
PH15/I2S3_LRCK/RGMII0_RXD2/RMII0_NULL/PH_EINT15
PH16/I2S3_DOUT0/I2S3_DIN1/RGMII0_RXCK/RMII0_NULL/PH_EINT16
PH17/I2S3_DOUT1/I2S3_DIN0/RGMII0_TXD3/RMII0_NULL/PH_EINT17
PH18/CIR_OUT/I2S3_DOUT2/I2S3_DIN2/RGMII0_TXD2/RMII0_NULL/PH_EINT18
PH19/CIR_IN/I2S3_DOUT3/I2S3_DIN3/LEDC/PH_EINT19
PL0/S_TWI0_SCK/S_PL_EINT0
PL1/S_TWI0_SDA/S_PL_EINT1
PL2/S_UART_TX/S_PL_EINT2
PL3/S_UART_RX/S_PL_EINT3
PL4/S_JTAG_MS/S_PL_EINT4
PL5/S_JTAG_CK/S_PL_EINT5
PL6/S_JTAG_DO/S_PL_EINT6
PL7/S_JTAG_DI/S_PL_EINT7
PL8/S_TWI1_SCK/S_PL_EINT8
PL9/S_TWI1_SDA/S_PL_EINT9
PL10/S_PWM/S_PL_EINT10
PL11/S_CPU_CUR_W/S_CIR_IN/S_PL_EINT11
VCC_PL
R0402 33R-5%
RM1 33R-5% R0402
RC2 33R-5% R0402
NOTE:
Serial port data signal needs to be reversed.
GPIO use gide:
1.Note that the voltage of SOC GPIO must matches the external IO voltage.
2.The pull up voltage of the GPIO is selected to correspond to the power field voltage of GPIO.
C38 0.1uF/16V C0402
C39 0.1uF/16V C0402
C40 0.1uF/16V C0402
C41 0.1uF/16V C0402
C42 0.1uF/16V C0402
C43 0.1uF/16V C0402
GND
AllWinner Technology Co.,Ltd
Design Name
A100_A133_B3_AXP707_LPDDR3
Size
A3
Page Name
07 SOC-GPIO
Rev
Date: Saturday, September 11, 2021
Sheet 7 of 18

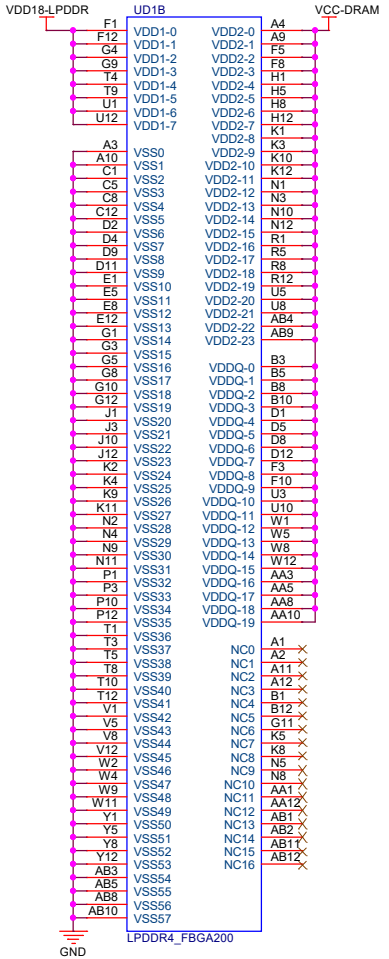
LPDDR4

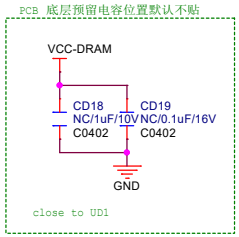












AllWinner Technology Co.,Ltd		
Design Name: A100_A133_B3_AXP707_LPDDR3		
Size: A3	Page Name: 08 LDDR3	Rev
Date: Thursday, September 09, 2021	Sheet 8 of 18	

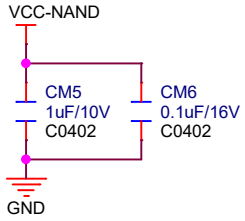
EMMC

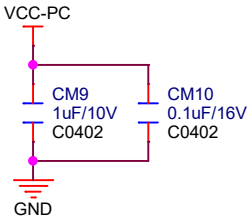
7 eMMC-DS
7 eMMC-CLK
7 eMMC-CMD
7 eMMC-RST
7 eMMC-D[7..0]

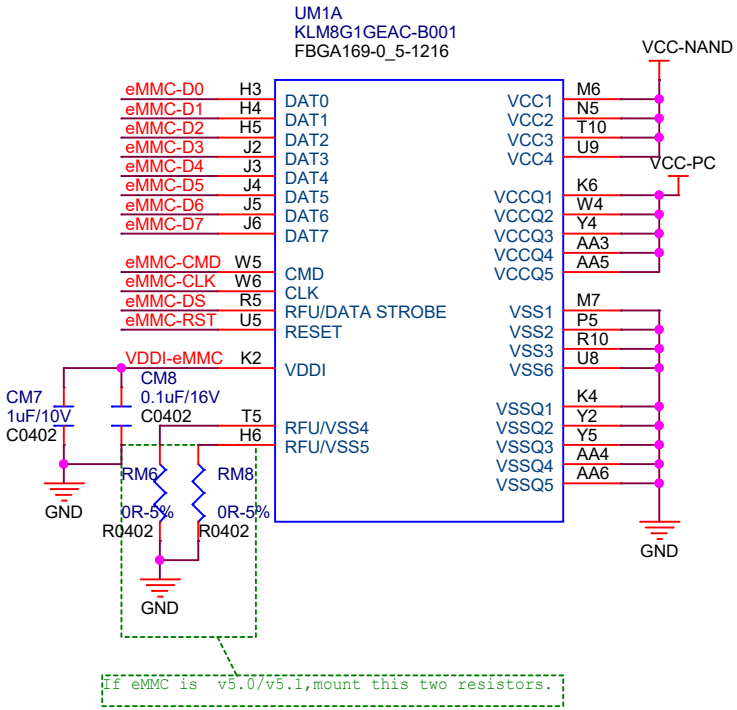
7 NWE
7 NALE
7 NRE
7 NRB0
7 NDQ[7..0]

VCC-NAND 50mA

VCC-PC 100mA

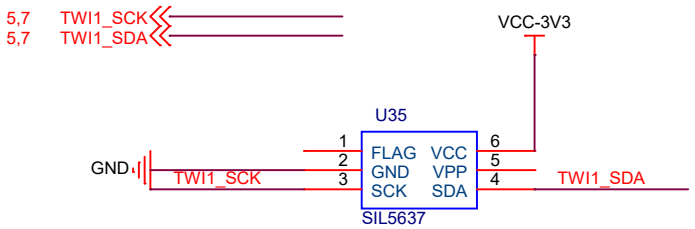


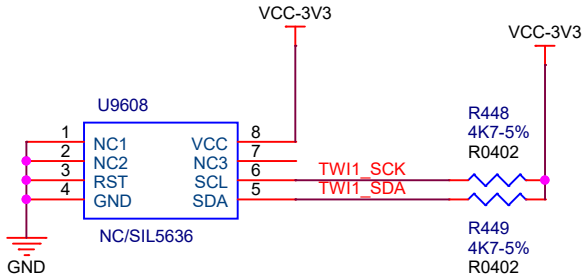


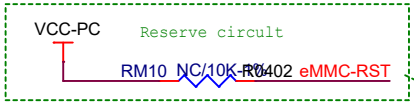


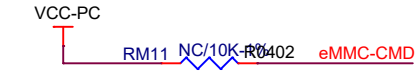
If eMMC is v5.0/v5.1,mount this two resistors.

加密 双LAYOUT

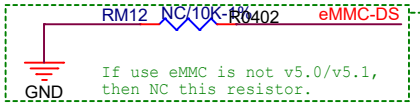






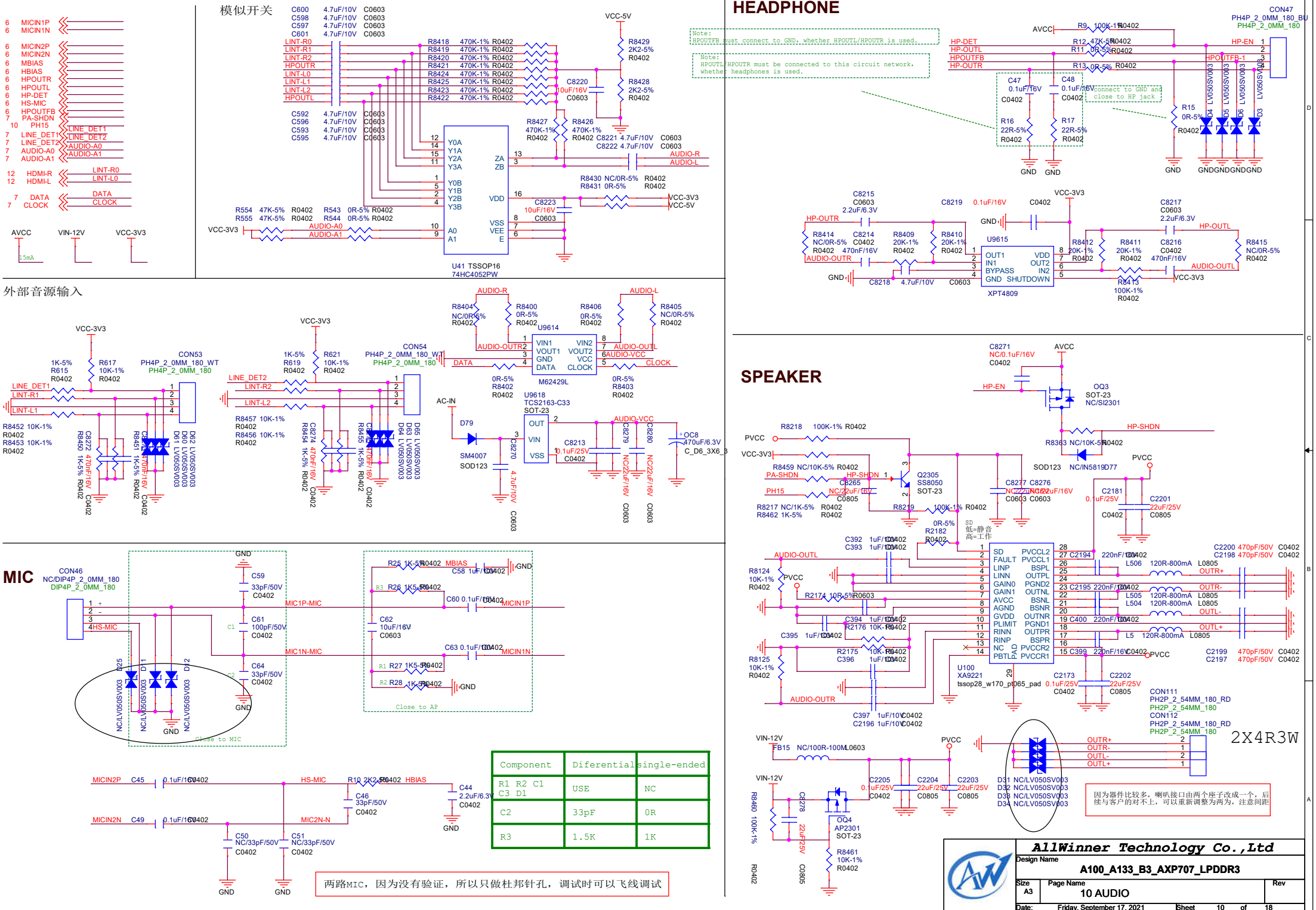


NOTE: eMMC-RST and eMMC-CMD signals are internally pulled up in the SOC, RM10 and RM11 can cost down.



NOTE: eMMC-DS signals are internally pulled down in the SOC, RM12 can cost down.

AllWinner Technology Co.,Ltd		
Design Name: A100_A133_B3_AXP707_LPDDR3		
Size: A4	Page Name: 09 NAND/EMMC	Rev
Date: Thursday, September 09, 2021	Sheet 9 of 18	



Component	Diferential	single-ended
R1 R2 C1 C3 D1	USE	NC
C2	33pF	0R
R3	1.5K	1K

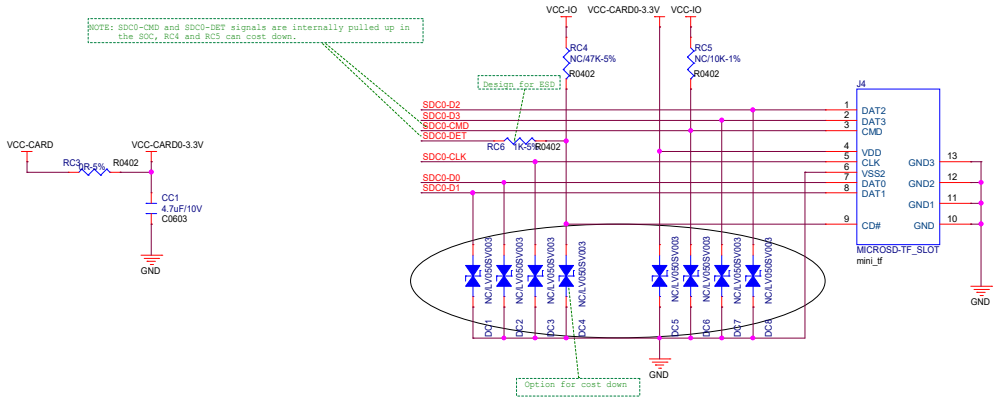
AllWinner Technology Co.,Ltd

Design Name: A100_A133_B3_AXP707_LPDDR3

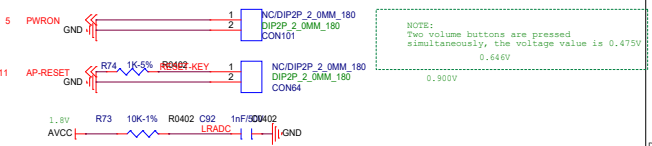
Size: A3 | Page Name: 10 AUDIO | Rev:

Date: Friday, September 17, 2021 | Sheet 10 of 18

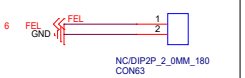
SD CARD



KEY

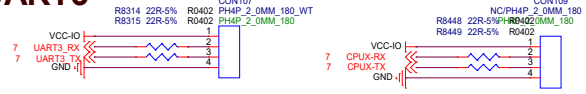


UBOOT

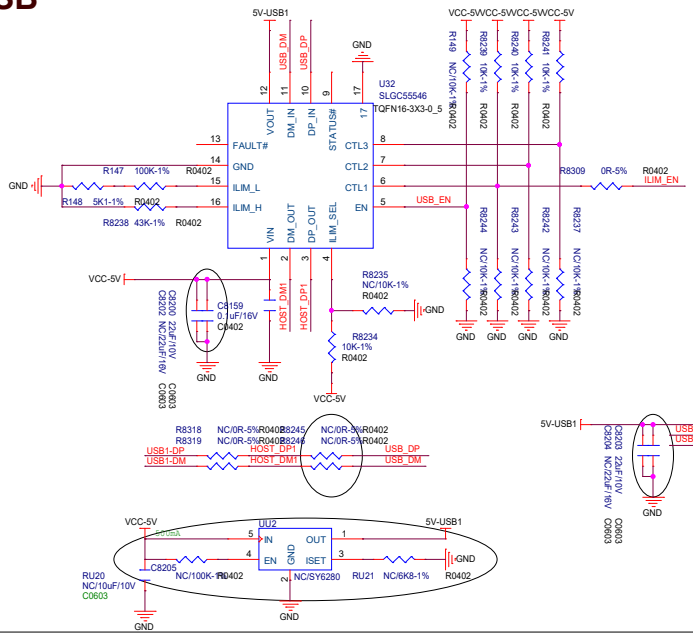


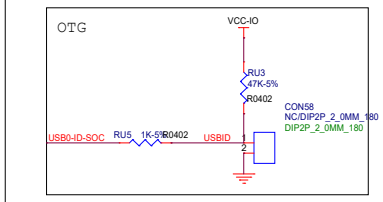
DBUG-UART

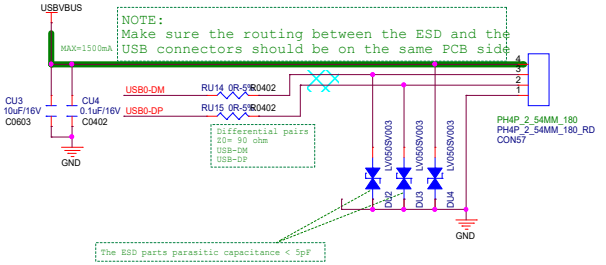
UART3

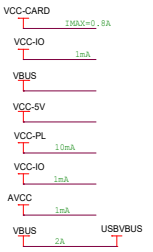


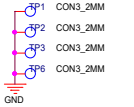
USB

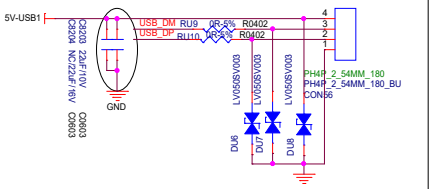


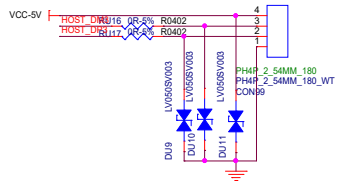


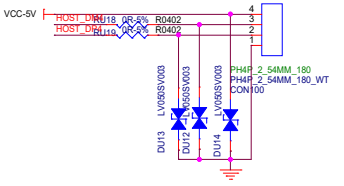


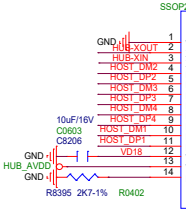


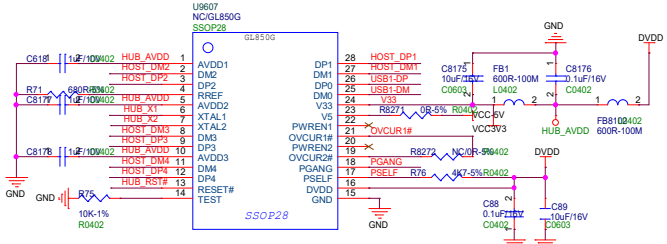


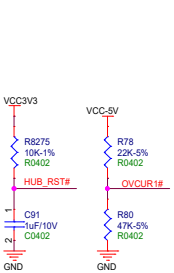


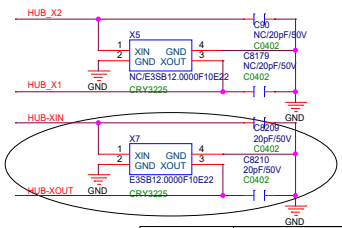


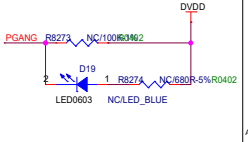




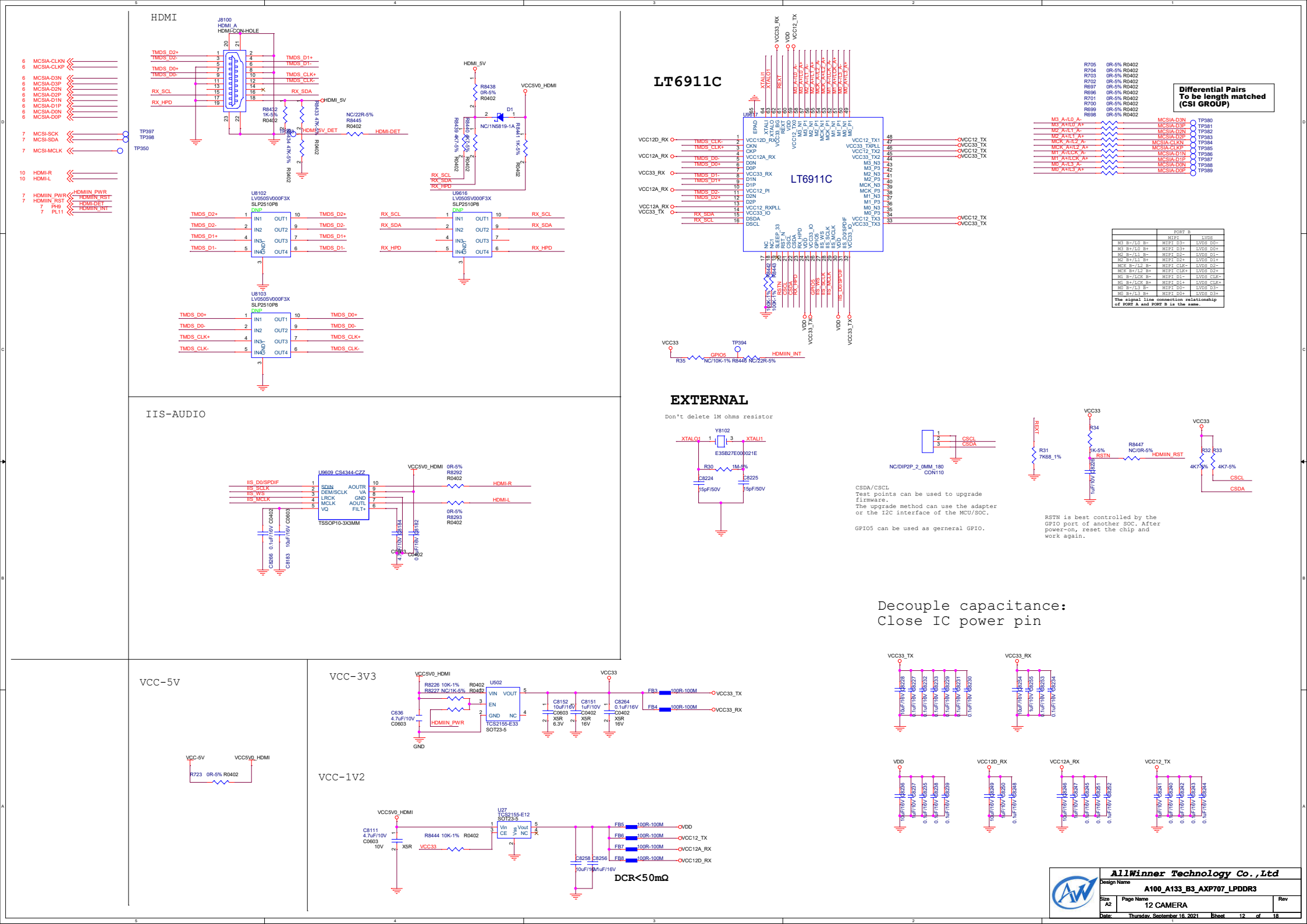








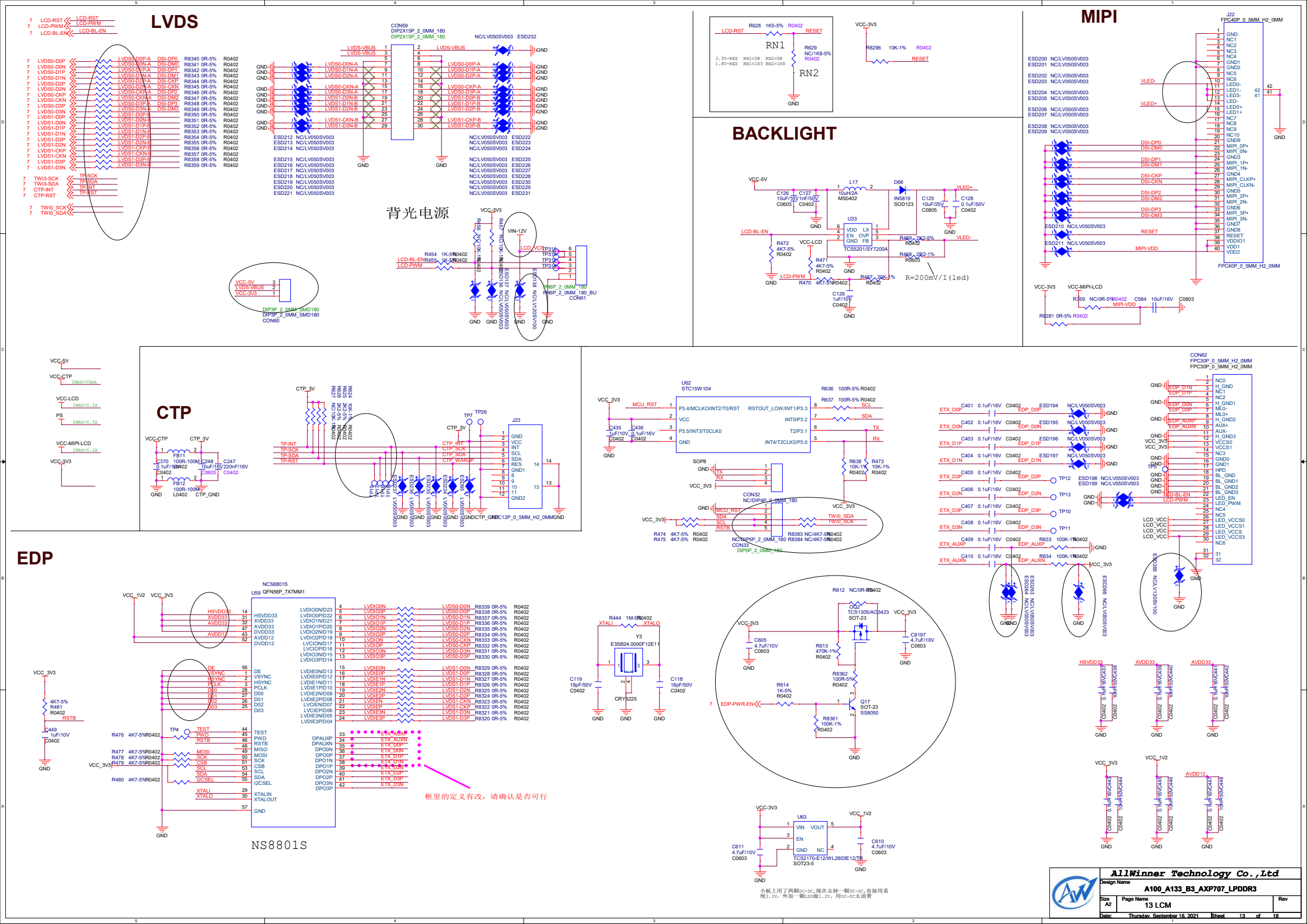
AllWinner Technology Co.,Ltd			
Design Name: A100_A133_B3_AXP707_LPDDR3			
Size: C	Page Name: 11 USB/CARD		Rev
Date: Thursday, September 16, 2021	Sheet 11 of 18		

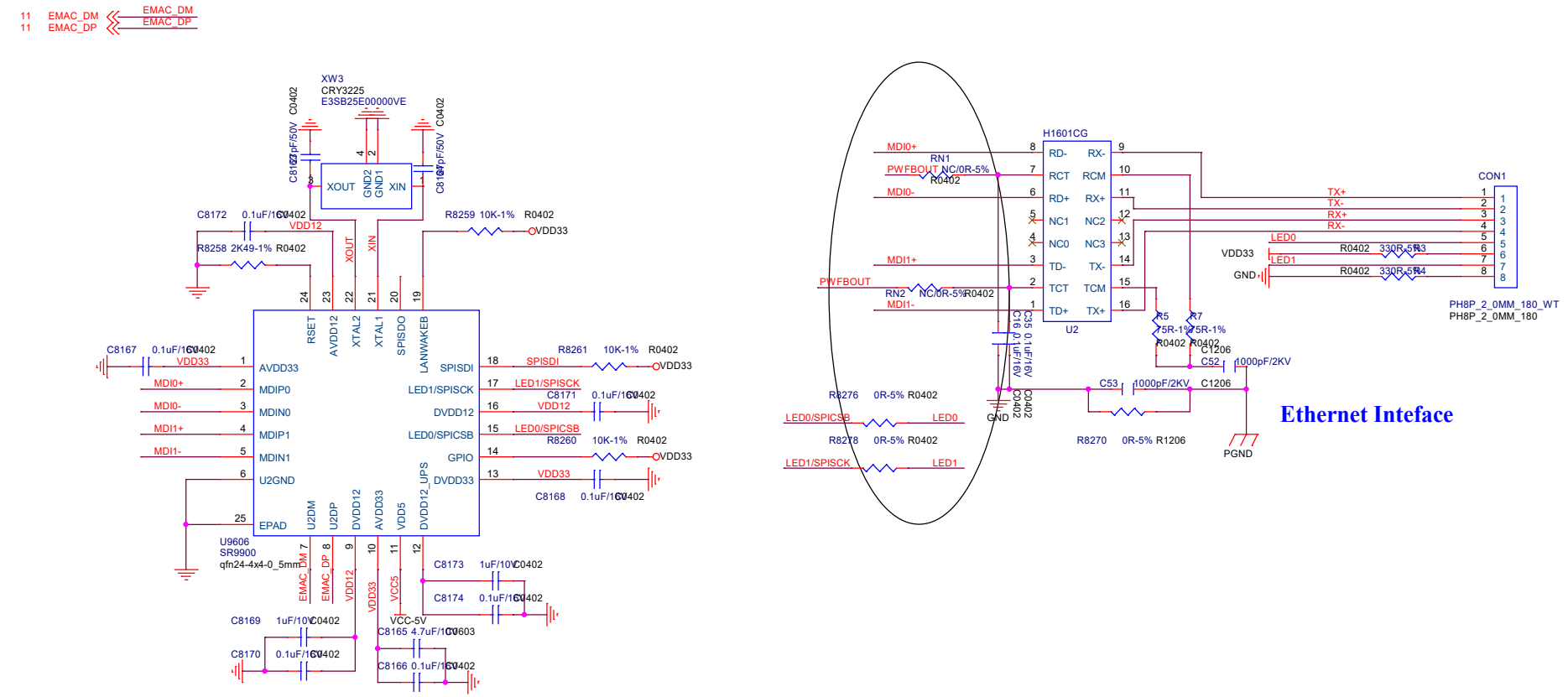


	PORT B	
	MIPI	LVDS
M3_B-/L0_B-	MIPI_D3-	LVDS_D0-
M3_B+/L0_B+	MIPI_D3+	LVDS_D0+
M2_B-/L1_B-	MIPI_D2-	LVDS_D1-
M2_B+/L1_B+	MIPI_D2+	LVDS_D1+
MCK_B-/L2_B-	MIPI_CLK-	LVDS_D2-
MCK_B+/L2_B+	MIPI_CLK+	LVDS_D2+
M1_B-/LCK_B-	MIPI_D1-	LVDS_CLK-
M1_B+/LCK_B+	MIPI_D1+	LVDS_CLK+
M0_B-/L3_B-	MIPI_D0-	LVDS_D3-
M0_B+/L3_B+	MIPI_D0+	LVDS_D3+

The signal line connection relationship of PORT A and PORT B is the same.

AllWinner Technology Co.,Ltd		
Design Name	A100_A133_B3_AXP707_LPDDR3	
Size A2	Page Name 12 CAMERA	Rev
Date: Thursday, September 16, 2021	Sheet 12 of 18	

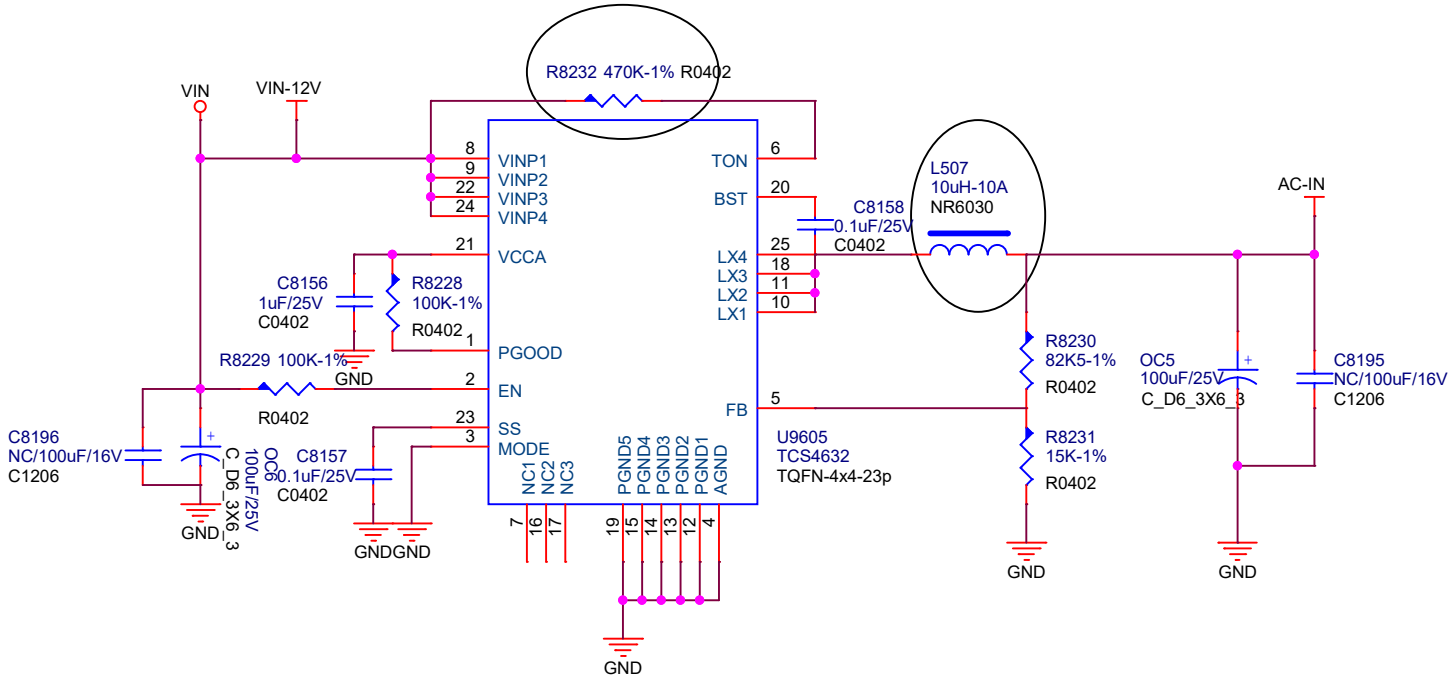

LVDS
MIPI
BACKLIGHT
背光电源
CTP
EDP
NS8801S
框里的定义有改，请确认是否可行
小板上用了两颗DC-DC,现在去掉一颗DC-DC,直接用系统3.3V，外加一颗LDO做1.2V，用DC-DC太浪费
AllWinner Technology Co.,Ltd
A100_A133_B3_AXP707_LPDDR3
13 LCM
Thursday, September 16, 2021



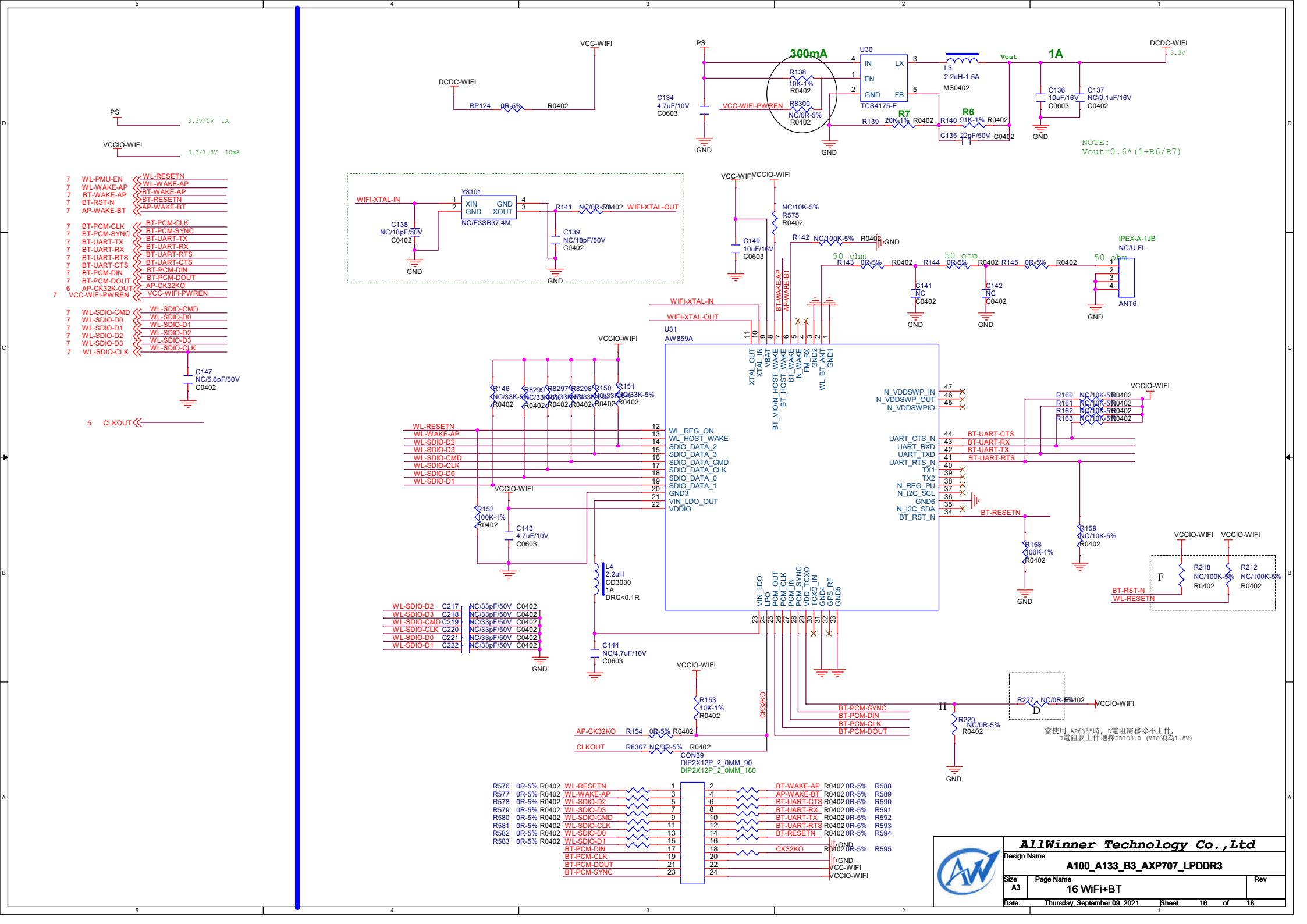
(CONNECT TO CH

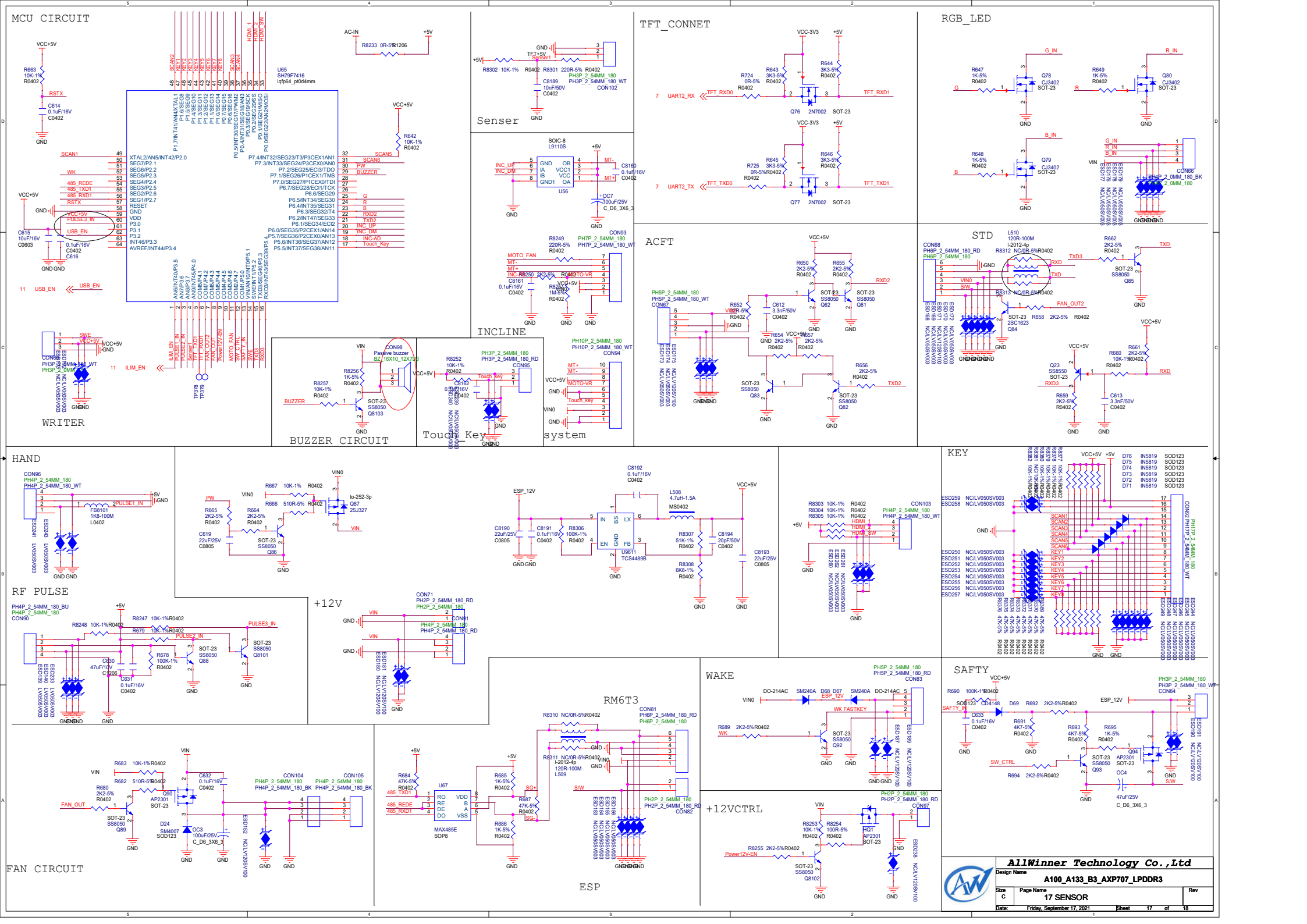
Et Inteface

AllWinner Technology Co.,Ltd		
Design Name (CONNECT TO CHASSIS GND) A100_A133_B3_AXP707_LPDDR3		
Size A3	Page Name 14 CTP	Rev
Date: Thursday, September 09, 2021	Sheet 14 of 18	



AllWinner Technology Co.,Ltd		
Design Name: A100_A133_B3_AXP707_LPDDR3		
Size: A4	Page Name: 15 KEY/DEBUG	Rev
Date: Thursday, September 09, 2021	Sheet 15 of 18	


PS
3.3V/5V 1A
VCCIO-WIFI
3.3/1.8V 10mA
WL-PMU-EN
WL-WAKE-AP
BT-WAKE-AP
BT-RST-N
AP-WAKE-BT
BT-PCM-CLK
BT-PCM-SYNC
BT-UART-TX
BT-UART-RX
BT-UART-RTS
BT-UART-CTS
BT-PCM-DIN
BT-PCM-DOUT
AP-CK32KO
VCC-WIFI-PWREN
WL-SDIO-CMD
WL-SDIO-D0
WL-SDIO-D1
WL-SDIO-D2
WL-SDIO-D3
WL-SDIO-CLK
C147
NC/5.6pF/50V
C0402
CLKOUT
VCC-WIFI
DCDC-WIFI
RP124 0R-5% R0402
300mA
U30
TCS4175-E
R138
10K-1%
R0402
R8300
NC/0R-5%
R0402
R7
R6
R139 20K-1% R0402
R140 91K-1% R0402
C135 22pF/50V C0402
L3
2.2uH-1.5A
MS0402
Vout
1A
C136
10uF/16V
C0603
C137
NC/0.1uF/16V
C0402
C134
4.7uF/10V
C0603
NOTE:
Vout=0.6*(1+R6/R7)
Y8101
NC/E3SB37.4M
WIFI-XTAL-IN
WIFI-XTAL-OUT
C138
NC/18pF/50V
C0402
C139
NC/18pF/50V
C0402
R141 NC/0R-5% R0402
NC/10K-5%
R575
R0402
C140
10uF/16V
C0603
R142 NC/100K-5% R0402
R143 0R-5% R0402
R144 0R-5% R0402
R145 0R-5% R0402
50 ohm
C141
NC
C0402
C142
NC
C0402
IPEX-A-1JB
NC/U.FL
ANT6
U31
AW859A
XTAL_OUT
XTAL_IN
VBAT
BT_HOST_WAKE
BT_WAKE
N_WAKE
FM_RX
FM_TX
WL_BT_ANT
GND1
BT_VIO/N_HOST_WAKE
BT_HOST_WAKE
BT_WAKE
WL_REG_ON
WL_HOST_WAKE
SDIO_DATA_2
SDIO_DATA_3
SDIO_DATA_CMD
SDIO_DATA_CLK
SDIO_DATA_0
SDIO_DATA_1
GND3
VIN_LDO_OUT
VDDIO
N_VDDSWP_IN
N_VDDSWP_OUT
N_VDDSWPIO
UART_CTS_N
UART_RXD
UART_TXD
UART_RTS_N
TX1
TX2
N_REG_PU
N_I2C_SCL
GND6
N_I2C_SDA
BT_RST_N
BT-UART-CTS
BT-UART-RX
BT-UART-TX
BT-UART-RTS
BT-RESETN
R146 NC/33K-5% R0402
R8299 NC/33K-5% R0402
R8297 NC/33K-5% R0402
R8298 NC/33K-5% R0402
R150 NC/33K-5% R0402
R151 NC/33K-5% R0402
R152
100K-1%
R0402
C143
4.7uF/10V
C0603
L4
2.2uH
CD3030
1A
DRC<0.1R
C144
NC/4.7uF/16V
C0603
R153
10K-1%
R0402
R154 0R-5% R0402
R8367 NC/0R-5% R0402
CON39
DIP2X12P_2_0MM_90
DIP2X12P_2_0MM_180
R158
100K-1%
R0402
R159
NC/10K-5%
R0402
R160 NC/10K-5% R0402
R161 NC/10K-5% R0402
R162 NC/10K-5% R0402
R163 NC/10K-5% R0402
R218
NC/100K-5%
R0402
R212
NC/100K-5%
R0402
R227 NC/0R-5% R0402
R229
NC/0R-5%
R0402
當使用 AP6335時, D電阻需移除不上件,
H電阻要上件選擇SDIO3.0 (VIO須為1.8V)
WL-SDIO-D2 C217 NC/33pF/50V C0402
WL-SDIO-D3 C218 NC/33pF/50V C0402
WL-SDIO-CMD C219 NC/33pF/50V C0402
WL-SDIO-CLK C220 NC/33pF/50V C0402
WL-SDIO-D0 C221 NC/33pF/50V C0402
WL-SDIO-D1 C222 NC/33pF/50V C0402
R576 0R-5% R0402 WL-RESETN
R577 0R-5% R0402 WL-WAKE-AP
R578 0R-5% R0402 WL-SDIO-D2
R579 0R-5% R0402 WL-SDIO-D3
R580 0R-5% R0402 WL-SDIO-CMD
R581 0R-5% R0402 WL-SDIO-CLK
R582 0R-5% R0402 WL-SDIO-D0
R583 0R-5% R0402 WL-SDIO-D1
BT-PCM-DIN
BT-PCM-CLK
BT-PCM-DOUT
BT-PCM-SYNC
BT-WAKE-AP R0402 0R-5% R588
AP-WAKE-BT R0402 0R-5% R589
BT-UART-CTS R0402 0R-5% R590
BT-UART-RX R0402 0R-5% R591
BT-UART-TX R0402 0R-5% R592
BT-UART-RTS R0402 0R-5% R593
BT-RESETN R0402 0R-5% R594
CK32KO R0402 0R-5% R595
GND
VCC-WIFI
VCCIO-WIFI
AllWinner Technology Co.,Ltd
Design Name
A100_A133_B3_AXP707_LPDDR3
Size
A3
Page Name
16 WiFi+BT
Rev
Date: Thursday, September 09, 2021
Sheet 16 of 18


MCU CIRCUIT
U65
SH79F7416
lqfp64_pt0d4mm
WRITER
BUZZER CIRCUIT
Touch_Key
INCLINE
system
Senser
TFT_CONNET
RGB_LED
ACFT
STD
HAND
RF PULSE
+12V
KEY
FAN CIRCUIT
RM6T3
ESP
WAKE
+12VCTRL
SAFTY
AllWinner Technology Co.,Ltd
A100_A133_B3_AXP707_LPDDR3
17 SENSOR
Friday, September 17, 2021