



統寶光電股份有限公司
A Toppoly and Philips display company

機密等級

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文件編號: Document No.	文件名稱: TPG121 ASIC Customer Specification Document Title : TPG121 ASIC Customer Specification	版別: 1.7 Rev. 1.7	頁次: 1/29 Page No. 1/29
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TPG121 ASIC Customer Specification

Electric System Design Department

TPO Optoelectronics Corp.

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1 Revision History

Date (Y/M/D)	Page	Contents	Version
2006/12/21	All	First version	1.0
2007/4/25	2, 6	Modify index and add "FPC Pad Description"	1.1
2007/9/25	7	Modify standby mode figure	1.2
2007/9/25	11	Modify global reset	1.2
2007/9/25	26	Modify register suggestion table	1.2
2008/3/18	6	Remove FPC pad description and add IC pad definition	1.3
2008/3/18	7	Update LED application circuit and remove FPC application circuit	1.3
2008/3/18	9	Update power on/off sequence	1.3
2008/3/18	11	Modify electrical characteristics	1.3
2008/3/18	12	Add VCC slew time	1.3
2008/3/18	13, 14	Remove redundant QVGA description	1.3
2008/3/18	15	Modify input RGB sequence in through mode	1.3
2008/3/18	18	Update SPI comment	1.3
2008/3/18	27	Add gamma description and remove suggestion table	1.3
2008/6/25	26	Modify R05[7] function	1.4
2008/6/25	26	Add note for R06[7] function	1.4
2008/09/23	5~11, 19, 23	1. Remove PWM function 2. Modify power on/off sequence 3. Modify register table	1.5
2008/11/27	28	1. Add note for R07 [7] function 2. Modify R04 default value	1.6
2008/12/29	5, 29	1. Modify Charge Pump Circuit capacitance value 1. Add 39pin FPC connector application circuit	1.7

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TPG121

Black and Normally White RGB Driver/Timing Controller IC for LTPS TFT LCD

2 Description

This is digital signal processing IC for normally black/normally white low temperature poly-silicon TFT-LCD. Handles 8 bits of input data (256-level gray scale data) for each of the RGB or YUV colors and output analog RGB signals from internal OP AMP.

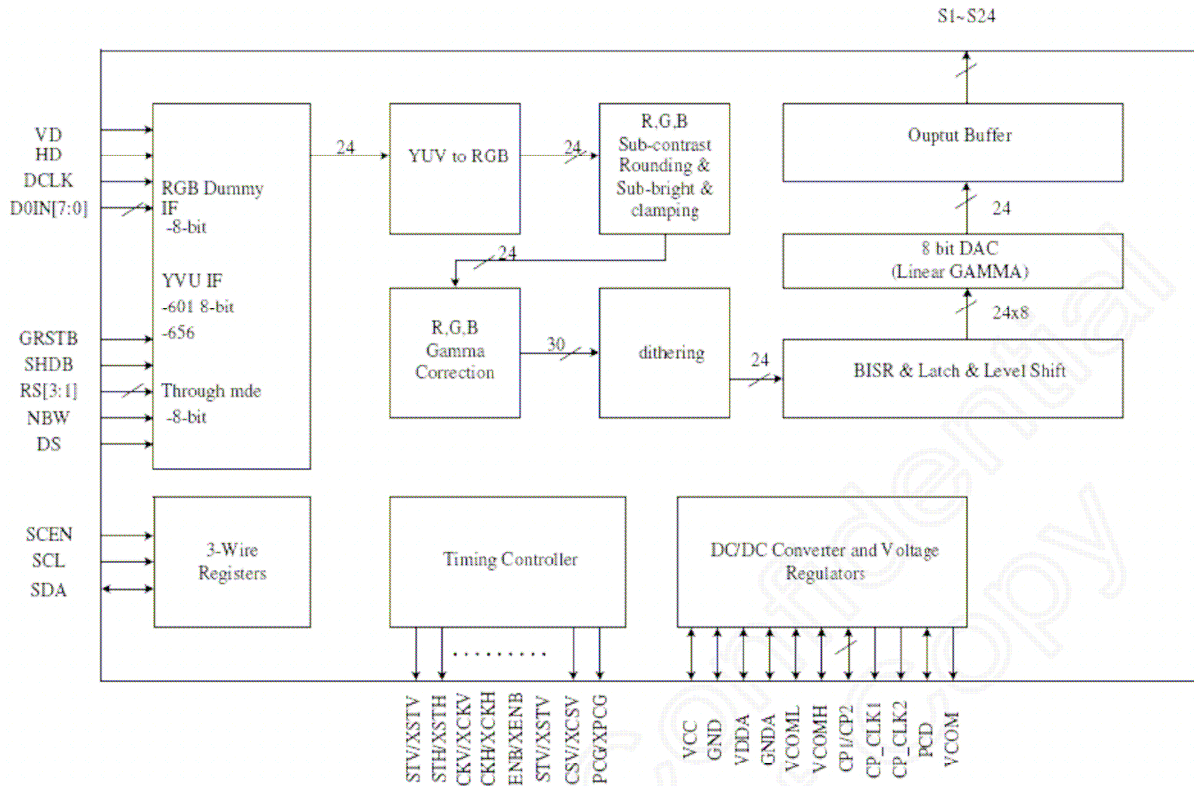
This is green product and spec refers to top's Green Product Chemical Substance Specification Standard Hand Book.

3 Features

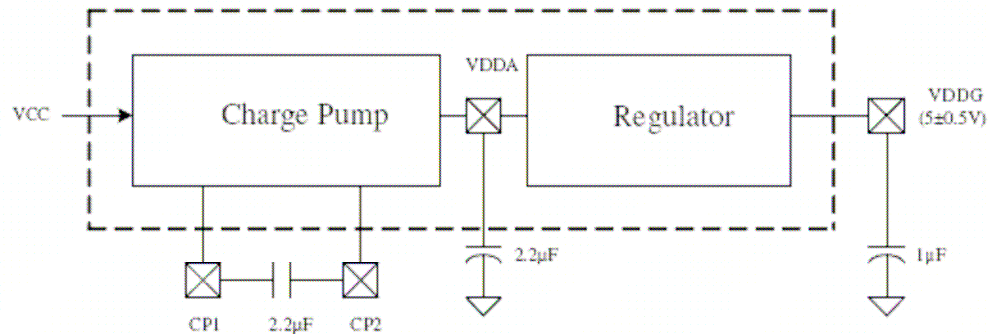
- 3.1 Support Normally Black and Normally White.
- 3.2 Installed timing controller to drive LCD panel.
- 3.3 Resolution: 480x240, 640x240 and 960x240 in delta color filter with same color source line, and 320xRGBx240 in stripe color filter.
- 3.4 Support 8-bit serial RGBDummy, serial RGB through mode, and ITU-R BT. 601 NTSC/PAL input formats.
- 3.5 Supply voltage: VCC (digital): 3.0V~3.6V.
- 3.6 Support 3-wire SPI commands setting.
- 3.7 Build-in RGB separated contrast, brightness and 3-gamma (RGB) adjustment.
- 3.8 Outputs: analog RGB, common data.
- 3.9 Support 24 output channels.
- 3.10 Build-in DC/DC circuit, charge pump circuit, Vcom and pre-charge adjustment circuit.
- 3.11 Line-inversion driving method.
- 3.12 COG package.
- 3.13 ESD rating: HBM: 2.5KV, MM: 250V.

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4 Block Diagram



4.1 Charge Pump Circuit



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5 Pad Definition

Pin No.	Symbol	I/O	Description			
3~10, 27, 28	TP1~TP10	T	Testing use, keep these pins open for normal operation.			
11	GRSTB	I	Global reset pin. It should be connected to VCC in normal operation. If connected to GND, the controller is in reset state.(Normally pulled high)			
12	SHDB	I	Standby mode setting pin. Active low, Timing Controller, Output Buffer DAC and DC2DC converter is off when SHDB is low(normally pulled high)			
13	SCEN	I	Serial interface chip enable line			
14	SCL	I	Serial interface clock line			
15	SDA	I/O	Serial interface data line			
16~23	DIN[7:0]	I	Digital data input			
24	DCLK	I	Clock signal; latch data onto line latches at rising edge			
25	HD	I	Horizontal sync input			
26	VD	I	Vertical sync input			
29~34	VCC	P	Power supply for digital circuit and charge pump circuit. 3.0V ~ 3.6V			
35~37	RS[3:1]	I	Resolution selection:			
			RS[3]	RS[2]	RS[1]	Resolution
			L	L	L	480x240
			L	H	L	640x240
			H	H	H	960x240(default)
38	NBW	I	Internally pulled high. NBW=H: Normally Black (default) NBW=L: Normally White			
39	DS	I	Display mode selection for 960x240 panel. Internally pulled high. Please set high for normal operation.			
40~42	GND	P	Digital ground			
46~48	CP2	C	Capacitor for charge pump (Ccp=2.2uF)			
49~51	CP1	C	Capacitor for charge pump (Ccp=2.2uF)			
52~54	VDDA	C	Regulation Capacitor for Analog Voltage (CAVDD= 2.2 uF)			
55~57	VDDG	C	Regulation Capacitor for Charge Pump (CGVDD= 1 uF)			
58,59,73,74,	GNDA	P	Analog ground			

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123, 124			
60	VCOMH	C	Capacitor for Vcom High($C_{VCOMH} = 2.2 \mu F$)
61	VCOML	C	Capacitor for Vcom low($C_{VCOML} = 2.2 \mu F$)
62	PCD	C	Capacitor for PCD
67, 68	CP_CLK1, CP_CLK2	O	Charge pump clock
69,70,125,126	VCOM	O	Common output signal
71,72,121,122	VDDA	C	Analog voltage output to panel
75	STV	O	Vertical start pulse output
76	XSTV	O	Inverted STV output
77	CKV	O	V clock pulse output
78	XCKV	O	Inverted V clock pulse output
79	CSV	O	Vertical inversion control signal output
80	XCSC	O	Inverted CSV output
81	ENB	O	Enable pulse output
82	XENB	O	Inverted ENB output
83, 117	PCG	O	Pre-charge pulse control output
84, 118	XPCG	O	Inverted PCG output
85,86,119,120	PCD	O	Pre-charge voltage output
87~110	DOUT[24:1]	O	Analog driver output
111	CSH	O	Horizontal inversion control signal output
112	XCSH	O	Inverted CSH output
113	STH	O	Horizontal start pulse
114	XSTH	O	Inverted STH output
115	CKH	O	H clock pulse output
116	XCKH	O	Inverted H clock pulse output
1, 2, 43~45, 63~66, 127, 128	Dummy	D	Dummy Pins

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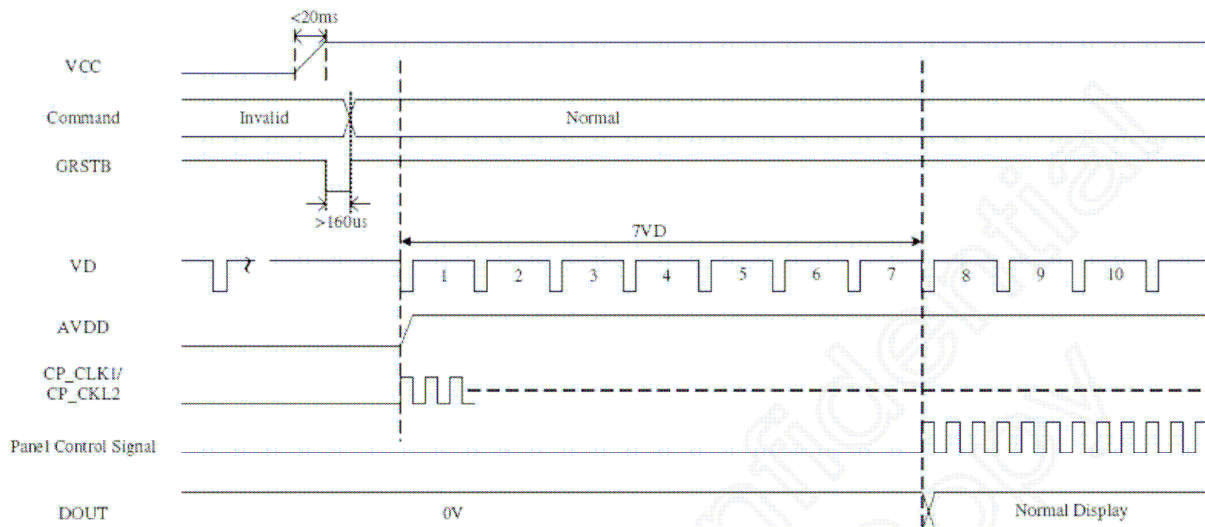
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6. Power ON/OFF and Mode Change Sequence

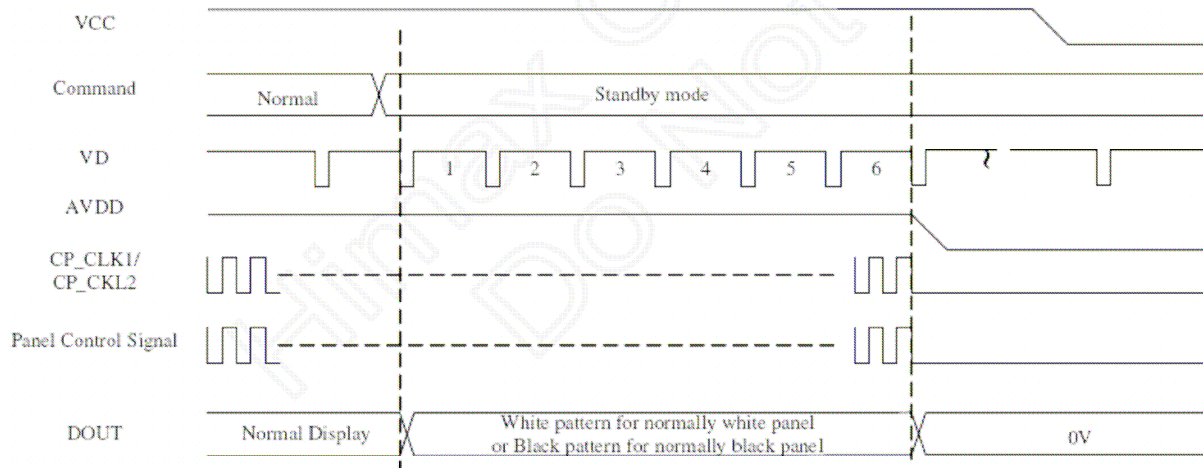
Power ON sequence (standby mode or global reset to normal mode)



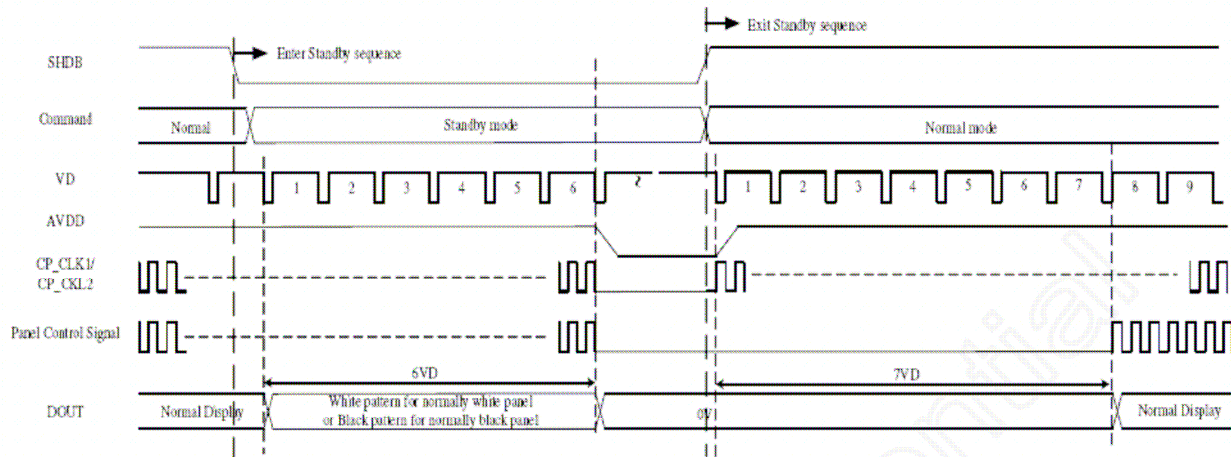
Note 1: After VCC rising, SPI (3-wire) command must wait 160us to start and accomplish all setting of the register value during 7VD field.

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Power OFF sequence (power off or normal mode into standby mode)



Enter and exit standby mode sequence

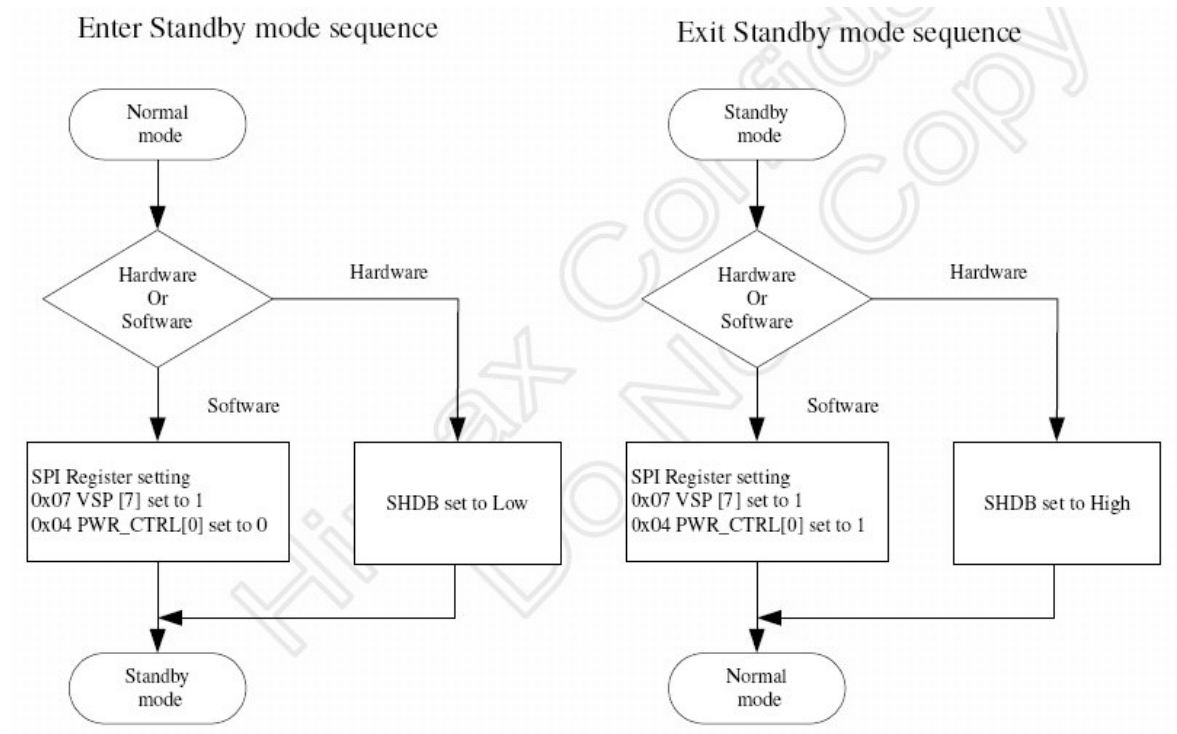


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7 Electrical Characteristics

For the digital circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	Digital power
Low Level Input Voltage	V_{il}	GND	-	$0.3 \times V_{CC}$	V	Digital input pins
High Level Input Voltage	V_{ih}	$0.7 \times V_{CC}$	-	V_{CC}	V	Digital input pins
Pull-high Impedance	R_{inh}	$0.5 \times \text{typ}$	550	$1.5 \times \text{typ}$	$k\Omega$	
Pull-low Impedance	R_{inl}	$0.5 \times \text{typ}$	350	$1.5 \times \text{typ}$	$k\Omega$	
Digital Stand-by Current	I_{st}	-	-	60	μA	DCLK is stopped, Outputs are High-Z Without pull high or low current
Digital Operating Current	I_{CC}	-	-	10	mA	DCLK=27MHz, V_{CC} =3.3V, PWM on load, RS[2:0]=HHL(960x240)

For the analog circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Internal Supply Voltage	AV_{DD}	5.0	5.5	7.0	V	Power supply for the analog circuit
	GV_{DD}	4.5	5.0	5.5	V	Power supply for the gamma resistor
Analog Standby Current	I_{st}	-	-	1	μA	Shutdown mode. V_{CC} =3.3V
Analog Operating Current	I_{DD}	-	-	4	mA	V_{CC} =3.3V, Line inversion, DOUT[24:1] no load, Vcom no load

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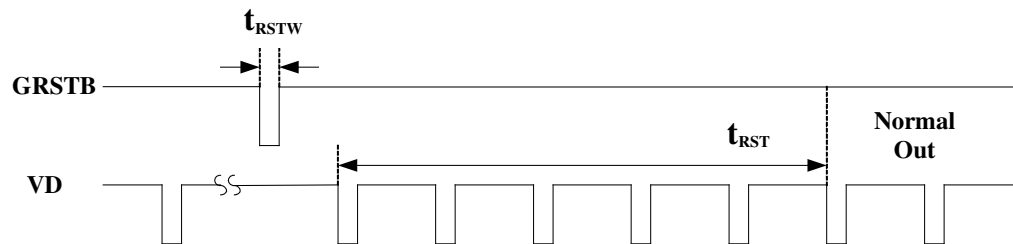
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8 VCC Power On Slew Time

Function pin	Symbol	Min.	Typ.	Max.	Unit	Condition
VCC power on slew time	T_{por}			20	ms	From 0V to 90% VCC

9 Global Reset

Function pin	Symbol	Min.	Typ.	Max.	Unit	Condition
GRSTB	t_{RSTW}	160	--	--	μs	$V_{CC}=3.3$
	t_{RST}	5			Field	



10 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Operating ambient temperature	T_A	-30°C to 85°C	°C
Storage temperature	T_{STG}	-50°C to 100°C	°C

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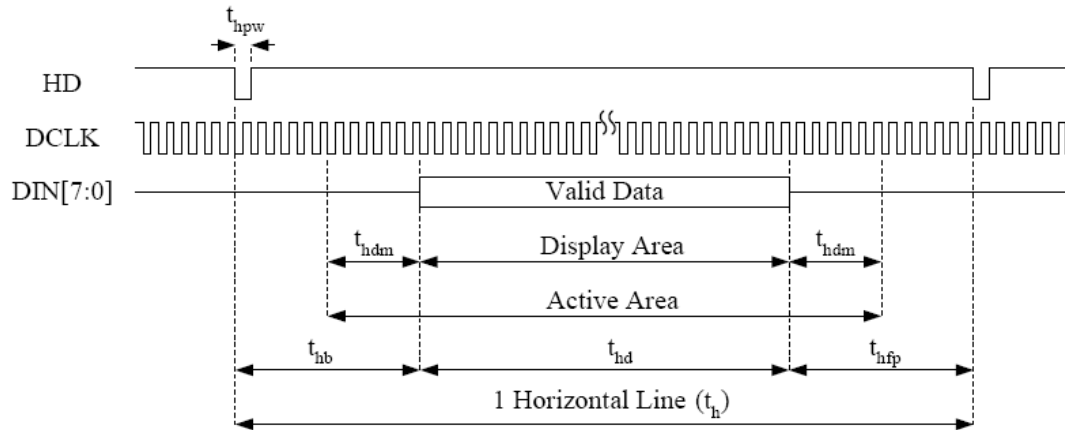
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11 Serial RGB Dummy or Serial-YUV 4:2:2 modes

--Horizontal--

Serial RGB dummy or YUV-4:2:2 Mode(480x240,640x240,960x240)



Parameter		Symbol	Mode				Unit
			NTSC		PAL		
DCLK Frequency		F _{DCLK}	27	24.54	27	24.38	MHz
Horizontal valid data		t _{hd}	1440	1280	1440	1280	DCLK
1 Horizontal Line		t _h	1716	1560	1728	1560	DCLK
HSYNC Pulse Width	Min.	t _{hpw}	1				DCLK
	Typ.		1				
	Max.		-				
Hsync blanking		t _{hp}	240				DCLK
Hsync front porch		t _{hfp}	36	40	48	40	DCLK
Horizontal dummy time	640x240	t _{hdm}	4				DCLK
	960x240		0				

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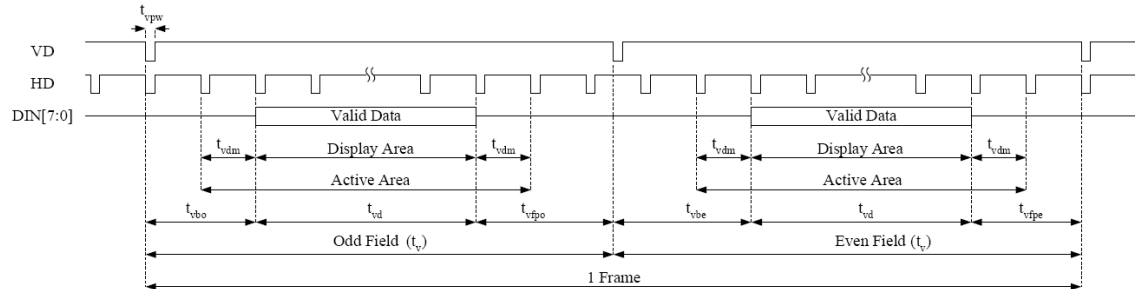
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--Vertical--

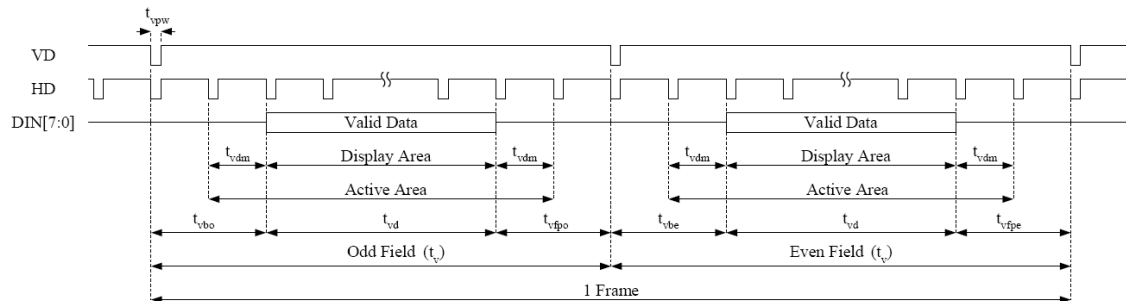
Interlace

ODD Field: same phase VD and HD

EVEN Field: same phase VD and Half-HD



Non-interlace



Parameter		Symbol	Interlace		Non-interlace		Unit
			NTSC	PAL	NTSC	PAL	
Vertical valid data		t _{vd}	240	288	240	288	H
1 Vertical field		t _v	262.5	312.5	262	312	H
Vsync pulse width	Min.	t _{vpw}	1		1		H
	Typ.		1				
	Max.		-				
Vsync blanking	Odd field	t _{vbo}	21	24	21	24	H
	Even field	t _{vbe}	21.5	24.5			H
Vsync front porch	Odd field	t _{vfpo}	1.5	0.5	1	0	H
	Even field	t _{vfpe}	1	0			H
Vertical dummy time		t _{vdm}	0	0	0	0	H

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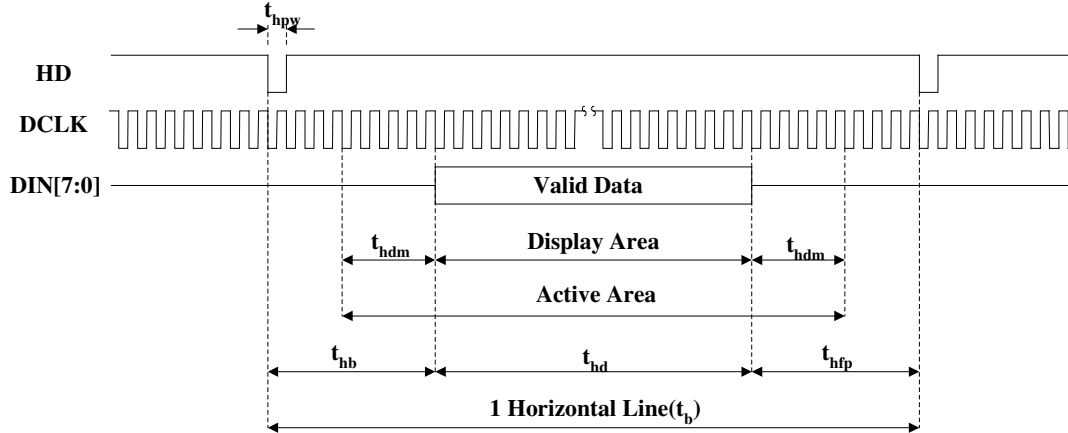
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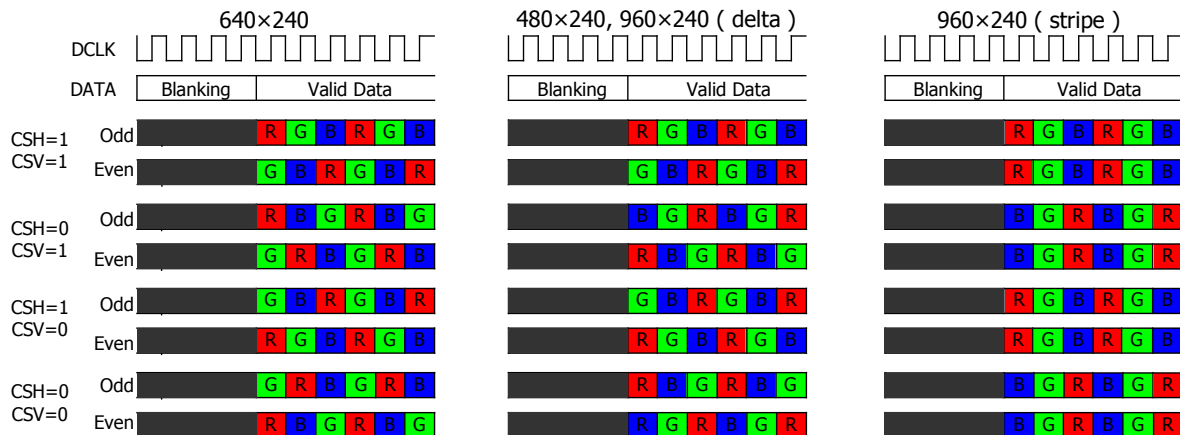
12 Through mode

--Horizontal--



Parameter		Symbol	Panel Resolution			Unit
DCLK Frequency		f _{clk}	10.36	12.90	18.42	MHz
Horizontal valid data		t _{hd}	480	640	960	DCLK
1 Horizontal Line		t _h	659	820	1171	DCLK
HSYNC Pulse Width	Min.	t _{h_{pw}}	1			DCLK
	Typ.		1			
	Max.		--			
Hsync blanking		t _{hb}	96	117	152	DCLK
Hsync front porch		t _{h_{fp}}	83	63	59	DCLK
Horizontal dummy time		t _{h_{dm}}	0	4	0	MCLK

Input RGB Sequence



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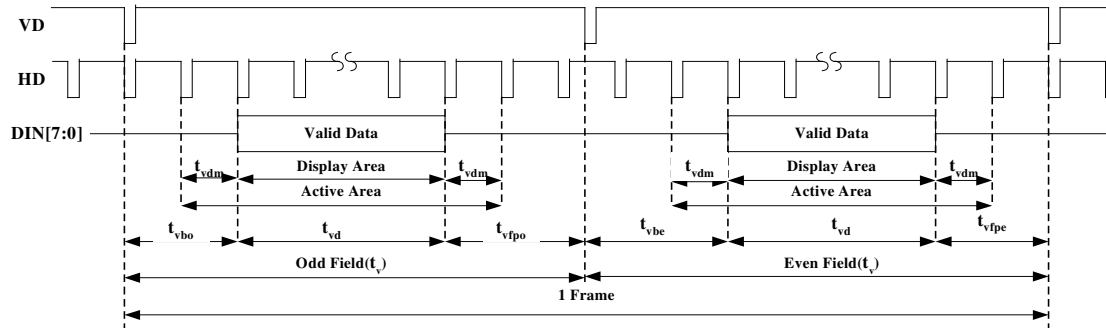
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--Vertical--

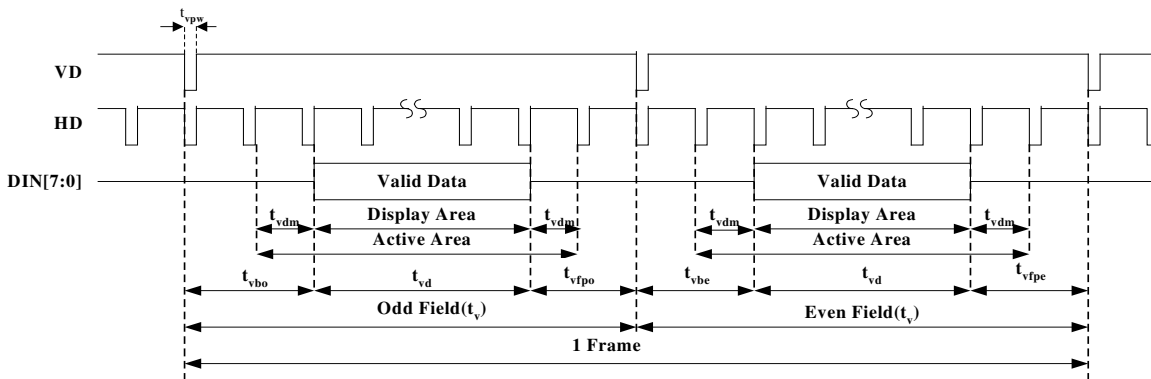
Interlace

ODD Field: same phase VD and HD

EVEN Field: same phase VD and Half-HD



Non-interlace



Parameter	Symbol	Interlace	Non-interlace	Unit
Vertical valid data	t_{vd}	240	240	H
1 Vertical field	t_v	262.5	262	H
Vsync pulse width	Min.	t_{vpw}	1	H
	Typ.		1	H
	Max.		-	H
Vsync blanking	Odd field	t_{vbo}	14	H
	Even field	t_{vbe}	14.5	H
Vsync front porch	Odd field	t_{vfpo}	8.5	H
	Even field	t_{vfpe}	8	H
Vertical dummy time	t_{vdm}	0	0	H

表單編號:

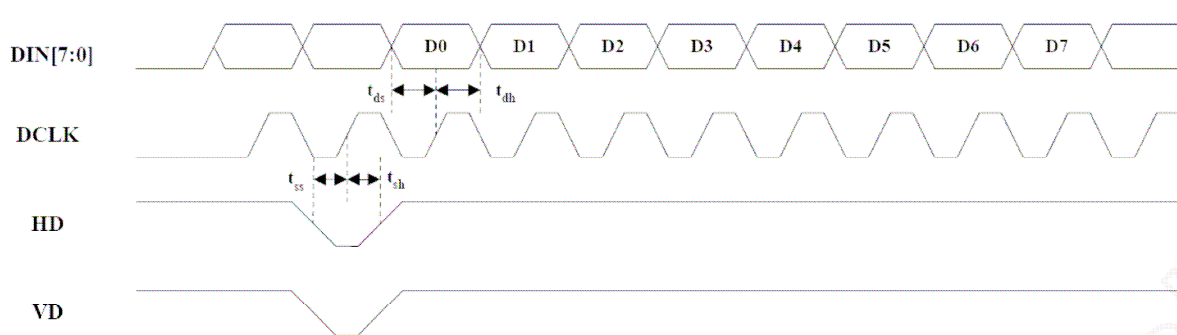
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13 Timing Diagram



Item	symbol	min	typ	Max	Unit
DCLK duty ratio	Duty	40	-	60	%
Data setup time	t_{ds}	12	-	-	ns
Data hold time	t_{dh}	12	-	-	ns
Control signal setup time	t_{ss}	12	-	-	ns
Control signal hold time	t_{sh}	12	-	-	ns

表單編號:

版本:

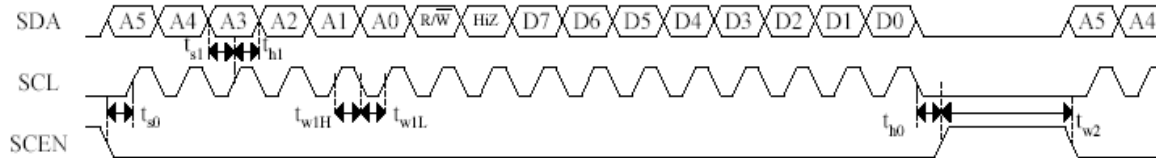
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14 3-Wires Serial control

3 wires Serial data transfer format:



Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SDA Setup Time	t_{s0}	SCEN to SCL	150			ns
	t_{s1}	SDA to SCL	150			ns
SDA Hold Time	t_{h0}	SCEN to SCL	150			ns
	t_{h1}	SDA to SCL	150			ns
Pulse Width	t_{w1L}	SCL pulse width	160			ns
	t_{w1H}	SCL pulse width	160			ns
	t_{w2}	SCEN pulse width	1.0			us
Clock duty			40	50	60	%

Note 2:

- The data is written to the register of assigned address when “End of transfer” is detected after the 16th SCL rising cycles. Data is not accepted if there are less or more than 16 cycles for one transaction.
- Only when SCL is input 16 times and SCEN is in the "Low" period simultaneously, SDA is accepted.
- It needs DCLK input for SDA setting.
- SDATA, SCLK, SLOAD can be floating.
- The first 6 bits (A5 ~ A0) specify the address of the register. And next bit mean Read/Write command. “0” is WRITE. “1” is READ. And next cycle is turn-round cycle. And the last 8 bits are for Data setting (D7 ~ D0). The address and data are transferred from the MSB to LSB sequentially.

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15 Register description

Address	Default	Read/Write	Meaning
0x02	0x09	R/W	[1:0]: Input format [2]: Format standard [3]: Valid data for RGBDm or YUV mode [4]: Input clock latch data edge [5]: HD polarity [6]: VD polarity
0x03	0x30	R/W	[0]: Select of interlace mode [1]: Select of field mix [3:2]: YCbCr sequence [4]: YUV input transfer matrix [5]: UV offset for matrix A [7:6]: Output driver capability
0x04	0x0B	R/W	[0]: Power management [2:1]: Reserved [3]: Pre-charge on/off [7:4]: VCOM inversion method selection
0x05	0x2B	R/W	[0]: Horizontal reverse mode [1]: Vertical reverse mode [2]: Color filter selection for 960x240 [6:3]: Sample and hold phase [7]: CP_CLK Duty cycle
0x06	0xD8	R/W	[5:0]: Horizontal start position for through mode [6]: Normal black/Normal white select [7]: display selection, 16:9 or 4:3
0x07	0x78	R/W	[3:0]: Vertical start position for through mode [6:4]: Resolution selection [7]: Resolution select for Hardware or software
0x08	0x00	R/W	[5:0]: ENB negative position
0x09	0x20	R/W	[5:0]: R gain of contrast
0x0A	0x20	R/W	[5:0]: G gain of contrast
0x0B	0x20	R/W	[5:0]: B gain of contrast
0x0C	0x10	R/W	[5:0]: Offset of brightness R
0x0D	0x10	R/W	[5:0]: Offset of brightness G
0x0E	0x10	R/W	[5:0]: Offset of brightness B
0x0F	0x53	R/W	[6:0]: Vcom high level
0x10	0x5A	R/W	[6:0]: Vcom low level
0x11	0x1D	R/W	[5:0]: PCD level
0x12	0xBC	R/W	[3:0]: Gamma output voltage level for data input 00H [7:4]: Gamma output voltage level for data input FFH

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0x13	0xFE	R/W	[7:6]: Red color GAMMA 0[9:8] of gamma Correction [5:4]: Red color GAMMA 8[9:8] of gamma Correction [3:2]: Red color GAMMA 16[9:8] of gamma Correction [1:0]: Red color GAMMA 32[9:8] of gamma Correction
0x14	0xA5	R/W	[7:6]: Red color GAMMA 64[9:8] of gamma Correction [5:4]: Red color GAMMA 96[9:8] of gamma Correction [3:2]: Red color GAMMA 128[9:8] of gamma Correction [1:0]: Red color GAMMA 192[9:8] of gamma Correction
0x15	0x00	R/W	[7:6]: Red color GAMMA 224[9:8] of gamma Correction [5:4]: Red color GAMMA 240[9:8] of gamma Correction [3:2]: Red color GAMMA 248[9:8] of gamma Correction [1:0]: Red color GAMMA 256[9:8] of gamma Correction
0x16	0xD0	R/W	[7:0]: Red color GAMMA 0[7:0] of gamma Correction
0x17	0x38	R/W	[7:0]: Red color GAMMA 8[7:0] of gamma Correction
0x18	0x10	R/W	[7:0]: Red color GAMMA 16[7:0] of gamma Correction
0x19	0xD5	R/W	[7:0]: Red color GAMMA 32[7:0] of gamma Correction
0x1A	0x8D	R/W	[7:0]: Red color GAMMA 64[7:0] of gamma Correction
0x1B	0x18	R/W	[7:0]: Red color GAMMA 96[7:0] of gamma Correction
0x1C	0xD3	R/W	[7:0]: Red color GAMMA 128[7:0] of gamma Correction
0x1D	0x7D	R/W	[7:0]: Red color GAMMA 192[7:0] of gamma Correction
0x1E	0xF2	R/W	[7:0]: Red color GAMMA 224[7:0] of gamma Correction
0x1F	0x8E	R/W	[7:0]: Red color GAMMA 240[7:0] of gamma Correction
0x20	0x52	R/W	[7:0]: Red color GAMMA 248[7:0] of gamma Correction
0x21	0x00	R/W	[7:0]: Red color GAMMA 256[7:0] of gamma Correction
0x22	0xFE	R/W	[7:6]: Green color GAMMA 0[9:8] of gamma Correction [5:4]: Green color GAMMA 8[9:8] of gamma Correction [3:2]: Green color GAMMA 16[9:8] of gamma Correction [1:0]: Green color GAMMA 32[9:8] of gamma Correction
0x23	0xA5	R/W	[7:6]: Green color GAMMA 64[9:8] of gamma Correction [5:4]: Green color GAMMA 96[9:8] of gamma Correction [3:2]: Green color GAMMA 128[9:8] of gamma Correction [1:0]: Green color GAMMA 192[9:8] of gamma Correction
0x24	0x00	R/W	[7:6]: Green color GAMMA 224[9:8] of gamma Correction [5:4]: Green color GAMMA 240[9:8] of gamma Correction [3:2]: Green color GAMMA 248[9:8] of gamma Correction [1:0]: Green color GAMMA 256[9:8] of gamma Correction
0x25	0xD0	R/W	[7:0]: Green color GAMMA 0[7:0] of gamma Correction
0x26	0x38	R/W	[7:0]: Green color GAMMA 8[7:0] of gamma Correction
0x27	0x10	R/W	[7:0]: Green color GAMMA 16[7:0] of gamma Correction

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0x28	0xD5	R/W	[7:0]: Green color GAMMA 32[7:0] of gamma Correction
0x29	0x8D	R/W	[7:0]: Green color GAMMA 64[7:0] of gamma Correction
0x2A	0x18	R/W	[7:0]: Green color GAMMA 96[7:0] of gamma Correction
0x2B	0xD3	R/W	[7:0]: Green color GAMMA 128[7:0] of gamma Correction
0x2C	0x7D	R/W	[7:0]: Green color GAMMA 192[7:0] of gamma Correction
0x2D	0xF2	R/W	[7:0]: Green color GAMMA 224[7:0] of gamma Correction
0x2E	0x8E	R/W	[7:0]: Green color GAMMA 240[7:0] of gamma Correction
0x2F	0x52	R/W	[7:0]: Green color GAMMA 248[7:0] of gamma Correction
0x30	0x00	R/W	[7:0]: Green color GAMMA 256[7:0] of gamma Correction
0x31	0xFE	R/W	[7:6]: Blue color GAMMA 0[9:8] of gamma Correction [5:4]: Blue color GAMMA 8[9:8] of gamma Correction [3:2]: Blue color GAMMA 16[9:8] of gamma Correction [1:0]: Blue color GAMMA 32[9:8] of gamma Correction
0x32	0xA5	R/W	[7:6]: Blue color GAMMA 64[9:8] of gamma Correction [5:4]: Blue color GAMMA 96[9:8] of gamma Correction [3:2]: Blue color GAMMA 128[9:8] of gamma Correction [1:0]: Blue color GAMMA 192[9:8] of gamma Correction
0x33	0x00	R/W	[7:6]: Blue color GAMMA 224[9:8] of gamma Correction [5:4]: Blue color GAMMA 240[9:8] of gamma Correction [3:2]: Blue color GAMMA 248[9:8] of gamma Correction [1:0]: Blue color GAMMA 256[9:8] of gamma Correction
0x34	0xD0	R/W	[7:0]: Blue color GAMMA 0[7:0] of gamma Correction
0x35	0x38	R/W	[7:0]: Blue color GAMMA 8[7:0] of gamma Correction
0x36	0x10	R/W	[7:0]: Blue color GAMMA 16[7:0] of gamma Correction
0x37	0xD5	R/W	[7:0]: Blue color GAMMA 32[7:0] of gamma Correction
0x38	0x8D	R/W	[7:0]: Blue color GAMMA 64[7:0] of gamma Correction
0x39	0x18	R/W	[7:0]: Blue color GAMMA 96[7:0] of gamma Correction
0x3A	0xD3	R/W	[7:0]: Blue color GAMMA 128[7:0] of gamma Correction
0x3B	0x7D	R/W	[7:0]: Blue color GAMMA 192[7:0] of gamma Correction
0x3C	0xF2	R/W	[7:0]: Blue color GAMMA 224[7:0] of gamma Correction
0x3D	0x8E	R/W	[7:0]: Blue color GAMMA 240[7:0] of gamma Correction
0x3E	0x52	R/W	[7:0]: Blue color GAMMA 248[7:0] of gamma Correction
0x3F	0x00	R/W	[7:0]: Blue color GAMMA 256[7:0] of gamma Correction

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<Input format standard>

R02[1:0]	0	1(Default)	2
Input Format	RGBDummy	YUV	Through mode

R02[2]	0(Default)	1
Format standard	NTSC/QVGA	PAL

R02[3]	0	1(Default)
Valid data for RGBDm or YUV	1280	1440

<Input data and clock>

R02[4]	0(Default)	1
Latch data edge	Positive Edge	Negative

R02[5]	0(Default)	1
HD Polarity	Low pulse	High pulse

R02[6]	0(Default)	1
VD Polarity	Low pulse	High pulse

R03[0]	0(Default)	1
Interlace Mode	Interlace	Non-interlace

R03[1]	0(Default)	1
Even Field Blanking	L2=L1	L2=L1-1

R03[3:2]	0(Default)	1	2	3
YCbCr sequence	CbYCrY	YCrYCb	CrYCbY	YCbYCr

R03[4]	0	1(Default)
YUV transfer matrix	Matrix A	Matrix B

Matrix A

$$R=Y+1.402Cr$$

$$G=Y-0.714Cr-0.344Cb; [Y=0\sim 255, Cr\&Cb=-128\sim 127]$$

$$B=Y+1.772Cb$$

Matrix B

$$R=1.16(Y-16)+1.60(Cr-128)$$

$$G=1.16(Y-16)-0.81(Cr-128)-0.39(Cb-128); [Y=16\sim 255, Cr \& Cb=-16\sim 240]$$

$$B=1.16(Y-16)+2.02(Cb-128)$$

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R03[5]	0	1(Default)
UV offset for Format A	Binary (0~255)	2's complement (-128~127)

R03[7:6]	0(Default)	1	2
Driver capability	50 %	75 %	100 %

R04[0]	0	1(Default)
Low power mode	Standby	Normal

Function pin	XSTV, XSTH, CKV, CKH ENB, XPCG CP_CLK1	STV, STH, XCKV, XCKH XENB, PCG, DOUT[24:1], PCD, VCOM, CP_CLK2
Standby	High	Low

R04[3]	0	1(Default)
Pre-charge	Disable	Enable

R04[7:4]	VCOM inversion mode
0000	1 line inversion (Default)
0001	1+2 line inversion, field sequence 2, 4, 2, 4
0010	2+2 line inversion, field sequence 1, 3, 1, 3
1000	1+2/2+2 line inversion, field sequence 1, 2, 4, 3
1001	1+2/2+2 line inversion, field sequence 1, 3, 4, 2
1010	1+2/2+2 line inversion, field sequence 1, 4, 2, 3
1011	1+2/2+2 line inversion, field sequence 1, 3, 2, 4
1100	1+2/2+2 line inversion, field sequence 1, 4, 3, 2
1101	1+2/2+2 line inversion, field sequence 1, 2, 3, 4
others	Setting prohibited.

+	+	+	+
+	+	+	+
-	-	-	-
-	-	-	-

1

-	-	-	-
+	+	+	+
+	+	+	+
-	-	-	-

2

-	-	-	-
-	-	-	-
+	+	+	+
+	+	+	+

3

+	+	+	+
-	-	-	-
-	-	-	-
+	+	+	+

4

*** R04[7:4]=0000 is suggested to use for best quality.

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<Direction Control>

R05[0]	0	1(Default)
Horizontal reverse	Reverse	Normal

R05[1]	0	1(Default)
Vertical reverse	Reverse	Normal

<Color filter selection for 960x240>

R05[2]	0(Default)	1
Color filter	Delta	Strip

<Output sample and hold phase>

R05[6:3]	0	1	2	3	4	5 (default)	6	7	8	9	0xA	0xB	0xC	0xD	0xE	0xF
Output phase	0	SH 1	SH 2	SH 3	SH 4	SH 5	SH 6	SH 7	SH 8	SH 9	SH 10	SH 11	SH 12	SH 13	SH 14	SH 15

R05[7]: Don't care.

<Shift Display Area>

R06[5:0]	0x0	0x18(Default)	0x2D
STH phase	Advance 24 DCLK	Center	Delay 21 DCLK
Display position	Shift right 24 dot	Center	Shift left 21 dot

R06[6]	1(default)	0
NBW selection	NB	NW

Note 3: NB for normal black panel, NW for normal white panel.

R06[7]	1(default)	0
DS selection	Full mode	Setting prohibited

Note 4: Through mode doesn't support the function.

<STV Position>

R07[3:0]	0x0	0x8(Default)	0xF
STV phase	Advance 8H	Center	Delay 7H

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Display position	Shift down 8 Line	Center	Shift up 7 Line
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R07 [6:4]	0x00	0x02	0x07(Default)
Resolution	480x240	640x240	960x240

R07 [7]	0x0(Default)	0x01
Pin and register priority	Pin (Hardware)	Register (Software)
Function	SHDB RS[3:1] NBW	R04[0] R07[6:4] R06[6]

Note: Panel fixes hardware pin RS[3:1] and NBW already. Don't suggest choice hardware pin control.

<Gate non-overlap>

R08[5:0]	0x0(Default)	0x3F
ENB negative position	Origin	Shift right 63 DCLK

***Panel internal control signal. Don't suggest modifying it.

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<Contrast and Brightness>

$$D_{\text{contrast}} = D_{\text{in}} * \text{Gain}$$

R09 [5:0]	0x00	0x20(Default)	0x3F
R Gain of Contrast	0.00000	1.00000	1.96875
R0A [5:0]	0x00	0x20(Default)	0x3F
G gain of contrast	0.00000	1.00000	1.96875
R0B [5:0]	0x00	0x20(Default)	0x3F
B gain of contrast	0.00000	1.00000	1.96875

$$D_{\text{brightness}} = D_{\text{contrast}} + \text{Offset}$$

R0C [5:0]	0x00	0x10(Default)	0x3F
R Offset of Brightness	-16	0	47
R0D [5:0]	0x00	0x10(Default)	0x3F
G Offset of Brightness	-16	0	47
R0E [5:0]	0x00	0x10(Default)	0x3F
B Offset of Brightness	-16	0	47

<Voltage Level>

$$V_{\text{comH}} = 2.94 + 0.02 * R0F, V_{\text{comL}} = 2.0 - 0.02 * R10$$

R0F[6:0]	0x00	0x53(default)	0x67
Vcom high level	2.94	4.60	5.0

R10[6:0]	0x00	0x5A(Default)	0x5F
Vcom low level	2.0	0.20	0.1

$$V_{\text{pcd}} = 0.22 + 0.08 * R12$$

R11[5:0]	0x00	0x1D(Default)	0x3C
PCD level	0.2	2.52	5.0

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<Gamma Output voltage level>

Define DAC low reference voltage:

R12[3:0]	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC (default)	0xD	0xE	0xF
Voltage	0.3	0.35	0.4	0.45	0.5	0.55	0.6	0.65	0.7	0.75	0.8	0.85	0.9	0.95	1.0	1.05

Define DAC high reference voltage:

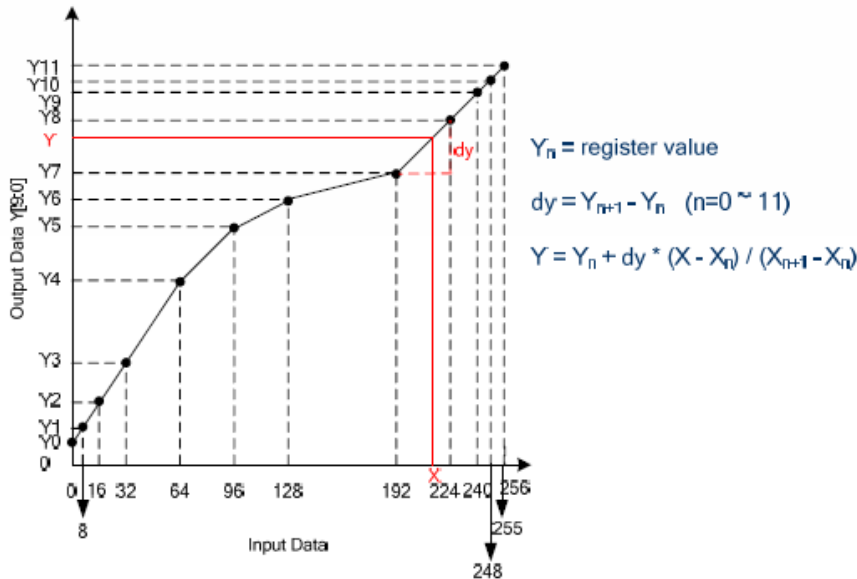
R12[7:4]	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC (default)	0xD	0xE	0xF
Voltage	3.5	3.6	3.7	3.8	3.9	4.0	4.1	4.2	4.3	4.4	4.5	4.6	4.7	4.8	4.9	5.0

R13~R3F: Gamma correction

The gamma correction function for red, green, and blue individual color is provided. The gamma correction is done by 11-segment piecewise linear interpolation. The 11 segments are defined with 12 register values for level 0, 8, 16, 32, 64, 96, 128, 192, 224, 240, 248, and 256 for positive polarity. Negative polarity data are generated symmetrically. The gamma correction output is then fed to DAC and OP to drive the source lines on the panel.

The following figure shows the concept of gamma correction with interpolation. The gamma reference point register values must be fine-tuned to fit LC characteristics of the panel.

Normally black gamma concept



表單編號:

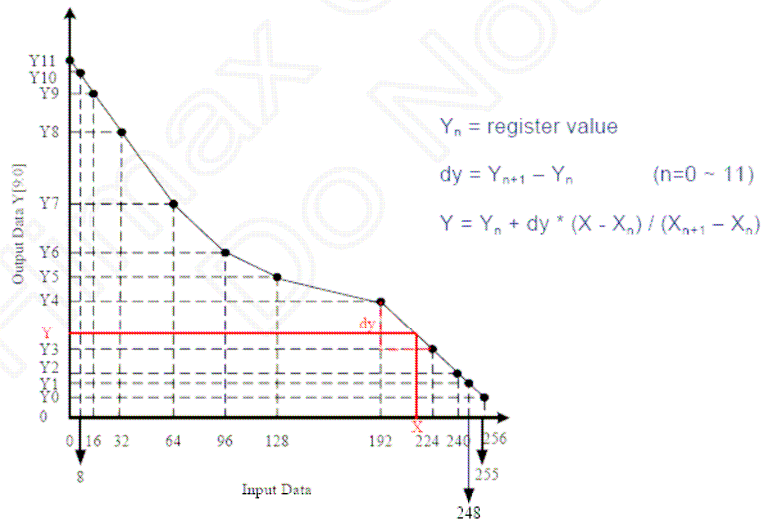
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Normally white gamma concept



Example of gamma setting:

Normally black

Addr	0X13	0X14	0X15	0X16	0X17	0X18	0X19	0X1A	0X1B	0X1C	0X1D	0X1E	0X1F	0X20	0X21
Value	1A	AB	FF	00	DF	0C	33	5E	86	B3	20	73	B0	D4	FF
Addr	0X22	0X23	0X24	0X25	0X26	0X27	0X28	0X29	0X2A	0X2B	0X2C	0X2D	0X2E	0X2F	0X30
Value	1A	AB	FF	00	DF	0C	33	5E	86	B3	20	73	B0	D4	FF
Addr	0X31	0X32	0X33	0X34	0X35	0X36	0X37	0X38	0X39	0X3A	0X3B	0X3C	0X3D	0X3E	0X3F
Value	1A	AB	FF	00	DF	0C	33	5E	86	B3	20	73	B0	D4	FF

Normally white

Addr	0X13	0X14	0X15	0X16	0X17	0X18	0X19	0X1A	0X1B	0X1C	0X1D	0X1E	0X1F	0X20	0X21
Value	FE	95	50	D2	83	1D	A0	3B	F6	C8	76	41	1A	F9	00
Addr	0X22	0X23	0X24	0X25	0X26	0X27	0X28	0X29	0X2A	0X2B	0X2C	0X2D	0X2E	0X2F	0X30
Value	FE	95	50	D2	83	1D	A0	3B	F6	C8	76	41	1A	F9	00
Addr	0X31	0X32	0X33	0X34	0X35	0X36	0X37	0X38	0X39	0X3A	0X3B	0X3C	0X3D	0X3E	0X3F
Value	FE	95	50	D2	83	1D	A0	3B	F6	C8	76	41	1A	F9	00

Note 5: Above tables merely are setting examples; the best gamma curve should be fine-tuned case by case.

表單編號:

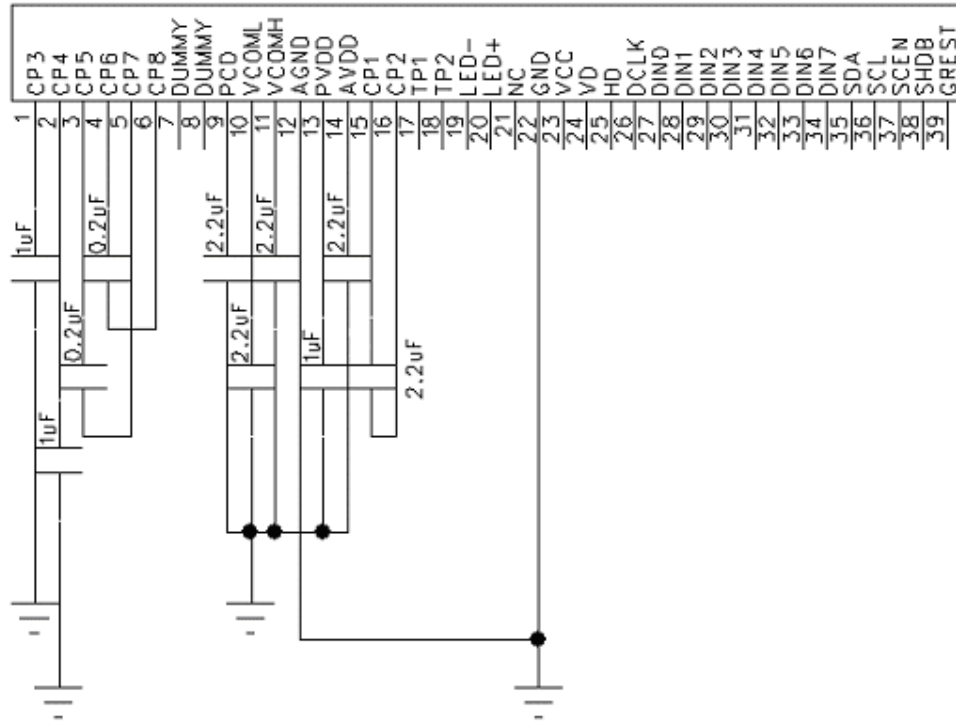
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Appendix I 39pin FPC connector application circuit



Application Side	Capacitance (F)	Rated Voltage (V)	Remark
CP1	2.2u	16	Suggest Using X5R Dielectric
CP2			
CP3	1u	16	
CP4	1u	25	
CP5	0.2u	25	
CP7			
CP6	0.2u	25	
CP8			
PCD	2.2u	16	
VCOML	2.2u	16	
VCOMH	2.2u	16	
PVDD	1u	16	
AVDD	2.2u	16	

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